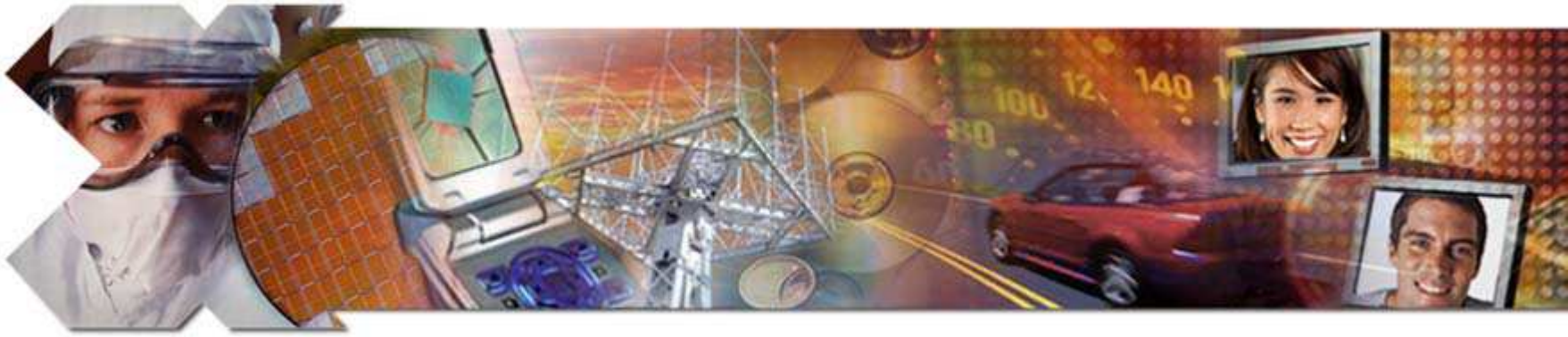


The Next Generation 65-nm FPGA

Steve Douglass, Kees Vissers, Peter Alfke
Xilinx
August 21, 2006

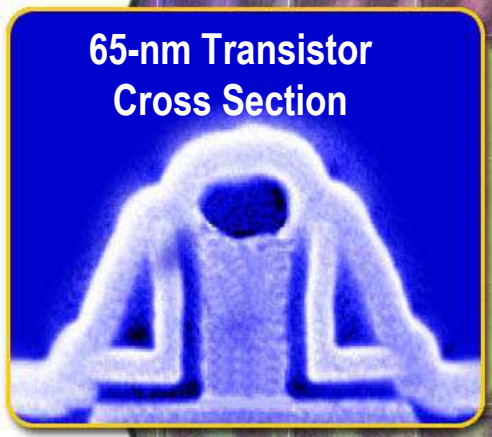
XILINX®

Structure of the talk

- 65nm technology going towards 32nm
- Virtex-5 family
- Improved I/O
- Benchmarking Virtex-5 LUT6 fabric
- New Microblaze in Virtex-5 fabric
- Conclusion

65nm Process Technology

- 40-nm gate length (physical poly)
- 1.6nm oxide thickness (16 Angstrom)
  - ~5 atomic layers
- Triple-Oxide II technology
  - 3 oxide thicknesses for optimum power and performance
- 1.0 Vcc core
  - Lower dynamic power
- Mobility engineered transistors (strained silicon)
  - Maximum performance at lowest AC power



Over 1 Billion Transistors on a 23 x 23 mm Chip

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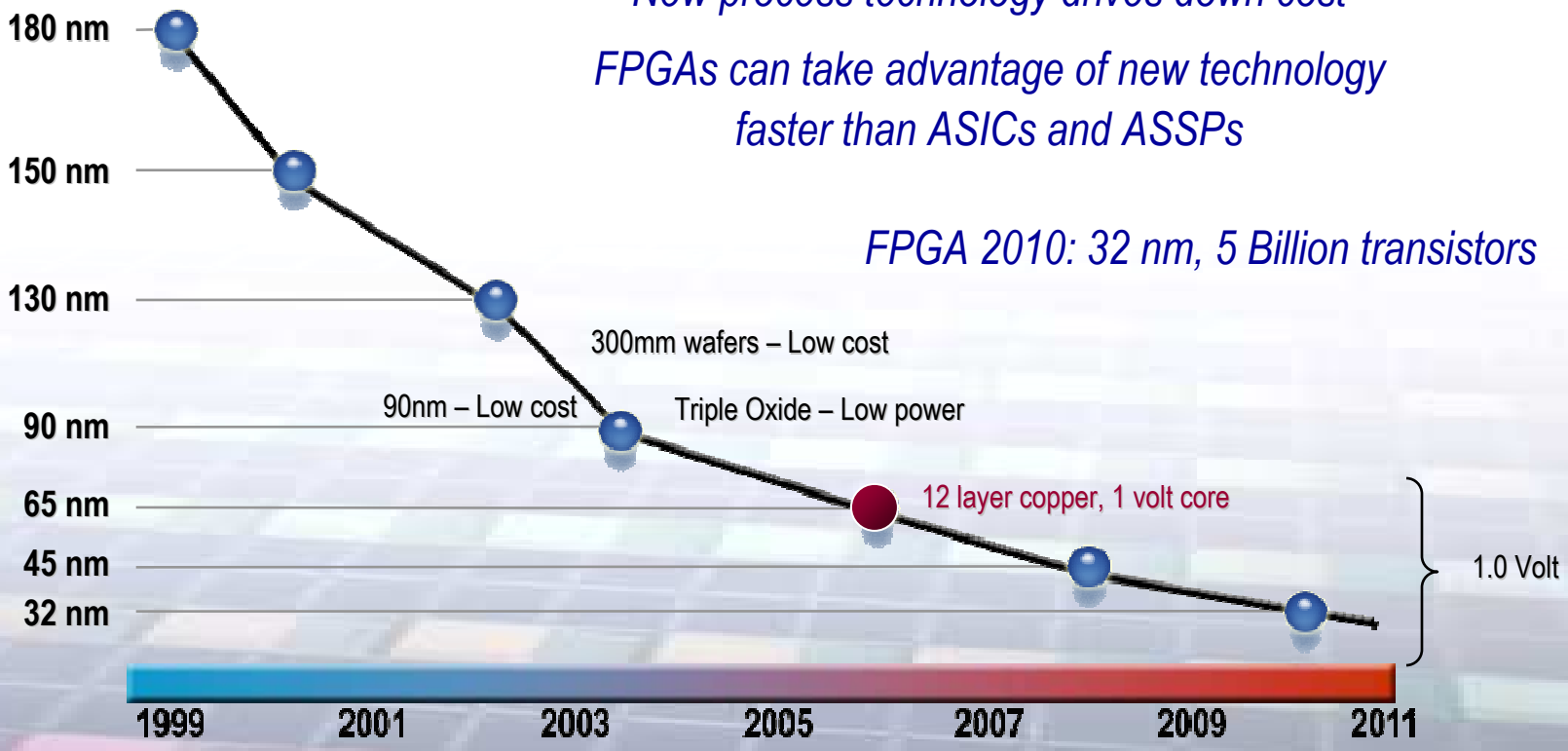
FPGAs Drive the Process



The cost of IC development increases. Therefore customers want to buy reconfigurable and programmable platforms, instead of developing their own.

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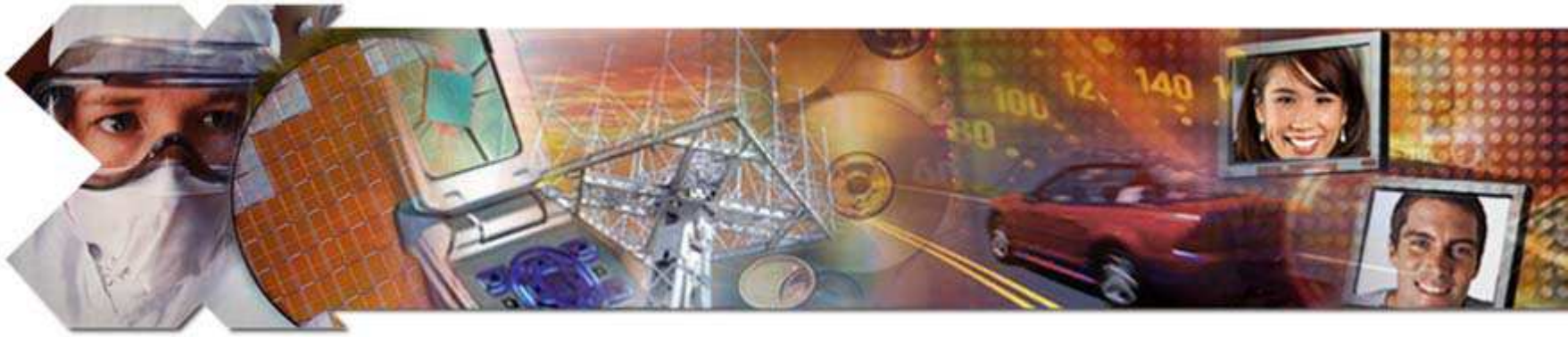
Challenges

- Higher leakage current and stand-by power
- Lower Vcc: good for power, tough for decoupling
  - 3.3-V compatibility is getting more difficult
  - 1 billion transistors, large chips, heat density
  - 12-layer chip, 10-layer package, 16-layer pc-board
- Faster transitions, 2 V/ns and 50 mA/ns per pin,
  - Pc-board signal integrity problems

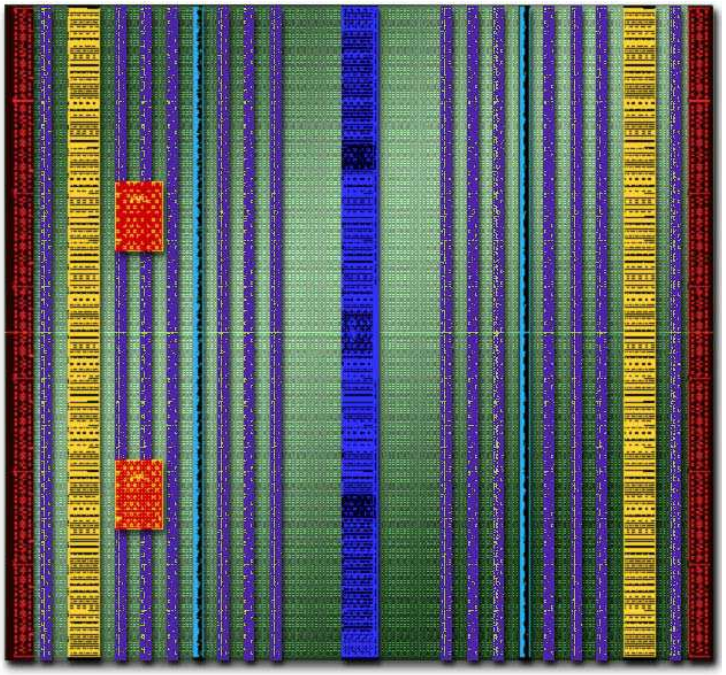
Complex chip, complex package, complex board



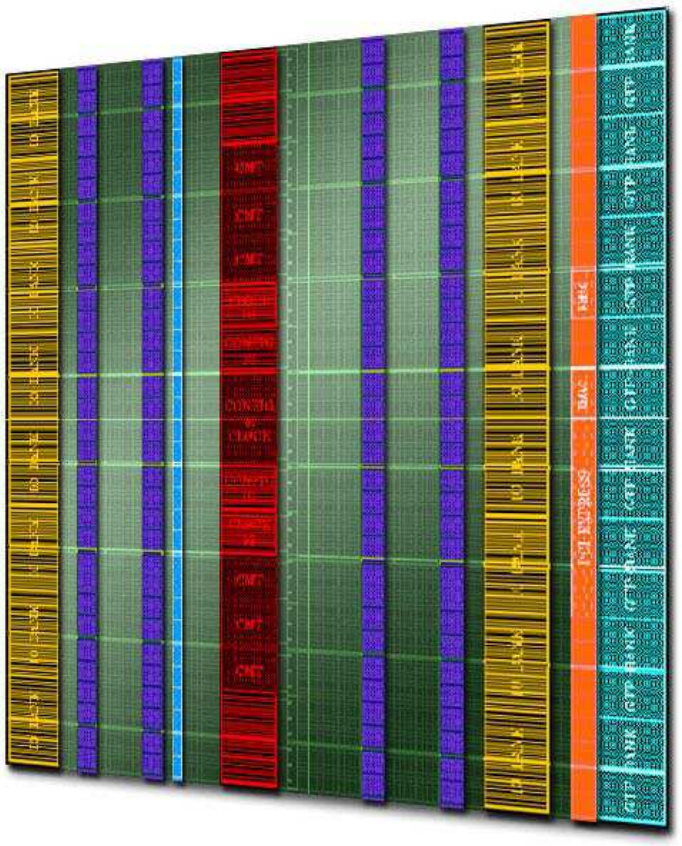
LX Platform Overview

Two Generations of ASMBL

(Application-Specific Modular BLock Architecture)



Virtex-4

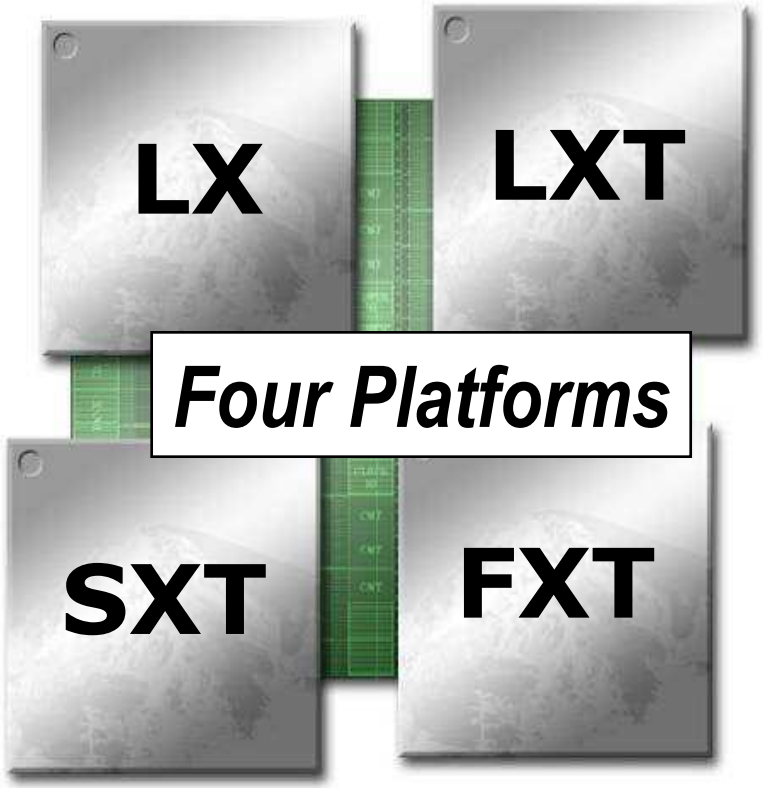


Virtex-5

2nd Generation of ASMBL

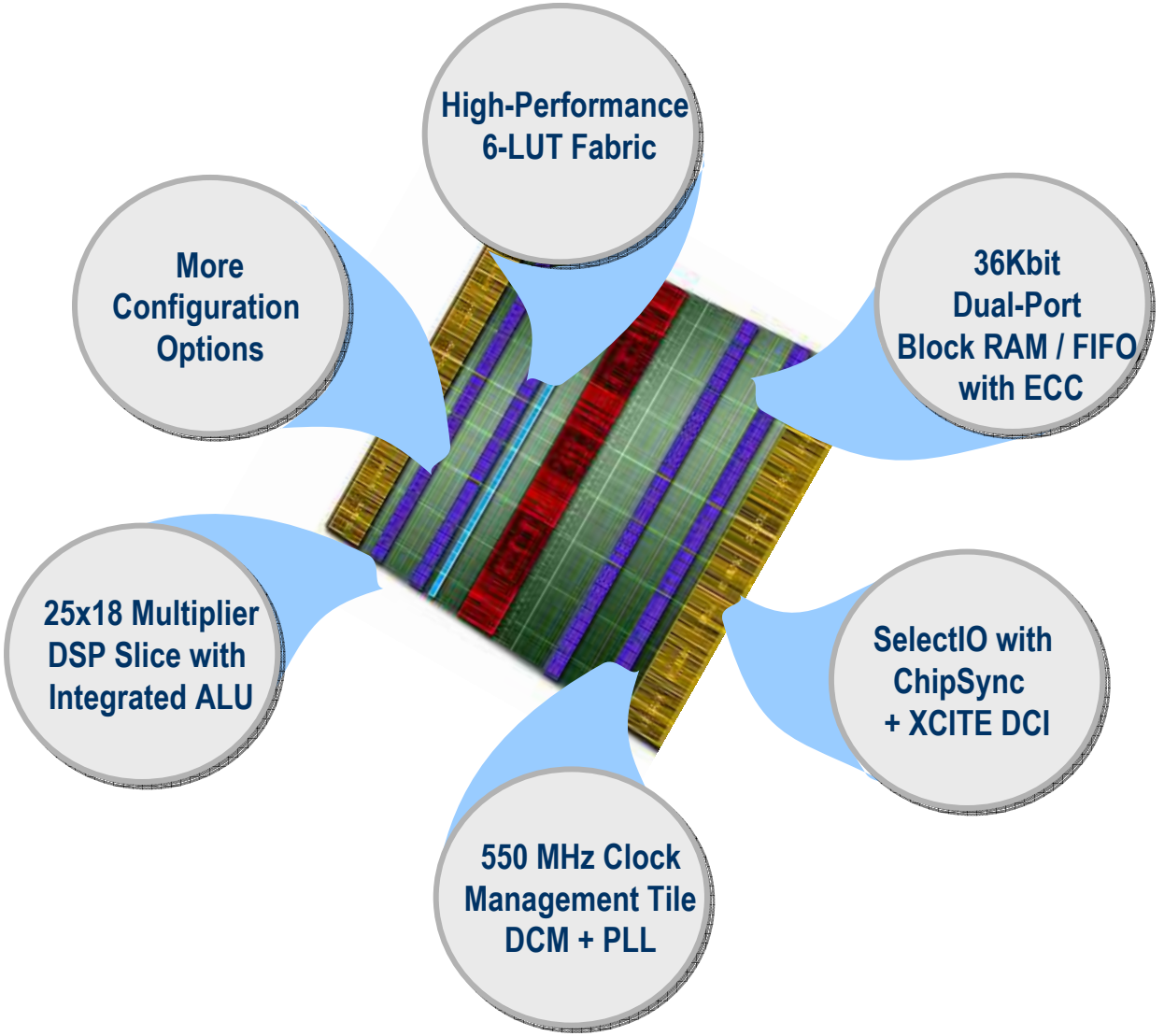
Easy to create sub-families

- **LX** : Logic + parallel IO
- **LXT**: Logic + serial I/O
- **SXT**: DSP + serial I/O
- **FXT**: PPC + fastest serial I/O



Many choices to optimize cost and performance

System components



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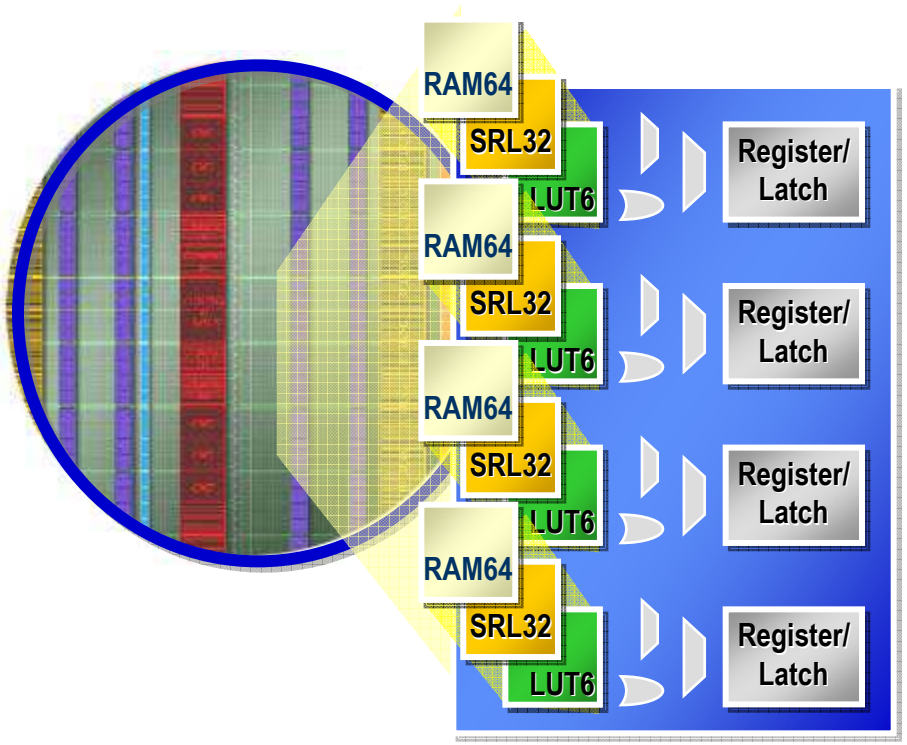
Virtex-5 Logic Architecture

- True 6-input LUTs
  - with dual 5-input LUT option
  - 1.4 times the value for actual logic
  - only 1.15 times the cost in silicon ar
- 64-bit RAM per M-LUT
  - about half of all LUTs
- 32-bit or 16-bit x 2
  - shift register per M-LUT



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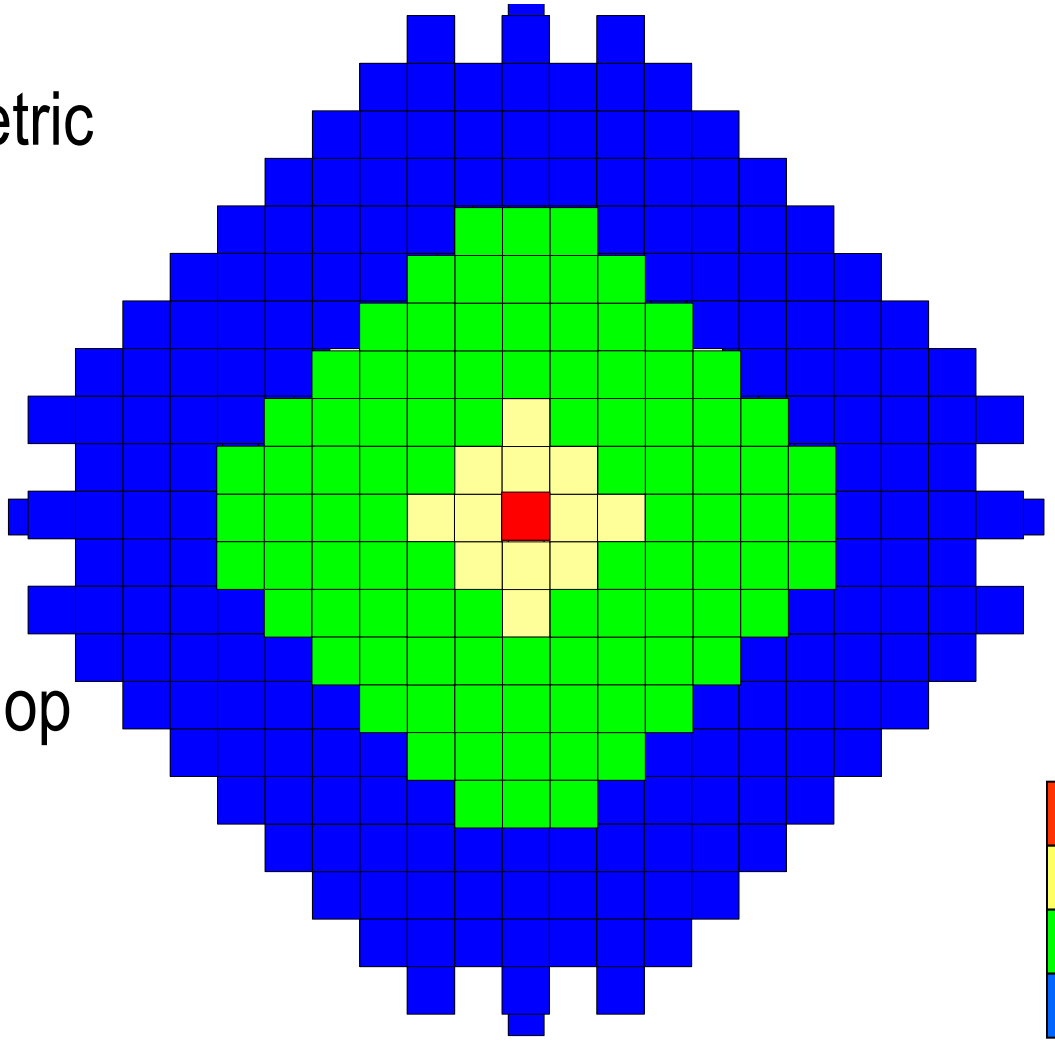
Virtex-5 Routing

More symmetric pattern, connecting CLBs

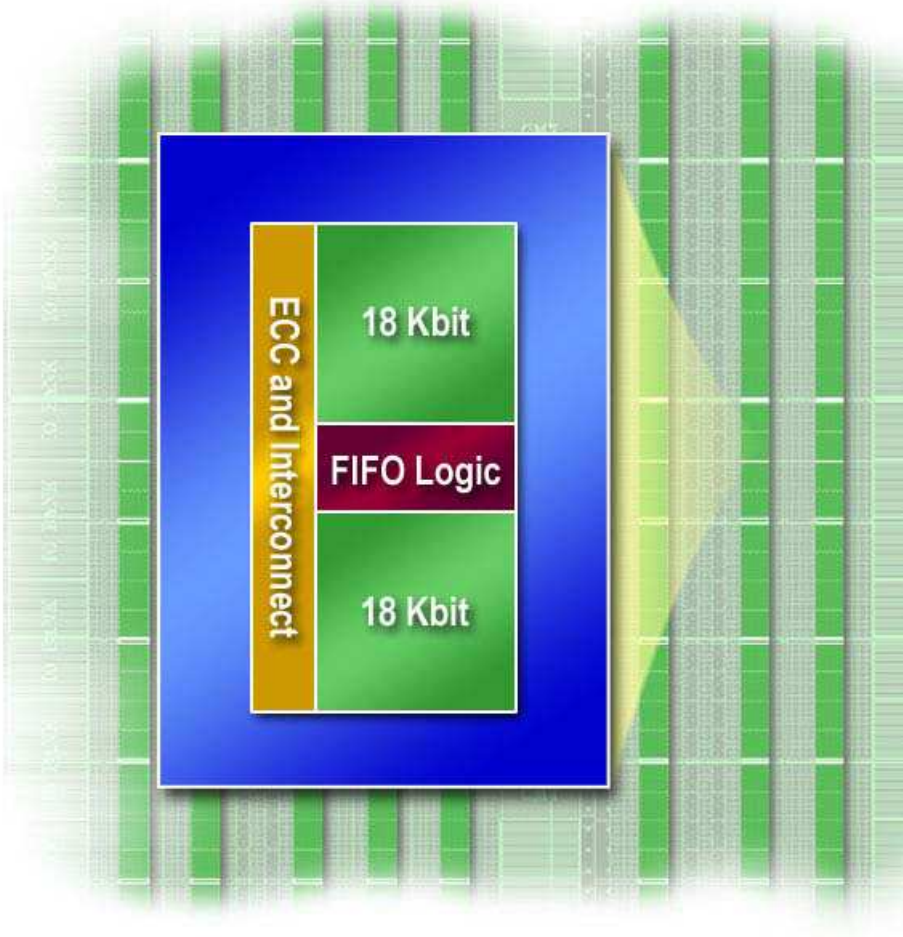
More logic reached per hop

Same pattern for all outputs



BRAM/FIFO

- 36 Kbit BRAM
  - Integrated FIFO Logic for multi-rate designs
  - Built-in ECC
  - Cascadable to build larger RAM arrays
  - Dual Port: a read and write every clock cycle
- Performance up to 550 MHz

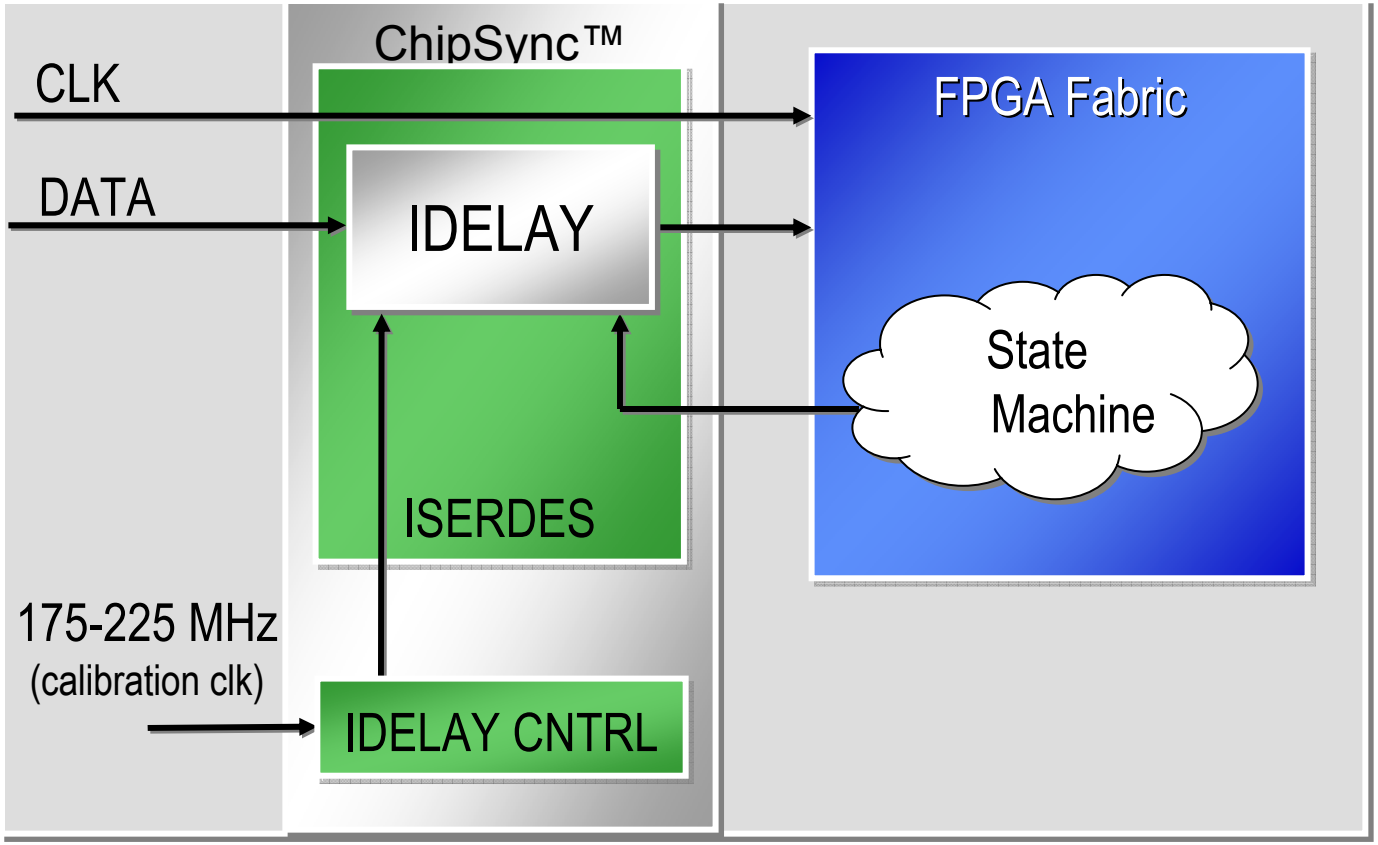


General Purpose I/O (Select I/O)

- All I/O pins are “created equal”
- Compatible with >40 different standards
  - Vcc, output drive, input threshold, single/differential, etc
- Each I/O pin has **dedicated circuitry** for:
  - On-chip transmission-line termination (serial or parallel)
  - Fine timing adjustment in 75 ns steps (IDELAY + ODELAY)
  - Serial-to-parallel converter on the input (CHIPSYNC)
  - Parallel -to-serial converter on the output (CHIPSYNC)
  - Clock divider, and high-speed “regional” clock distribution

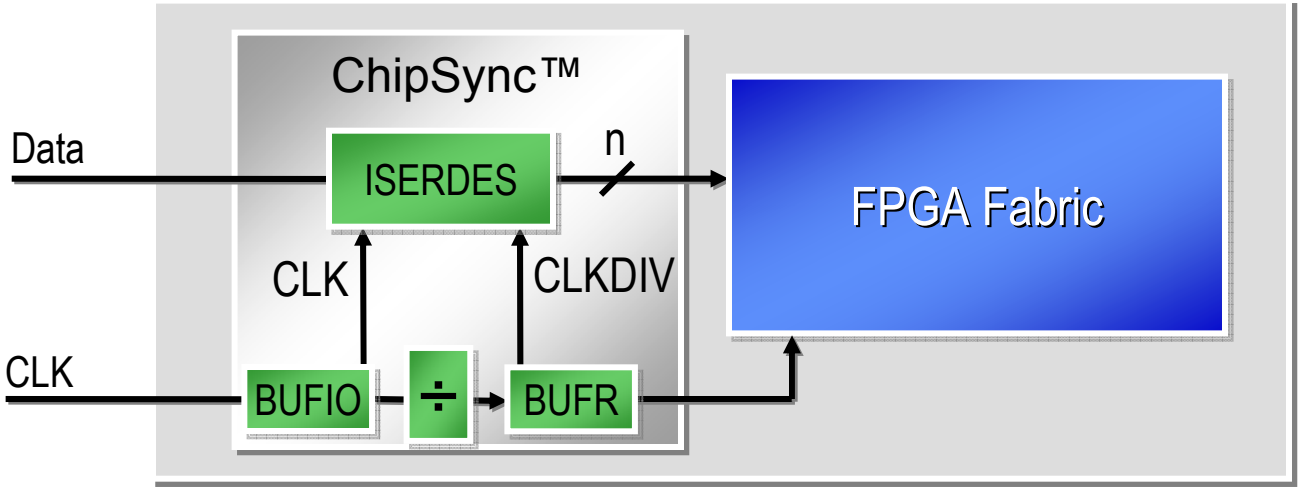
Ideal for source-synchronous I/O up to 1 Gbps

75-ps Incremental Alignment



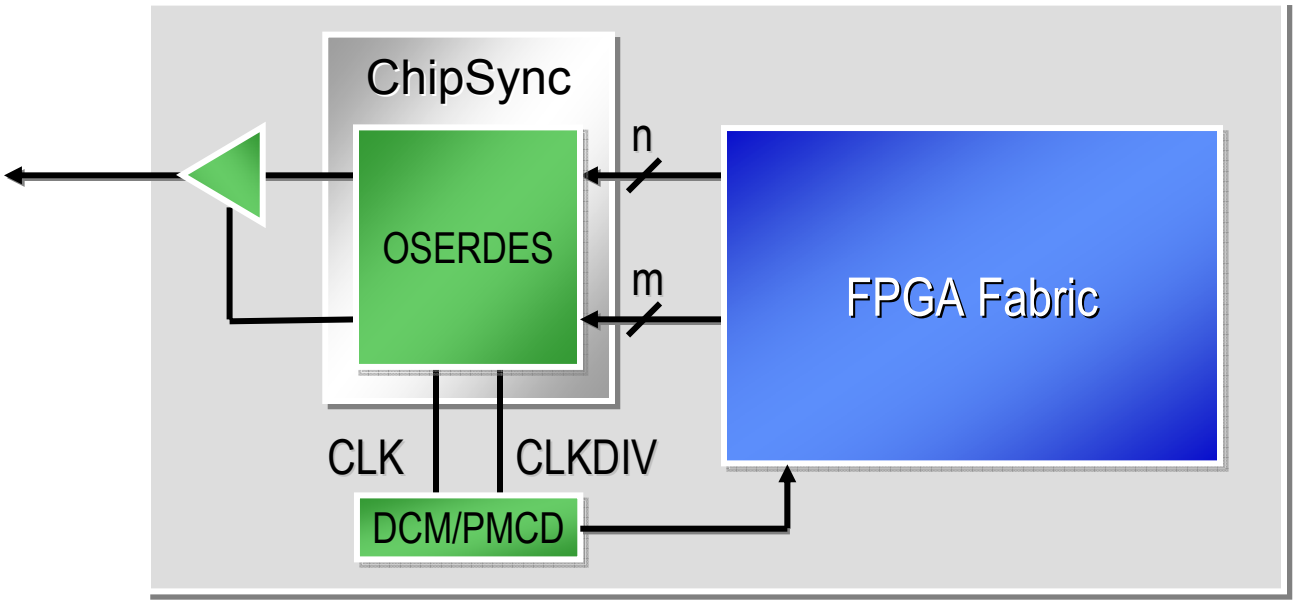
- Calibration clock can be internal or external
- 64 delay elements of ~ 70 to 89 ps each

ISERDES for Incoming Data

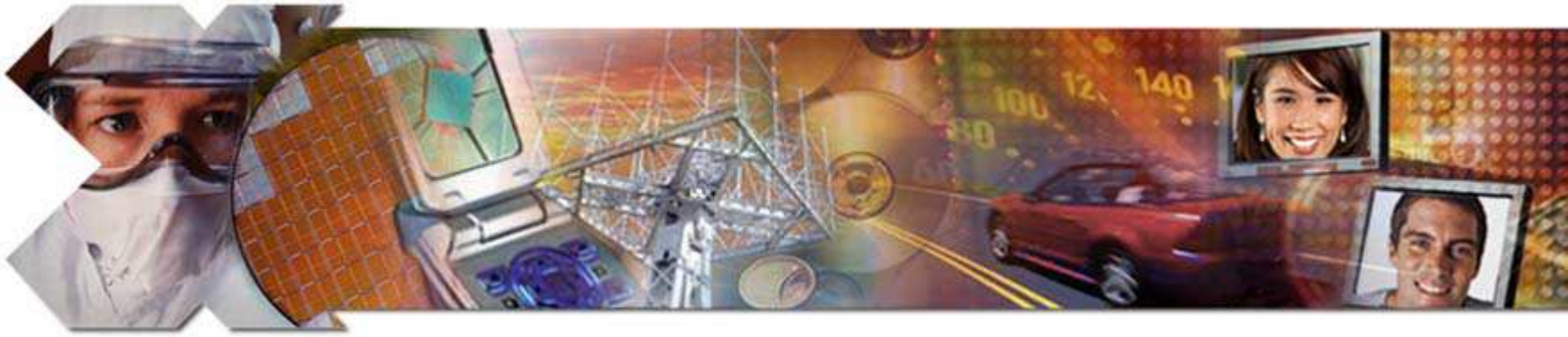


- Clock frequency division widens internal data path
  - n = 2, 3, 4, 5, 6, 7, 8, 10 bits
- Dynamic signal alignment
  - Bit alignment, Word alignment, Clock alignment
- Supports Dynamic Phase Alignment (DPA) using IDELAY

OSERDES for Outgoing Data



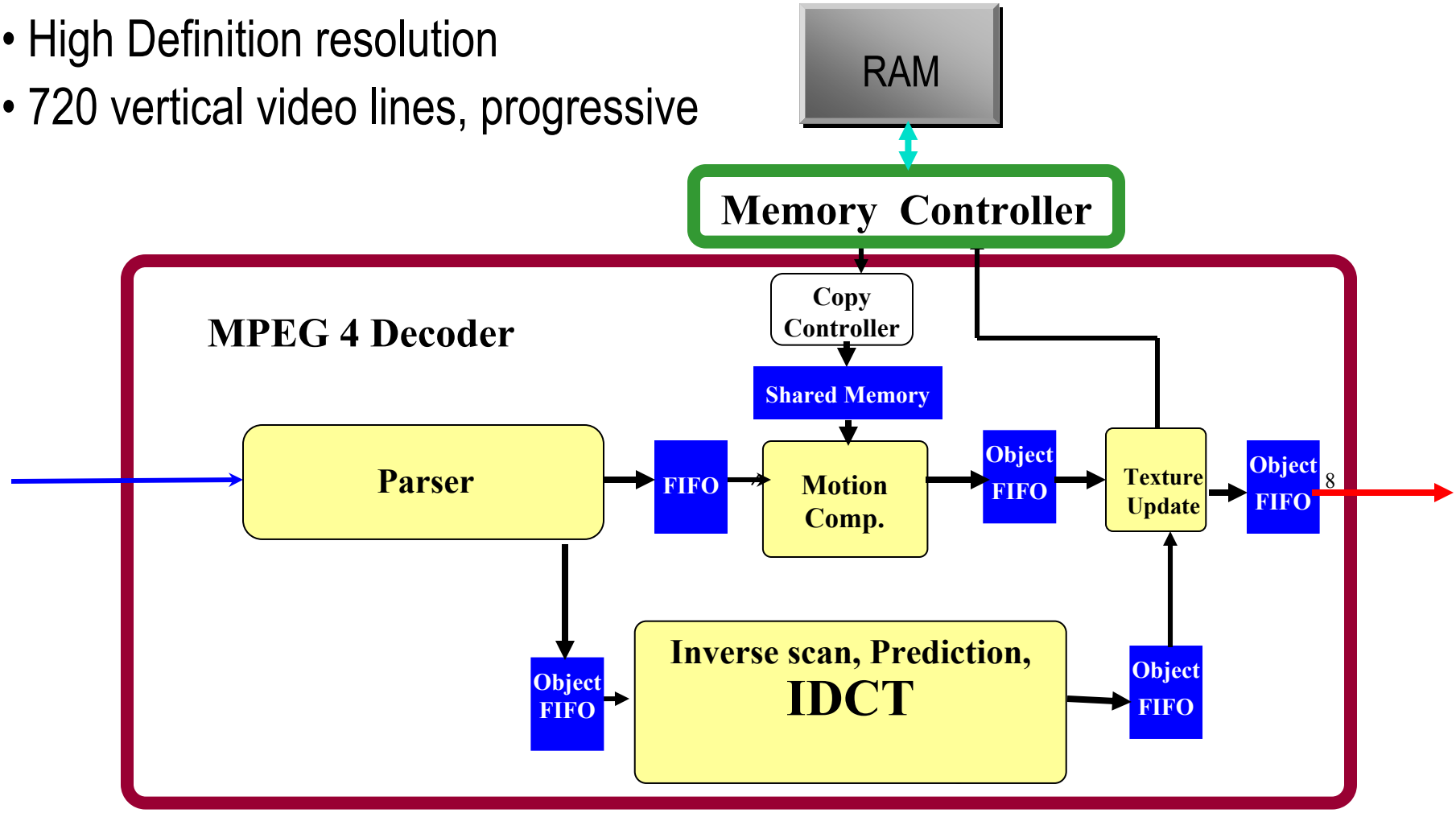
- Parallel-to-Serial converter
  - Data SERDES: 2, 3, 4, 5, 6, 7, 8, 10 bits
  - Three-state control SERDES: 1, 2, 4 bits



Virtex-5 Applications Benchmarks

One MPEG4 Video Decoder

- High Definition resolution
- 720 vertical video lines, progressive



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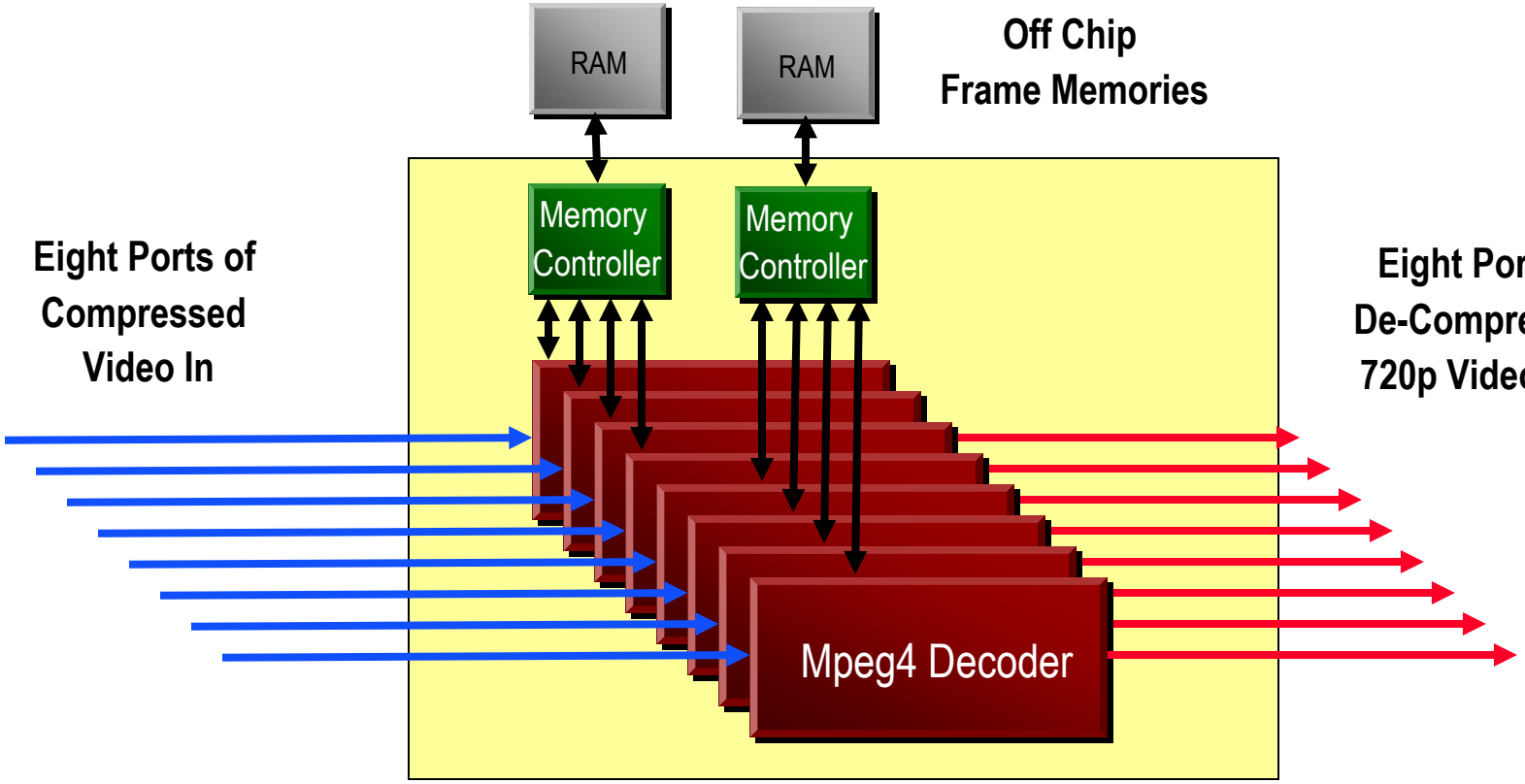
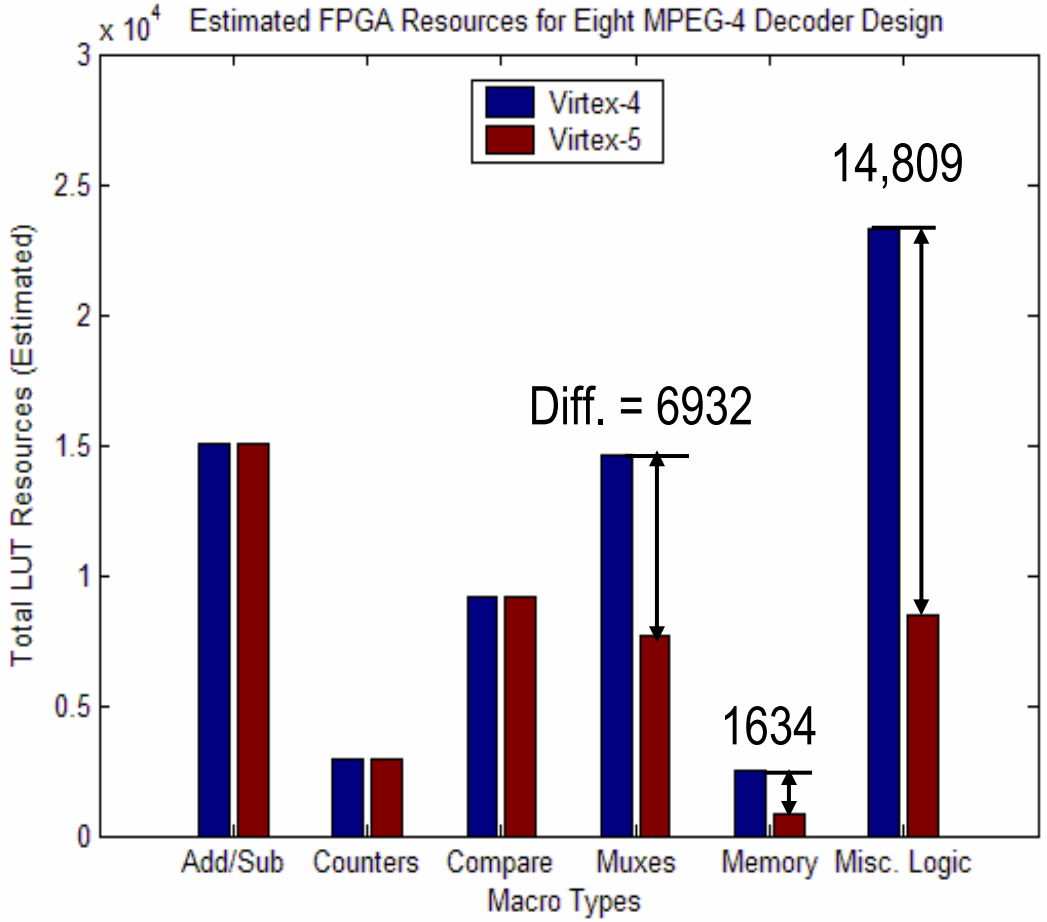
8 MPEG4 decoders



Category	Virtex-4	Virtex-5
Tools	XST/ISE 8.1.02i	XST/ISE 8.2i
Devices	XC4VFX140-11	Virtex5 part

8 Decoders: Resources



Design Resources	Virtex-4	Virtex-5
	Used	Used
Registers	21,248	20,242
LUTs	**67,523**	**44,148**
BlockRAMs	233	233
DSP Elements	192	216

- 35% fewer LUTs
- dramatic improvements for multiplexers, memory, and misc. logic
- Same VHDL source code used for both designs

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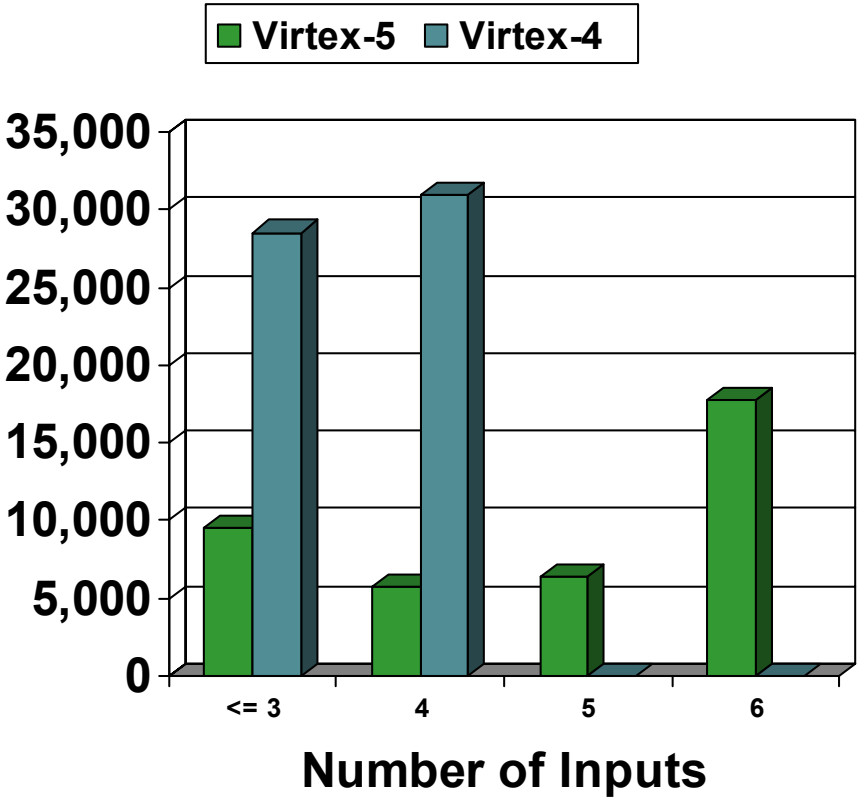
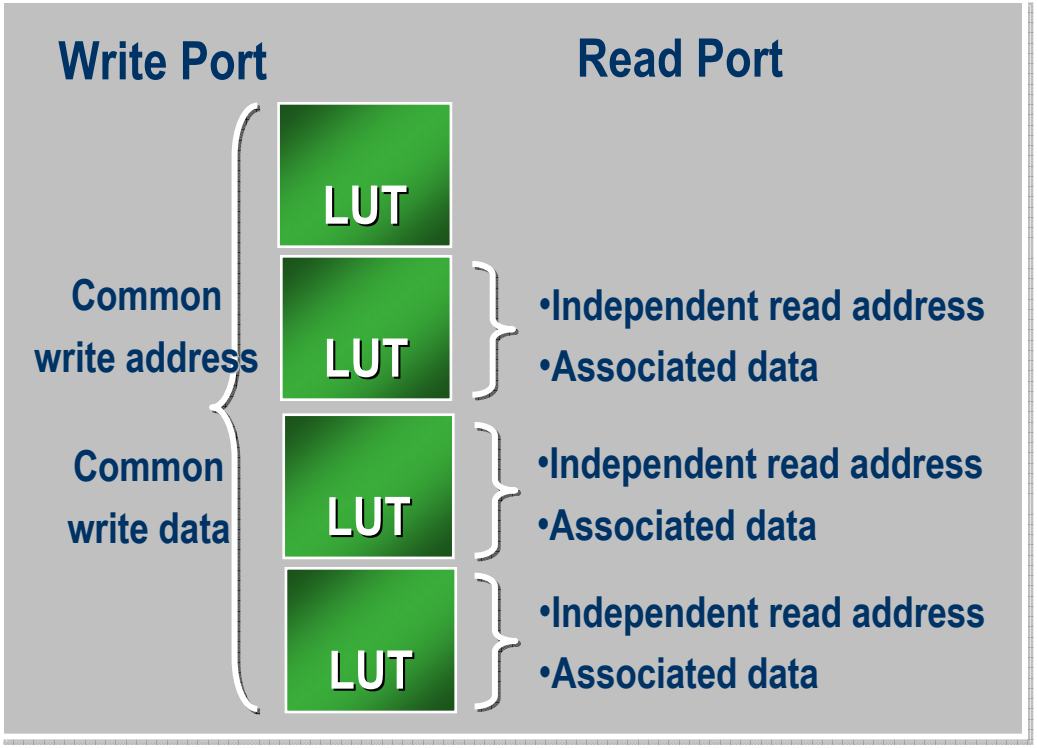
Logic Synthesis-Driven Results



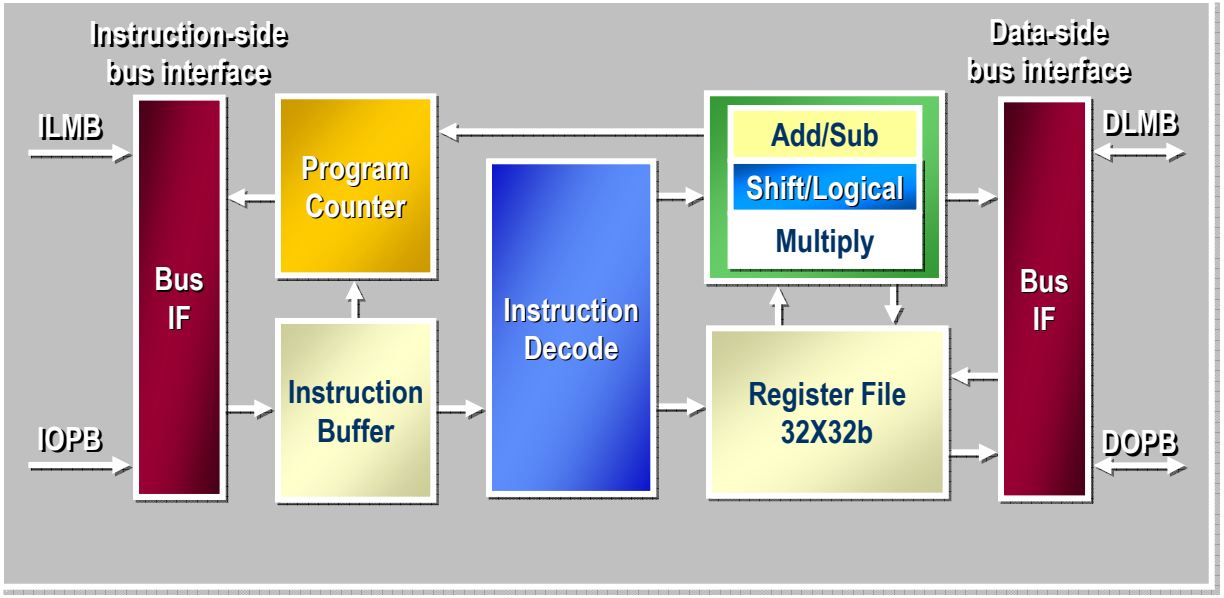
- Synthesis uses 6-input LUTs efficiently : fewer logic levels
- 23% increase in synthesized frequency, from 95MHz to 117MHz
- From 720p to 1080p video standards with little effort

Quad-Port Memory in Four LUT6

- Write Port: Four LUT6s share the data input and can also share a distributed write address
- Read Ports: Three independent read operations
- 32 x 32 Quad-Port RAM structure in 64 LUTs
- 6x density improvement over Virtex-4



Application Example: new MicroBlaze 5.0

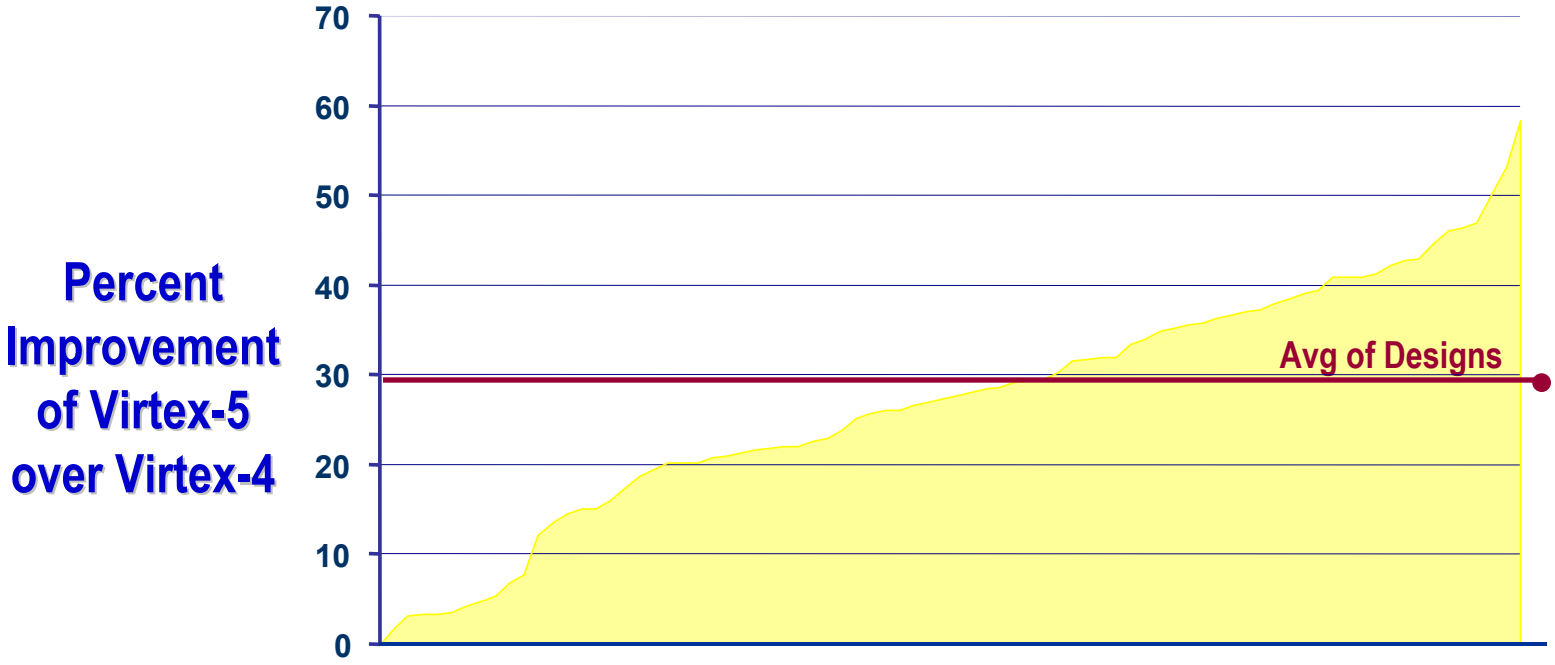


- Better use of new LUTs
  - 1269 LUT4s in Virtex-4, MB 4.0
  - 1400 LUT6s in Virtex-5, MB 5.0
- from 3 stage -> 5 stage pipeline
- new processor: from 0.92 DMips/MHz to 1.14 DMips/MHz
- 180MHz -> 201 MHz
- 166 -> 230 Dhrystone Mips

Use new 6 LUT, 2 stage deeper pipe, 10% more MHz, 39% better performance

Suite of Benchmarks

Suite of 74 designs run against ISE8.1i
Slow speedgrade (-10) Virtex-4 compared to slow speedgrade (-1) Virtex-5

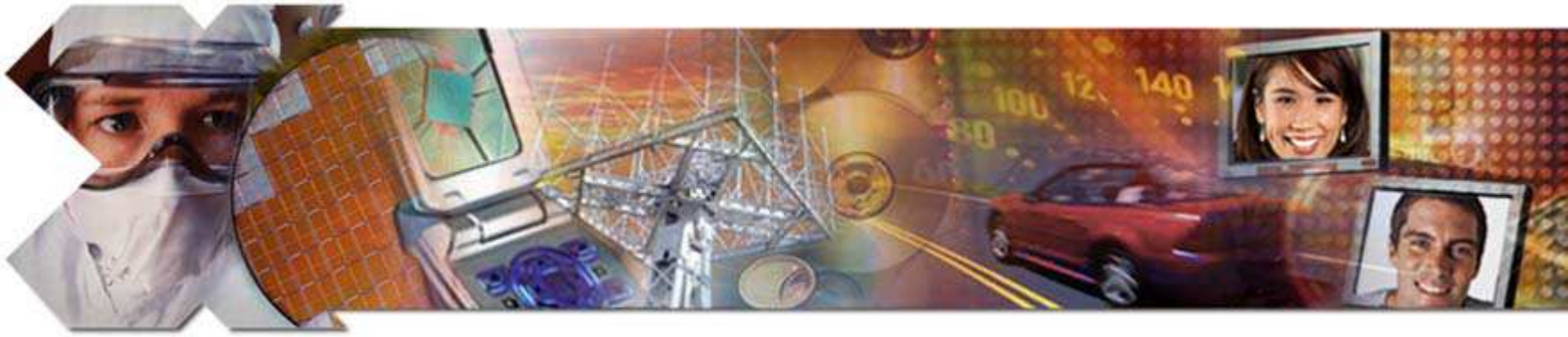


~30% average advantage for Virtex-5 fabric vs. Virtex-4

- As high as 56% advantage for some designs

Virtex-5: Summary

- Leading 65 nm technology FPGA platform
- Better input and output I/O on all pins
- New 6-input LUT logic that is 30% better
- Demonstrated example of video benchmark with 35% fewer LUTs and 23% increased frequency
- New Microblaze with 39% improved performance
- Expect more: new announcements on serial I/O and integrated processor technology very soon



Appendix: Virtex-5 LX

Virtex-5 LX Platform

			5VLX30	5VLX50	5VLX85	5VLX110	5VLX220	5VLX330
Logic Cells			30,720	46,080	82,944	110,592	221,184	331,776
LUT6/FFs			19,200	28,800	51,840	69,120	138,240	207,360
Distributed RAM Kbits			320	480	840	1,120	2,280	3,420
Block RAM Kbits			1,152	1,728	3,456	4,608	6,912	10,368
CMTs			2	6	6	6	6	6
DSP48E Slices			32	48	48	64	128	192
Total I/O Banks			13	17	17	23	23	35
EasyPath			No	No	Yes	Yes	Yes	Yes
Package	**Size**	**IO**						
FF324	19	220	220	220				
FF676	27	440	400	440	440	440		
FF1153	35	800		560	560	800		
FF1760	42.5	1,200				800	800	1,200