Home entertainment-quality multimedia experience whilst on the move

-Philips Nexperia™ Mobile Multimedia Processor PNX4103

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Philips Semiconductors

Acknowledgements

The PNX4103 represents the work of more than 100 engineers from Philips Semiconductors in:

- France : *Sophia Antipolis, Caen*
- The Netherlands : *Nijmegen, Eindhoven*
- India : *Bangalore*
- UK : *Redhill*
- USA : *San Jose*

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Quiz

- Would you use your mobile phone as the only camera at your daughter's wedding ?
- Would you use your mobile phone to download a movie, connect to your new HD TV with Dolby-Digital 5.1 and invite your friends over?
- Would you use your mobile phone to record the World Cup Finals?

Well … That'd be our target for the PNX4103

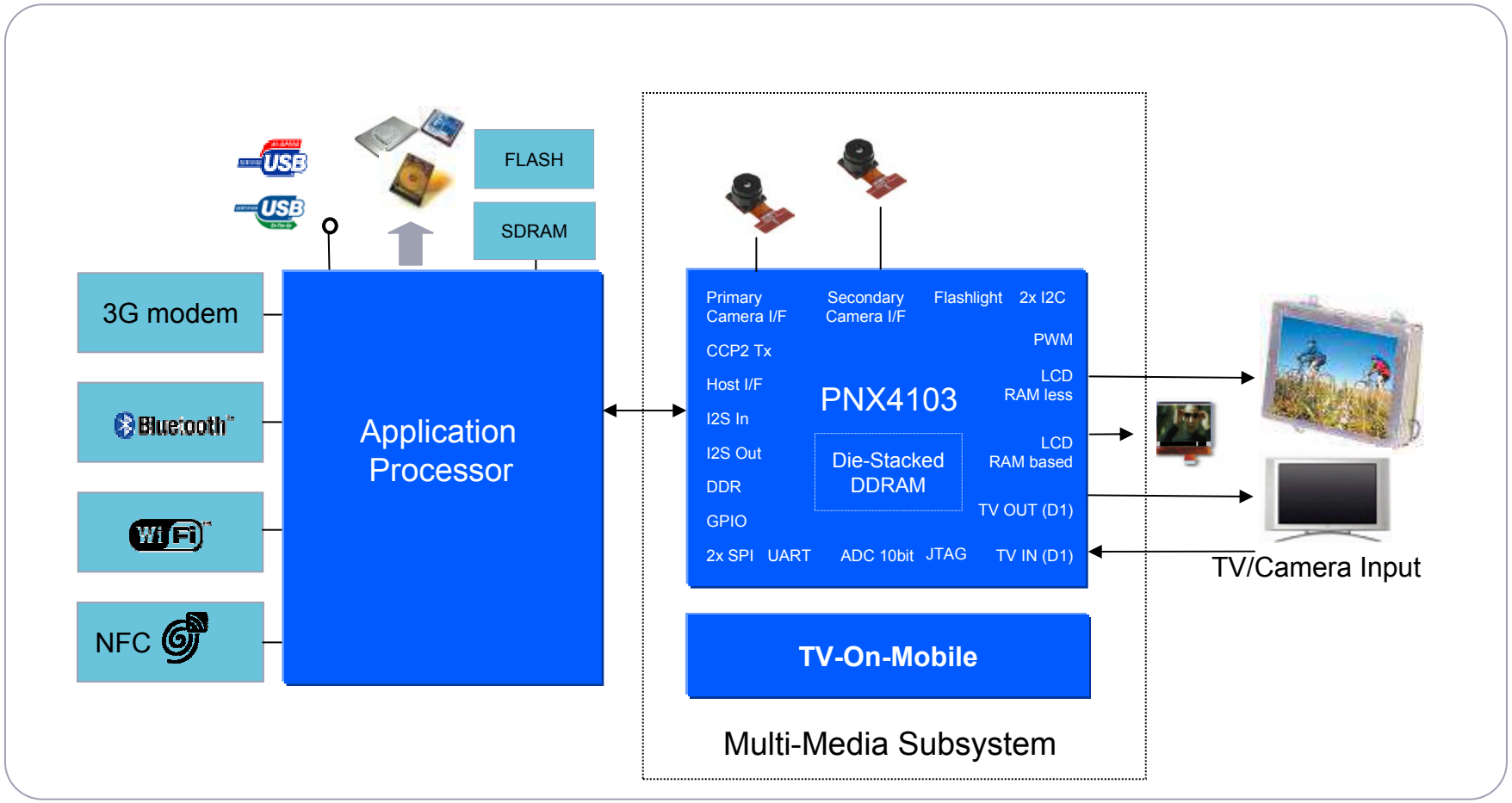
Requirements For the Future Mobile Phones

- Building a Mobile Phone of tomorrow is like shrinking the entire entertainment system of a Living Room, Car Infotainment system and Digital Camera altogether

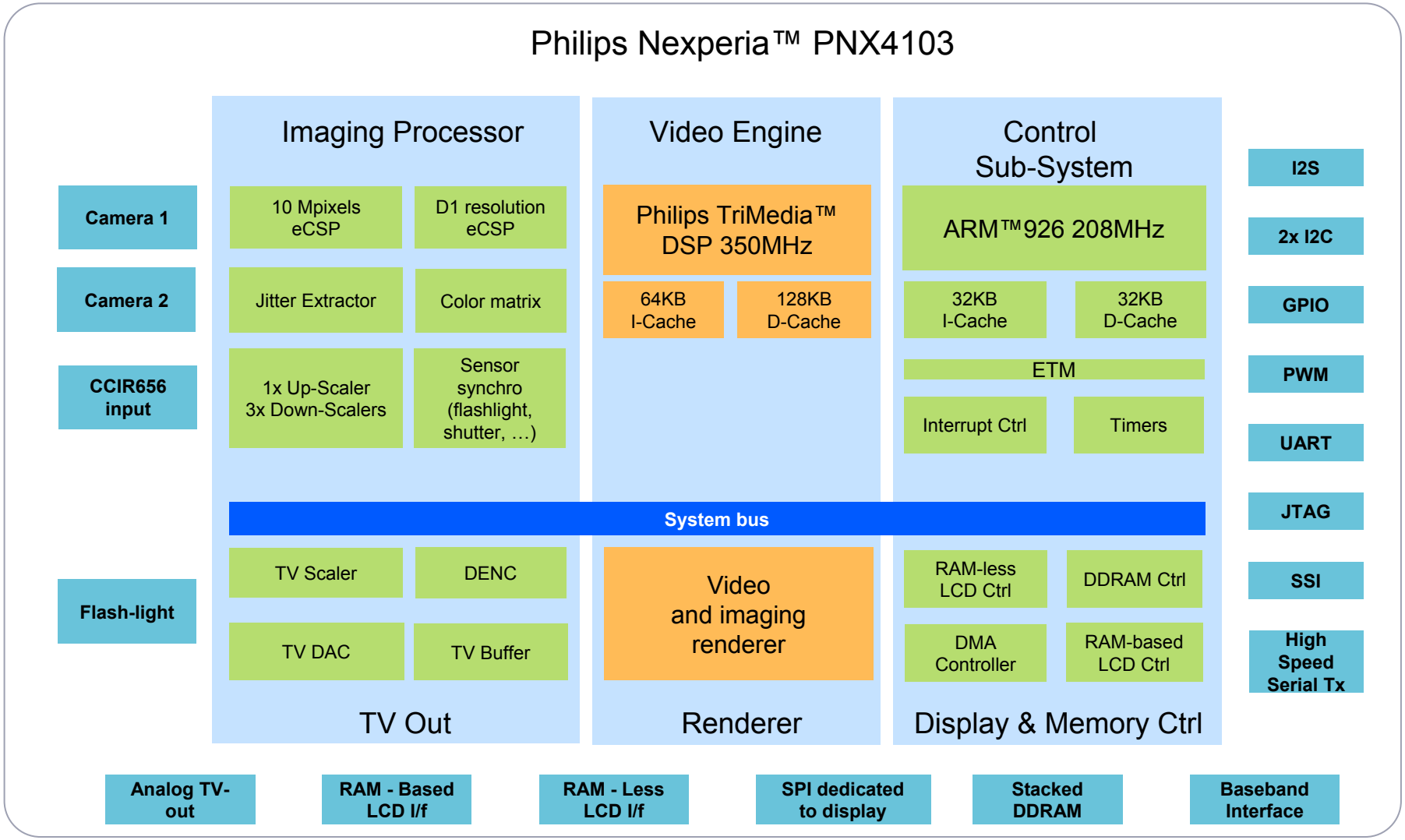
Additional functionality with the same, plain, old mobile phone battery

System Architecture of a Mobile Phone

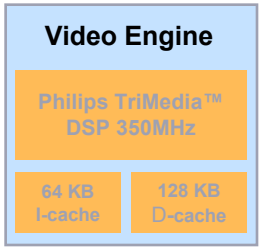
PNX4103 is addressing the Multi-Media part of a Mobile Phone



Philips Nexperia™ Mobile Multimedia Processor



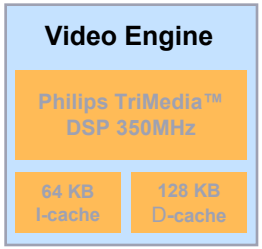
Video Engine
Media Processor TM3270



- Design Goals:
  - Multi-purpose programmable solution
    - Standard video/audio (en/de)-coders like
      - H.264 *standard definition* encode or decode
      - MPEG2, WMV *high definition* decode
    - Proprietary video enhancement processing to improve picture quality
    - Many applications evolve after HW designs complete
      - Programmable solution => Fast time-to-market
      - Easy to program in standard C/C++
  - Multi-market (stationary and mobile devices)
    - Share development costs (CPU, software and tools development)
    - Suitable for low power (battery operated products) and slow memories

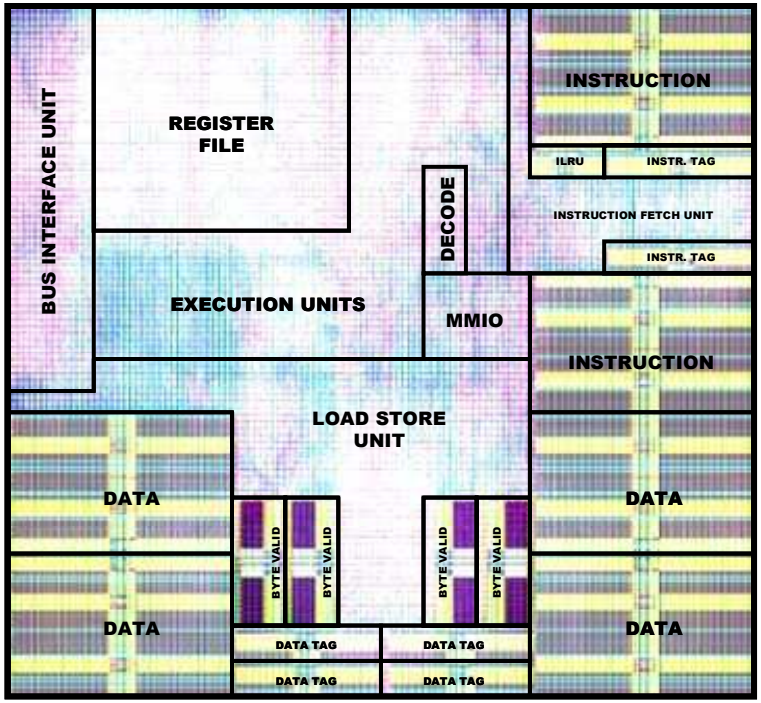
Enough Programmable Performance @ Acceptable Power Consumption within Smallest Possible Silicon Area

Video Engine
TM3270 Main Characteristics



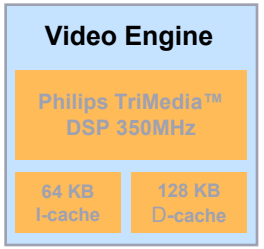
- Fully synthesizable design (450/350 MHz)
- VLIW machine with 5 issue slots
- 32-bit address range, 32-bit datapath
- Operations are guarded
- Unified 128x32-bit register-file
- 35 execution units
- SIMD multimedia and IEEE754 FP operation support
- 64 Kbyte instruction cache (8-way set associative)
- 128 Kbyte data cache (4-way set associative)
- Variable length instruction enco
- Pipeline depth 7-12 stages

```
if r34      fadd        r12 r14   -> r56,
if r24      fmul        r3  r89   -> r112,
            add         r34 r76   -> r121,
            std32d(4)   r42 r48,
if r21      ld32d(-8)   r93       -> r45;
```



TM3270 (8.08 mm^2)

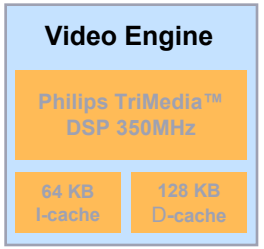
Video Engine
TM3270 Architecture Highlights

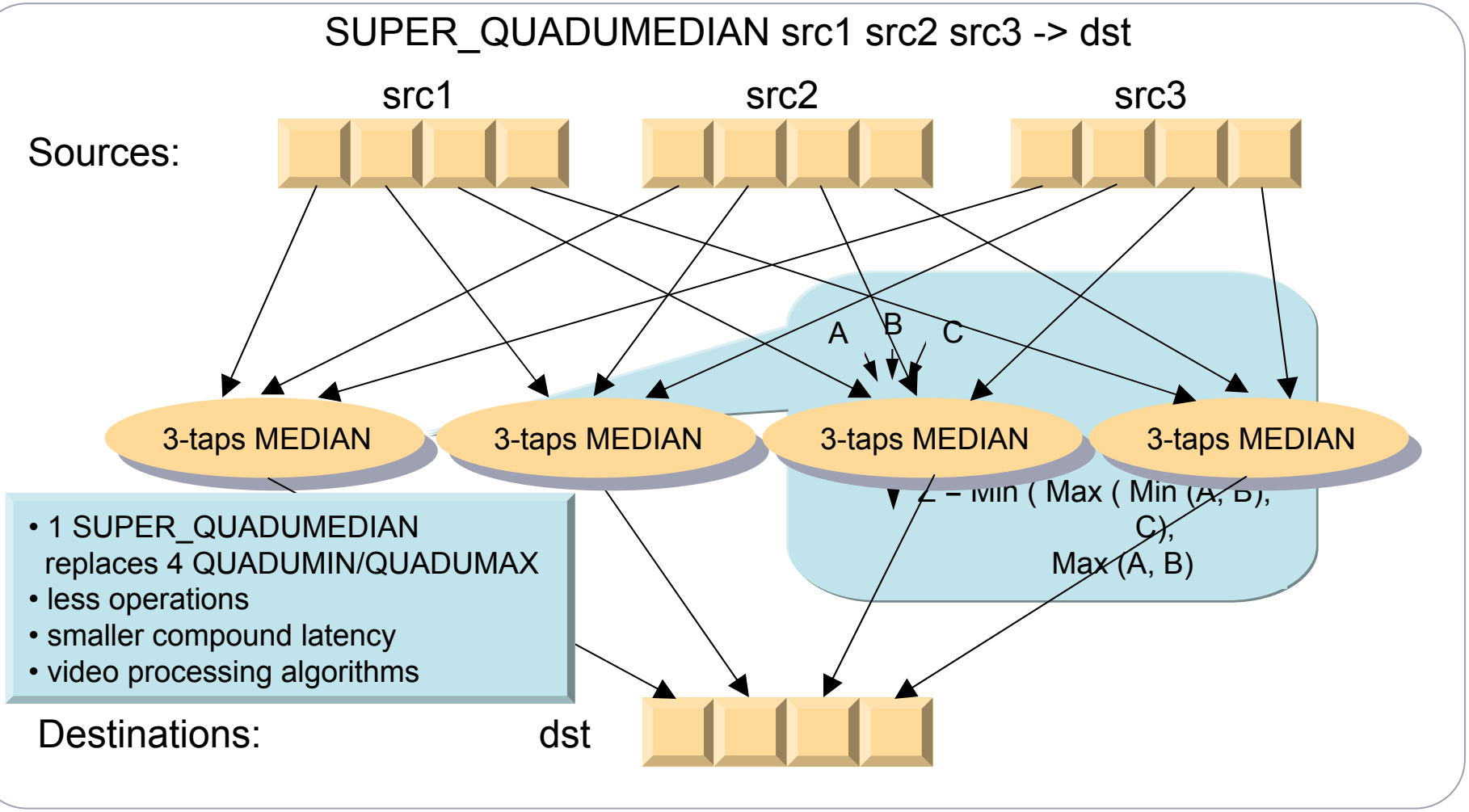


Essential improvements in order to meet the design goals:

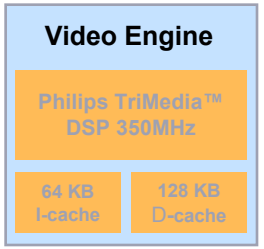
- Instruction Set Extensions
  - Two-slot operations
  - Fractional Load operations – Loads with on-the-fly filtering
  - H.264 CABAC (Context Adaptive Binary Arithmetic Coding) decoding operations
- Data cache / Prefetching
  - Pre-fetching “to hide” SDRAM latency in SoC environment
  - Pre-fetching based on “memory regions”
  - Memory regions are under software control
  - Non-aligned accesses
  - Allocate-on-write-miss policy
  - Selected cache size with the “right” system balance between area and performance
- Extensive usage of clock gating (170 domains in total)

Video Engine
Example of a two-slot Operation





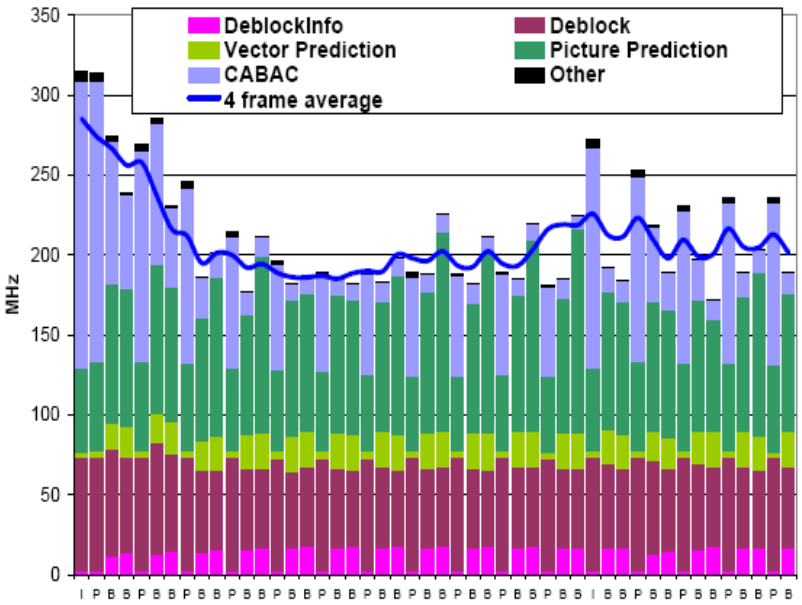
Video Engine
CABAC Operations – H.264 Decoder Profile



- SUPER_CABAC_CTX
  - CABAC Decode, Calculate new context info
  - Input:
    - value, range, state, mps, bit_position, data
  - Output:
    - value, range, state, mps

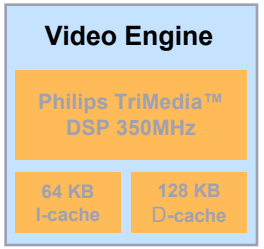
- SUPER_CABAC_STR
  - CABAC Decode, Calculate new stream info
  - Input:
    - value, range, state, mps, bit_position
  - Output:
    - bit_position, bit

- Performance speedup in CABAC processing: factor 1.5 – 1.7

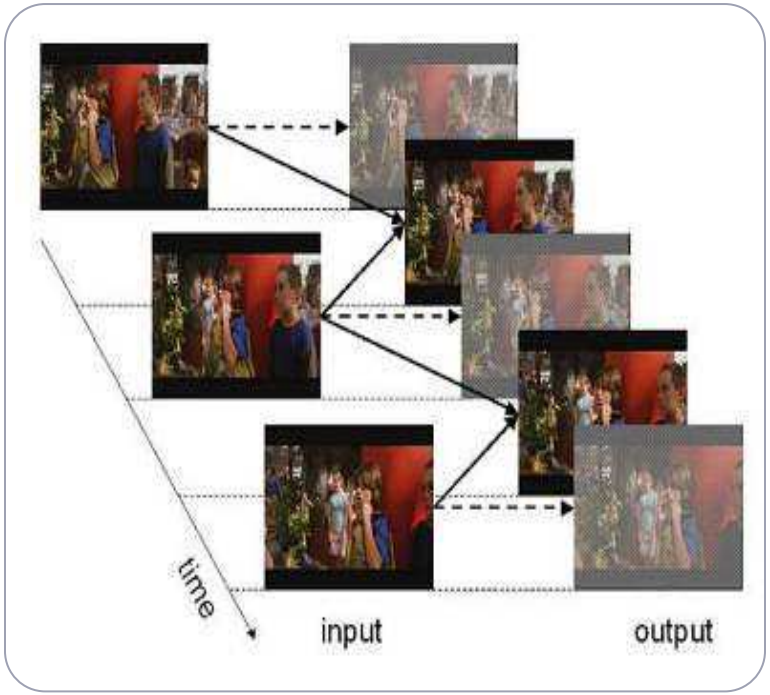


- *H.264 CABAC 2.5 Mbits/s encoded bit-stream*
- *720*576 resolution @ 25 frames/s*
- *80% of 16x16 blocks decomposed into sixteen 4x4 blocks*

Video Engine
Video Improvement Algorithms



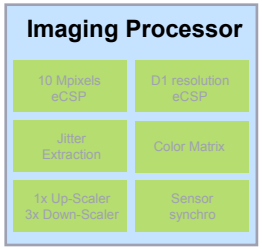
- TM3270 Architecture is also optimized for video improvement algorithms
- Lower bit-rate video streams (low resolution or frame rate) leave more TriMedia cycles for improvement algorithms and can be displayed at comparable video quality

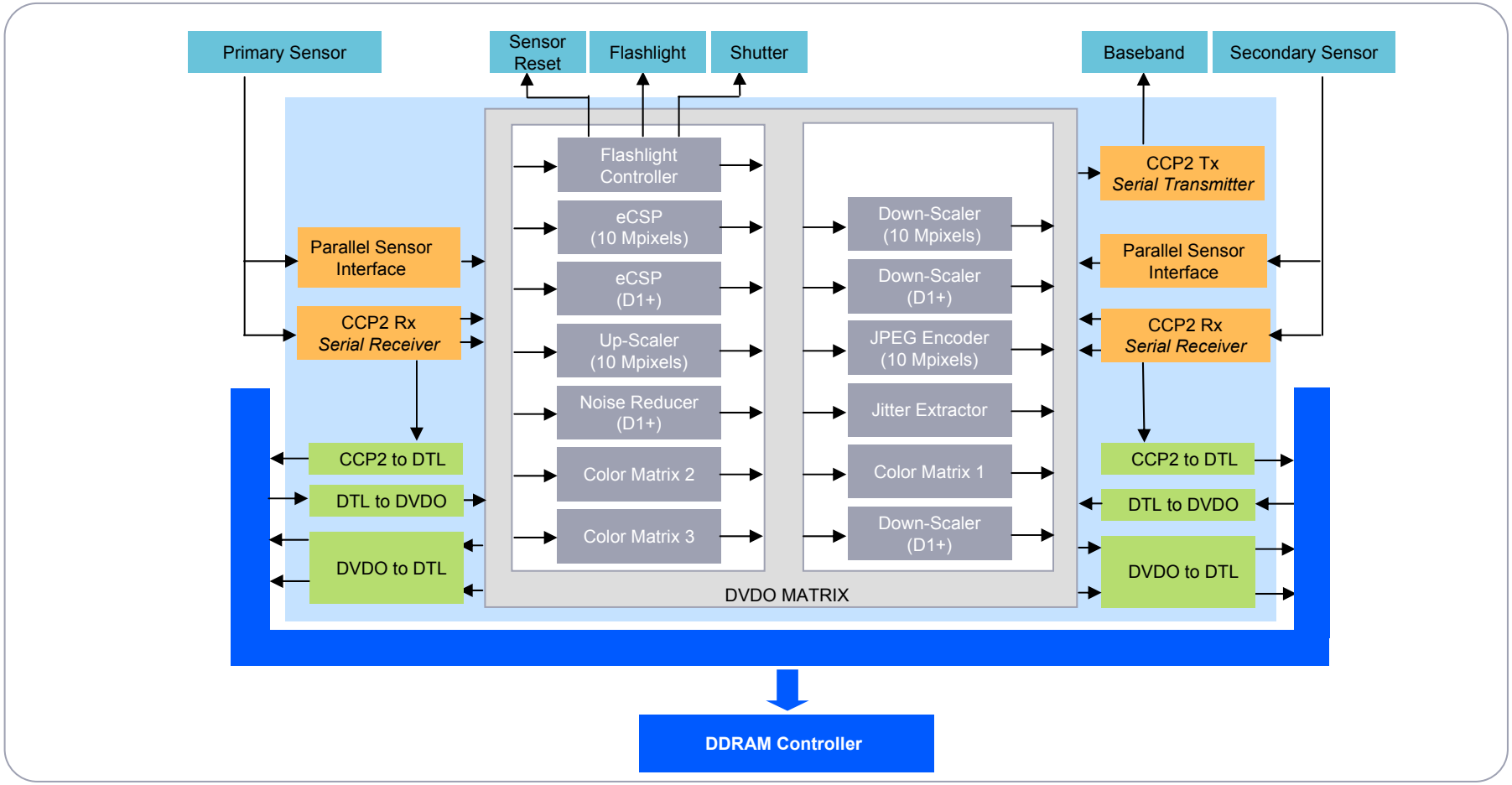


Mobile Natural Motion

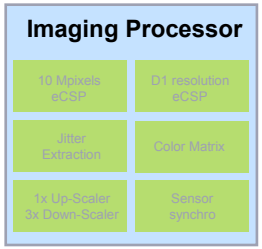
- Improves video playback quality
- Complete software solution
  - Motion Estimation
  - Motion-Compensated Temporal Up Conversion of Chroma and Luma
- Takes less than 10% of TM3270 cycles on PNX4103

Imaging Processor
Block Diagram





Imaging Processor
Main Characteristics



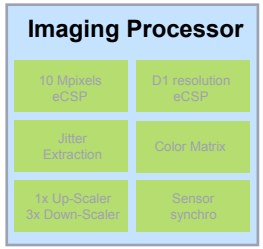
- Scalable streaming architecture
  - Central “switch” called DVDO Matrix acts as a MUX with clock-domain crossing
  - Processing blocks simply connect to the matrix
  - Processing chain is constructed by programming matrix
  - Independent clock frequencies (clock-domain crossing in matrix)
- Two simultaneous camera inputs
  - High and low resolution cameras
  - Internal parallel video pipes are possible
- Down-scalers work in streaming mode - reduce power
- Parallel and serial (sub-LVDS) camera interfaces

Power management framework
PNX4103 Low Power Design

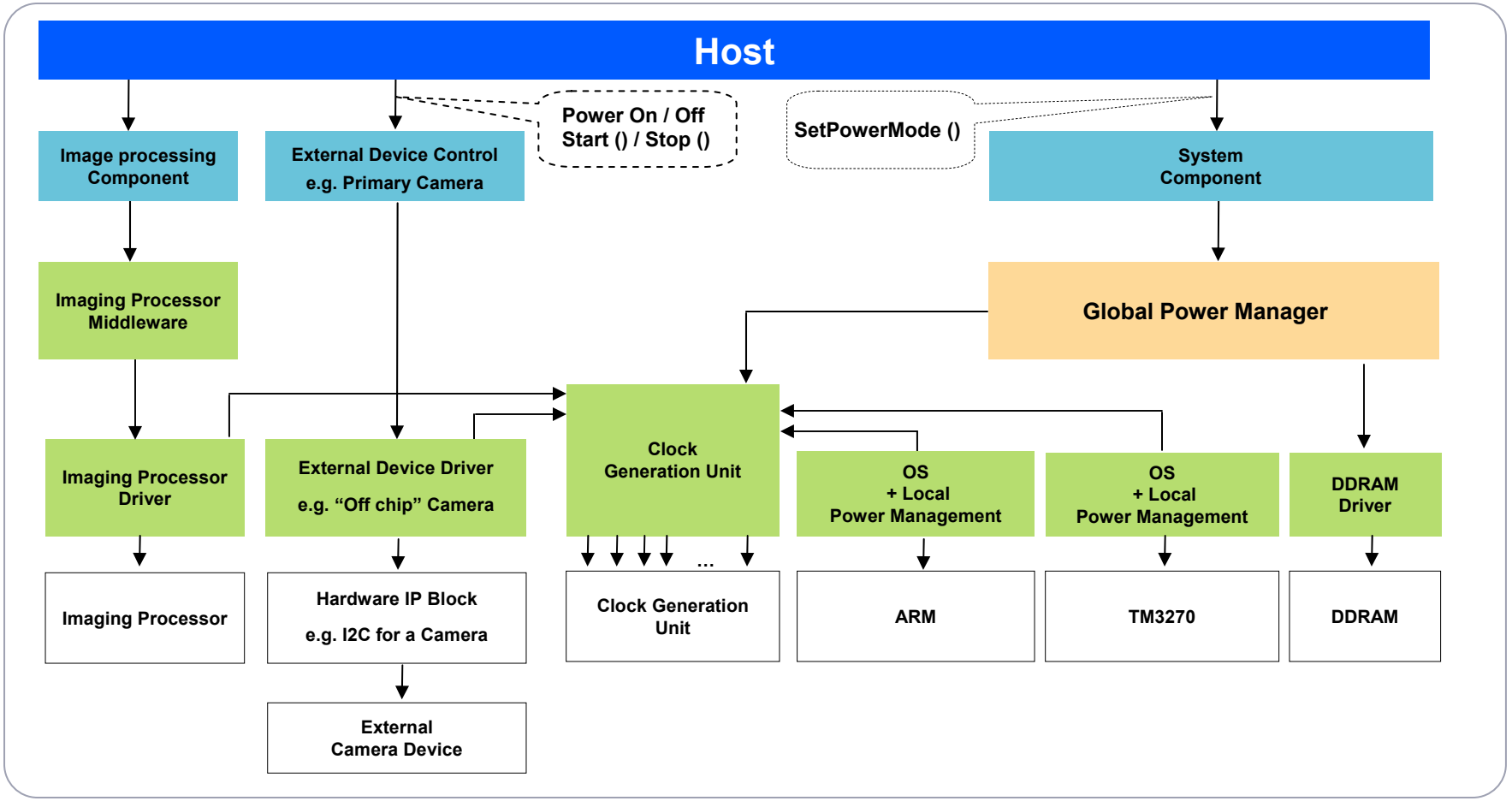
- General principles
  - Most logic designed using High-Vt transistors for low leakage
  - Central Clock Generation Unit (CGU) with over 100 independently controllable clocks
    - Independent clock domains allowing fine frequency control (switching and scaling) on the individual clocks
  - Auto-clock gating in many blocks
  - Two power down modes for TM3270
    - self-induced partial power-down and external-induced full power-down
  - Dynamic Voltage scaling for TM3270
- Control of leakage
  - TriMedia is 100% implemented in Standard-Vt transistors
    - High performance
    - High(er) leakage
  - Separate power supply (voltage domain) for TriMedia removes leakage when TriMedia is not needed

Power management framework

Software Aspects



Power-management incorporated into software driver framework



PNX4103 Silicon Characteristics

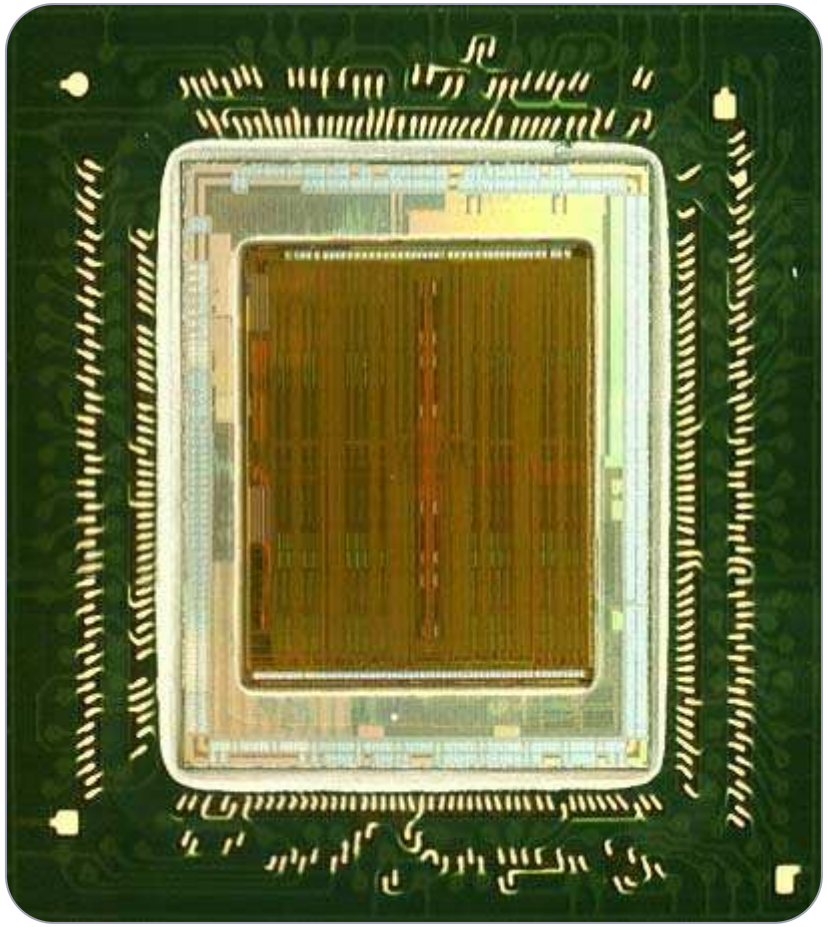
- Process
  - Low power 90nm
  - Operating voltage 1.2V
- Package
  - 10 x 10 mm LFBGA256
- Typical Power Consumption
  - TriMedia 1.0 mW/MHz
  - ARM 0.6 mW/MHz

PNX4103

PNX4103 Silicon Characteristics

Die-Stacked Memories

- The package contains a 128Mbit die-stacked LP-DDR
- The power consumption minimized due to limited off chip communication
- Reduced size of the overall system solution



Conclusions

- PNX4103 is following Philips Platform approach based on a Dual Core Architecture that was deployed already in TV and STB
- Low Power implementation of the TriMedia DSP enables the home entertainment quality multimedia on mobile devices
- Programmable design offers system upgradeability and flexibility in designing next generation consumer products
- Imaging Processor for High Quality Video Recording and Still Images
  – no need for additional camera in your pocket ☺
- Small form factor due to die-stacked memories
- Designed as a co-processor allowing an easy upgrade path for enhanced imaging and video capabilities on mobile phones

Quiz – answers!!!

- Would you use your mobile phone as the only camera at your Daughter's wedding ?

  ✓ YES

- Would you use your mobile phone to download a movie, connect to your new HD TV with Dolby-Digital 5.1 and invite your friends over?

  ✓YES

- Would you use your mobile phone to record the World Cup Finals?

  ✓ YES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