PHILIPS

PNX8535 hybrid television processor

Philips Semiconductors

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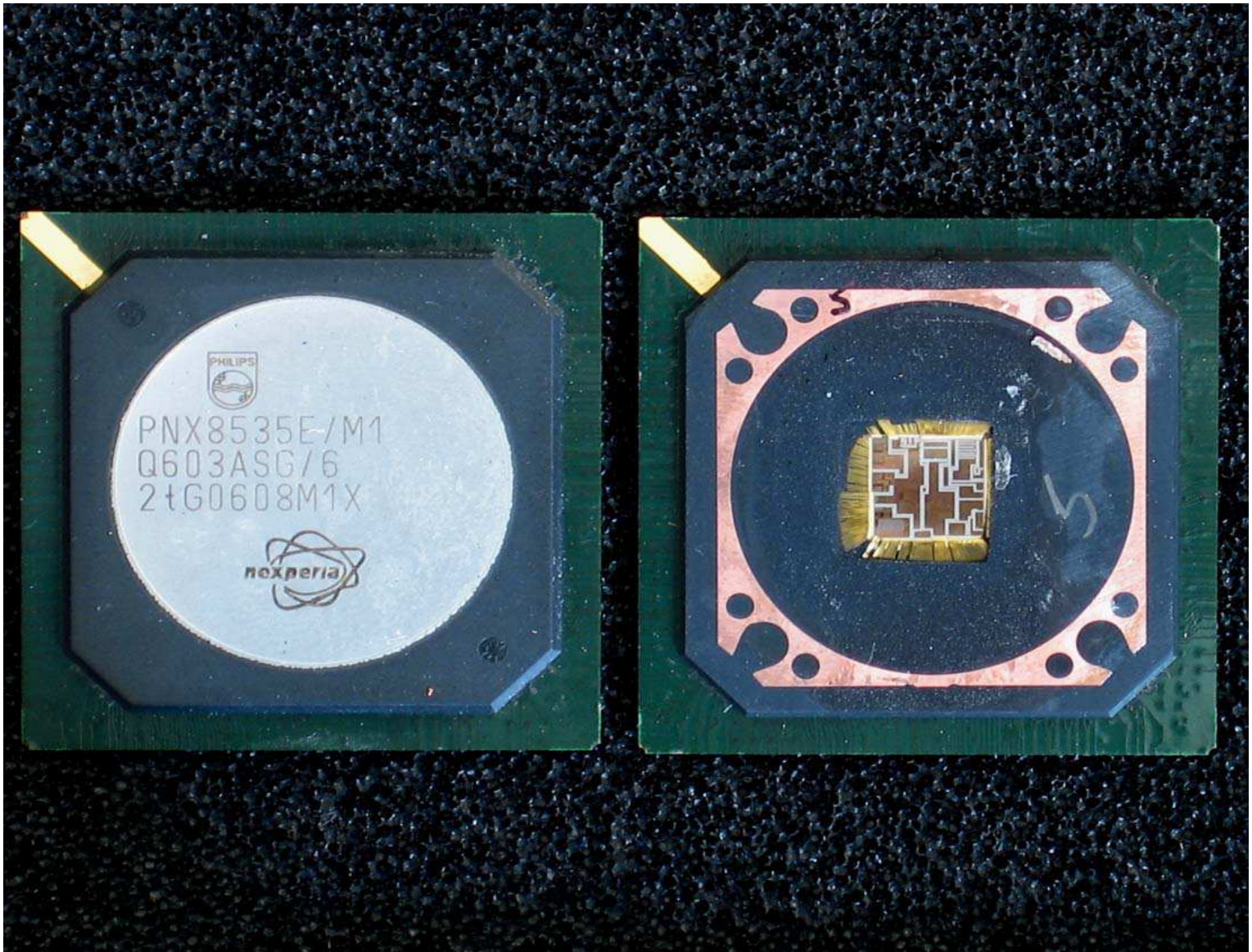
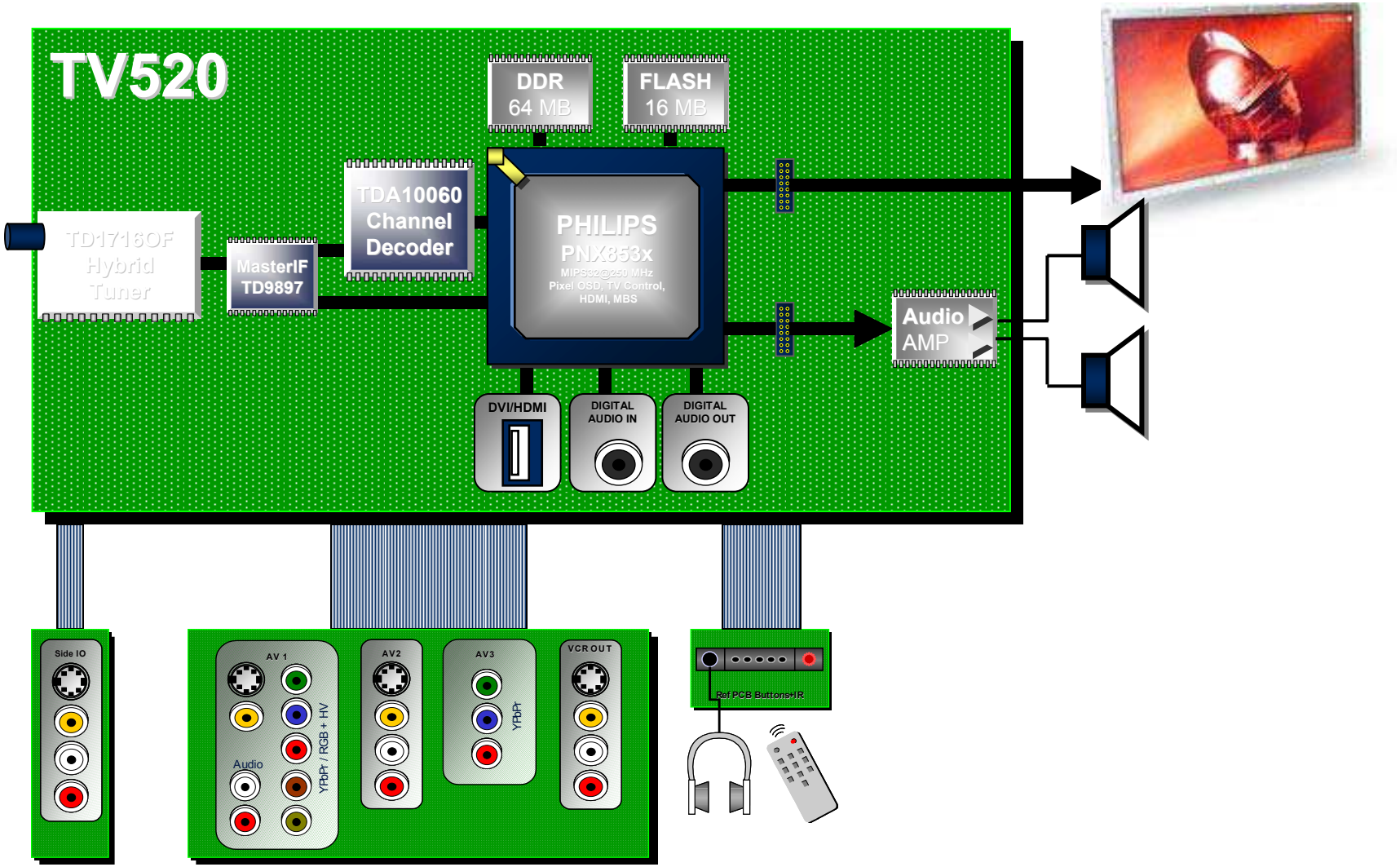
Agenda

- The PNX8535, first pictures
- Application background
- PNX8535 functions and use cases
- PNX8535 device design
- Physical characteristics and key data
- Software support and tools

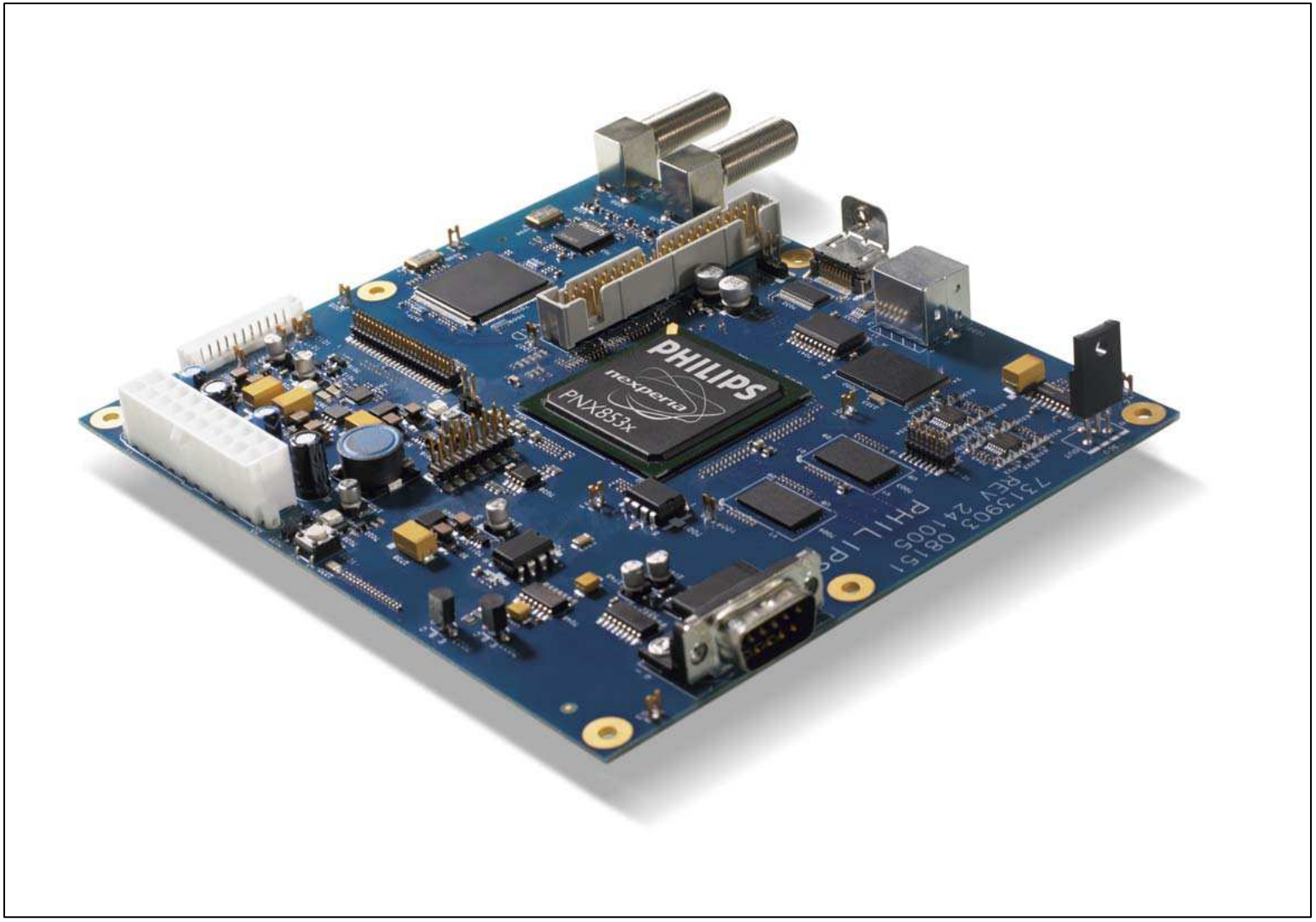
PNX8535, first silicon



Application background, integrated hybrid TV



Application background, integrated hybrid TV



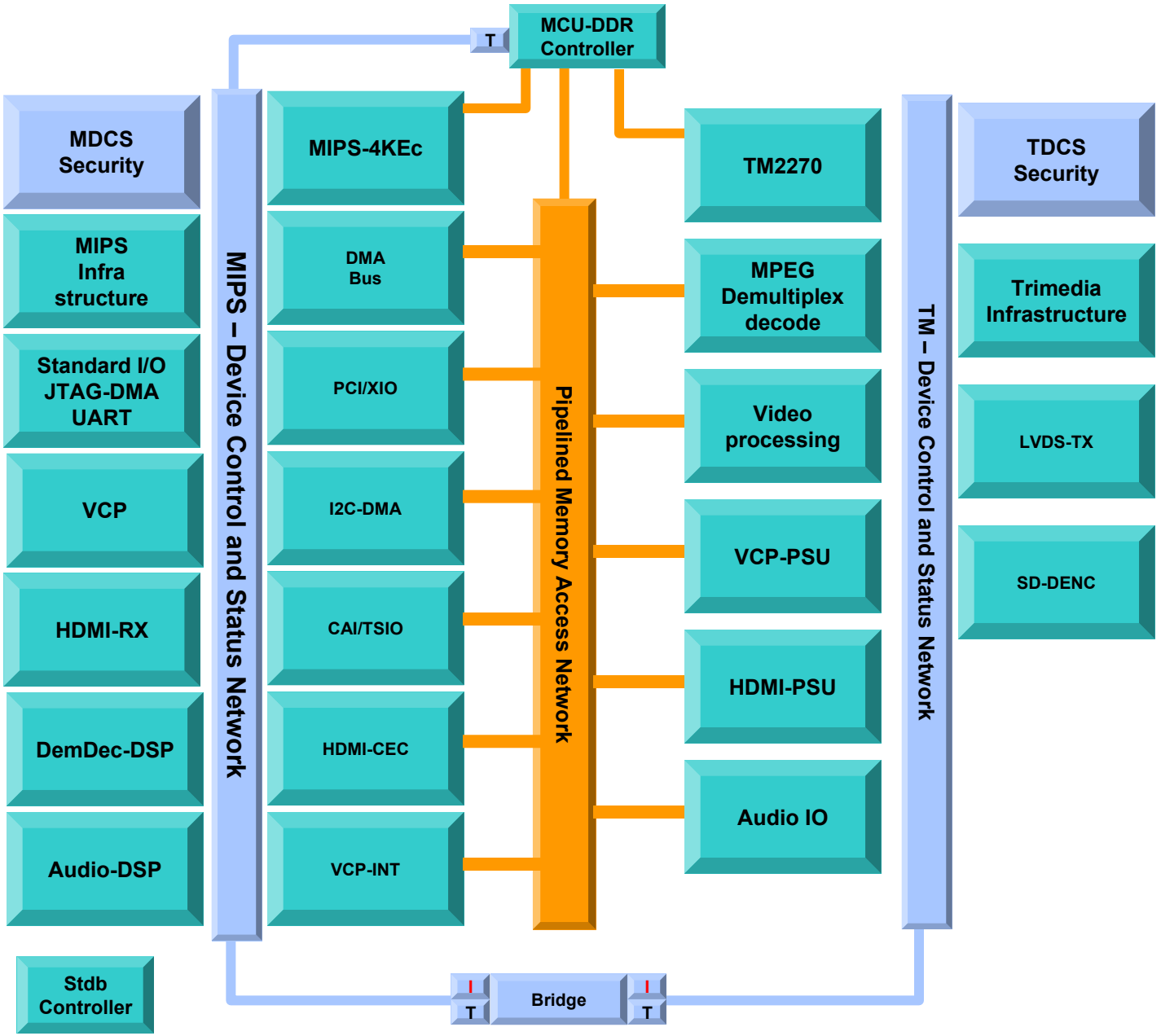
PNX8535 functions and use cases

- Hybrid matrix television, for the ATSC/DVB market
  - Analogue and Digital broadcast reception and decoding
  - Conditional access (CableCard/CI)
  - A/V connectivity like:
    - Cinch/scart connections
    - HDMI/DVI input
    - VGA/DVI PC-inputs
  - Audio processing (volume, bass, virtualisation, Dolby SRS, etc.)
  - Video processing (de-interlacing, scaling, colour features, sharpening)

PNX8535 functions and use cases

- Output
  - Support for panels up to 1366*768@60p
  - Monitor/VCR output
  - Four stereo audio output DAC's
  - Digital audio input/output (SPDIF)

- Use cases
  - HD/SD Analogue video/audio Input
  - HD/SD MPEG audio/video input/decode
  - HD/SD Digital video/audio input (HDMI)
  - PC Analogue Input
  - PC Digital Input via DVI/HDMI
  - FM radio


MCU-DDR Controller
T
MDCS Security
MIPS Infra structure
Standard I/O JTAG-DMA UART
VCP
HDMI-RX
DemDec-DSP
Audio-DSP
MIPS – Device Control and Status Network
MIPS-4KEc
DMA Bus
PCI/XIO
I2C-DMA
CAI/TSIO
HDMI-CEC
VCP-INT
Pipelined Memory Access Network
TM2270
MPEG Demultiplex decode
Video processing
VCP-PSU
HDMI-PSU
Audio IO
TM – Device Control and Status Network
TDCS Security
Trimedia Infrastructure
LVDS-TX
SD-DENC
Stdb Controller
I
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Bridge
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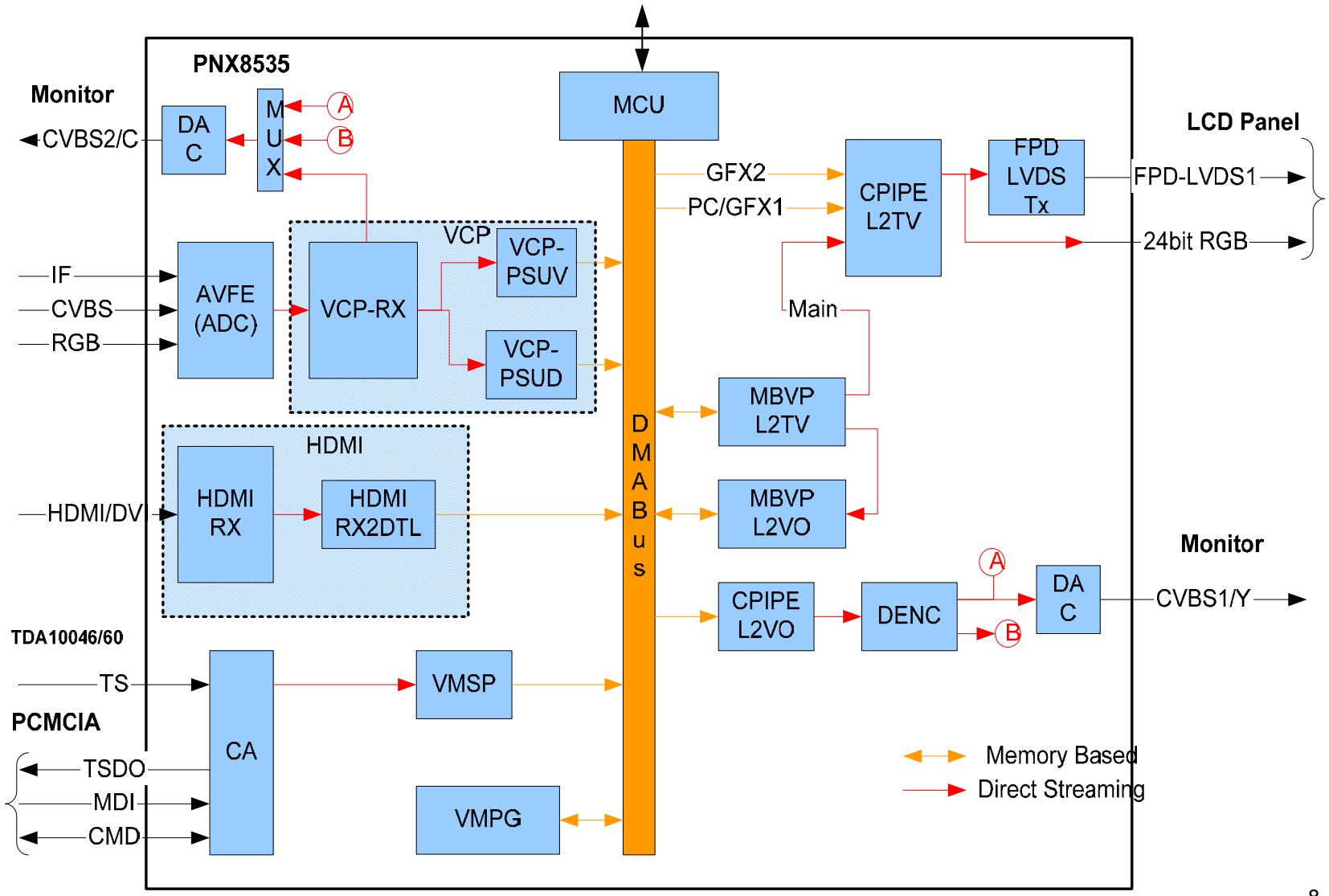
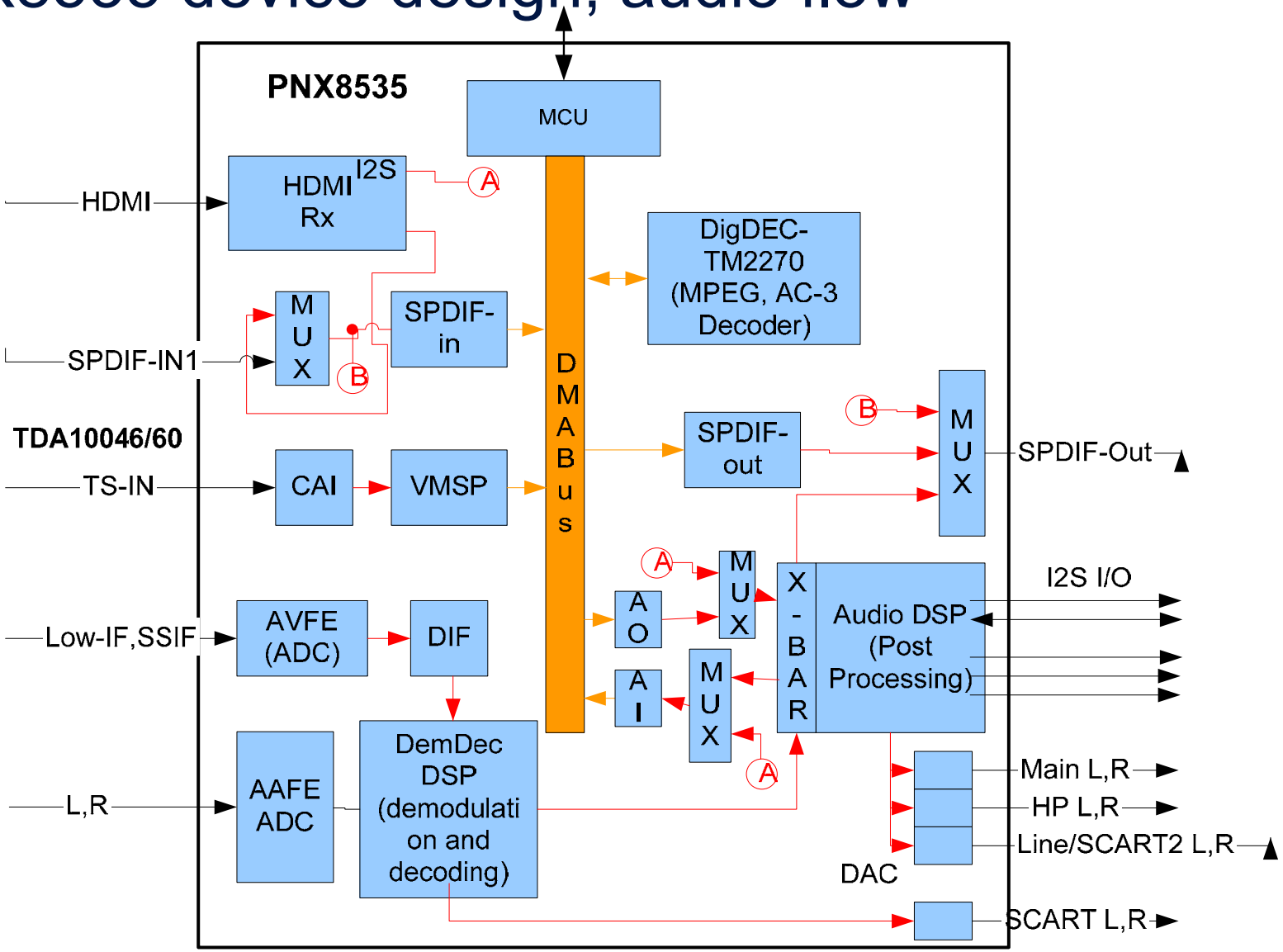
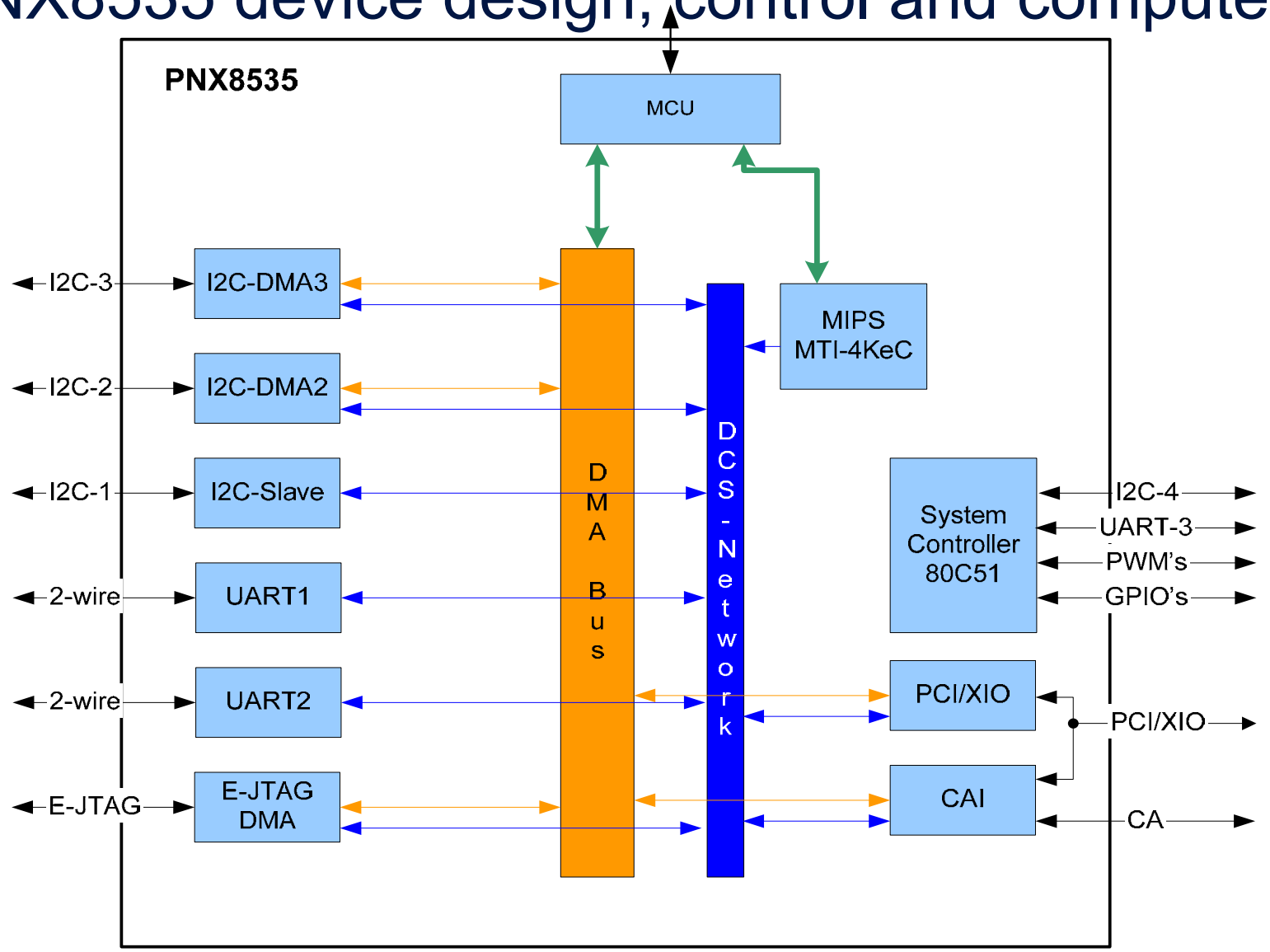
PNX8535 device design, video flow



PNX8535 device design, audio flow



PNX8535 device design, control and compute



PNX8535 device design, MIPS – 4KEc core

- MTI Core 4KEc
  - MIPS32 Instruction set (release2), with MIPS 16e code compression
- Cache
  - 16KB Instruction
  - 8KB Data
  - 32 Byte line size
- CPU Pipeline
  - 5 Stage (Fetch, Execute, Multi/Divide, ALU, Write)
- Memory Protection
  - 32 entry joint TLB with 1KB page size
- Frequency
  - 240MHz (Worst Case)

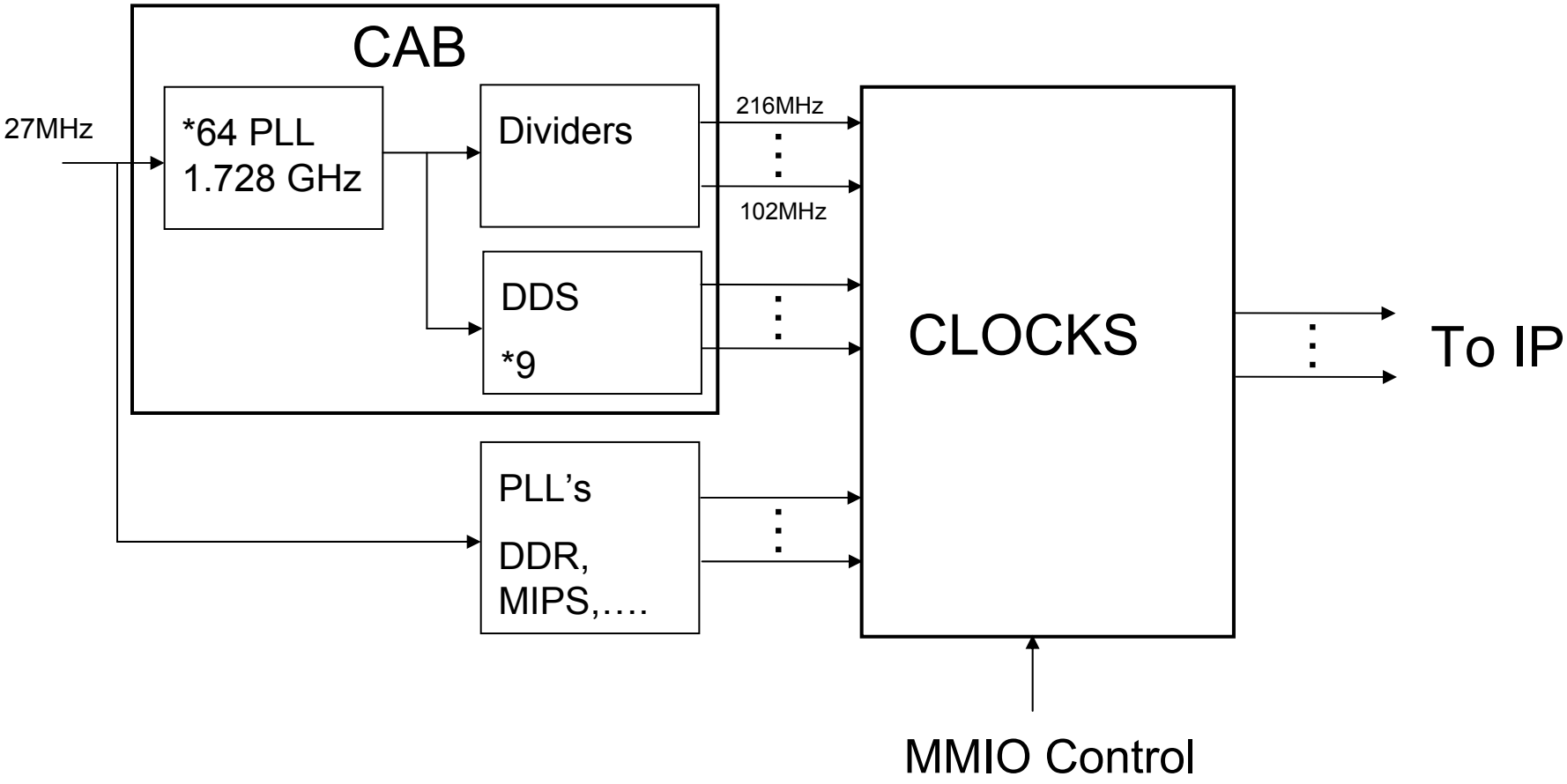
PNX8535 device design, TriMedia – TM2270

- TM2270 core
  - TriMedia DSPCPU32 Level 3 Architecture
- Cache
  - 32KB Instruction, 128 Byte line size
  - 16KB Data, 64 Byte line size
- Pipeline
  - 5 Stage pipeline
  - 29 Functional units: Integer and Floating point ALU+DSP
- Frequency
  - 300MHz (Worst Case)
- Debug Support
  - Data and Code Breakpoints

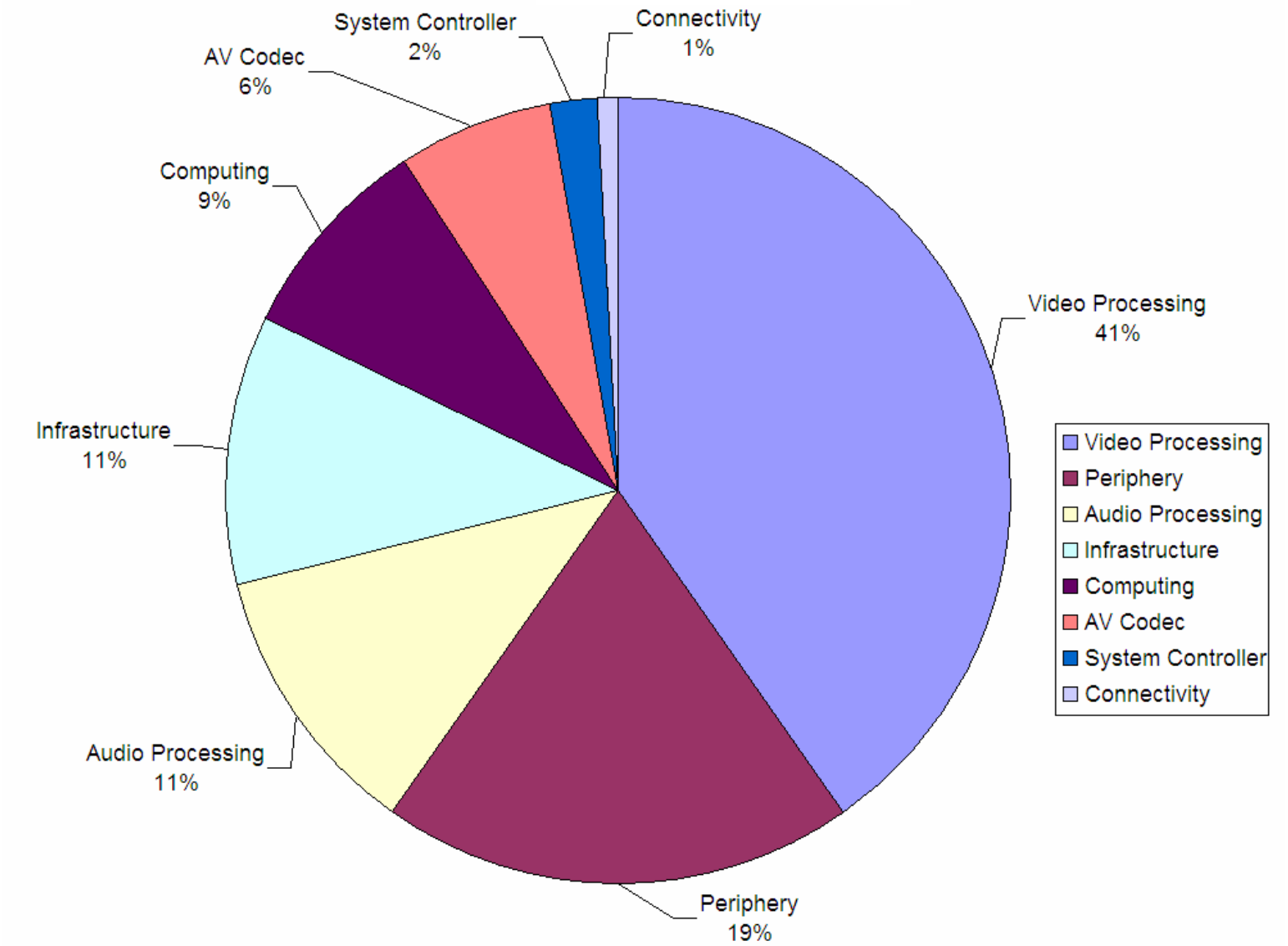
PNX8535 device design, clock source

- External 27MHz Xtal
  - Used for Standby Controller
  - All clocks are division of 27MHz
  - Used for AVC System
    - Clocks are divided from 64*27MHz=1.728GHz PLL
      - General clocks for IP e.g. UART, I2C, DCS,..
    - Clocks are generated from Direct Digital Synthesis
      - Fine adjustment fro Audio/Video Streams
    - Clocks are multiplied by dedicated PLL
      - LVDS, DDR, MIPS

PNX8535 device design, clock architecture



PNX8535 device functional split in area



PNX8535 physical characteristics- die

Process : CMOS090HLV

Masks : 34 (6 layer metal)

Transistors : ~40 Million

Power : 3-3.5Watts

Analogue/Decap : 20% of Core

Memory : 25% of Core

Logic : 55% of Core

Power Domains : 3.3V, 2.5V, 1.2V

Clocks Domains : 75

Wire diameter : 25um

Bondpad Opening : 50x70um

Pad Cells : 750

Bond Fingers : 515

Power Rails : 30

Bond Wires : 704

Package : BBGA 40x40mm

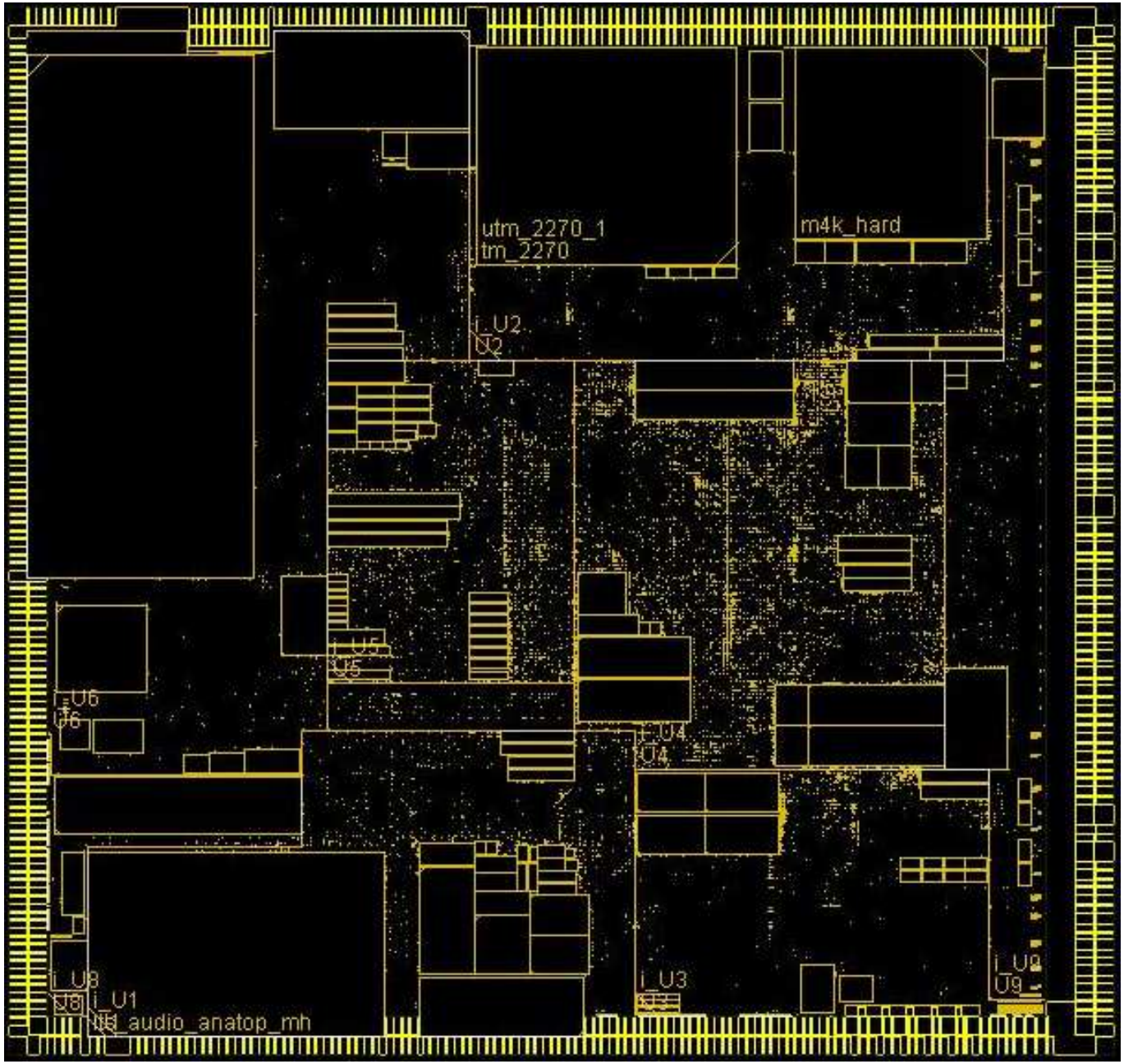
Ball : 596

Signals Balls : 416

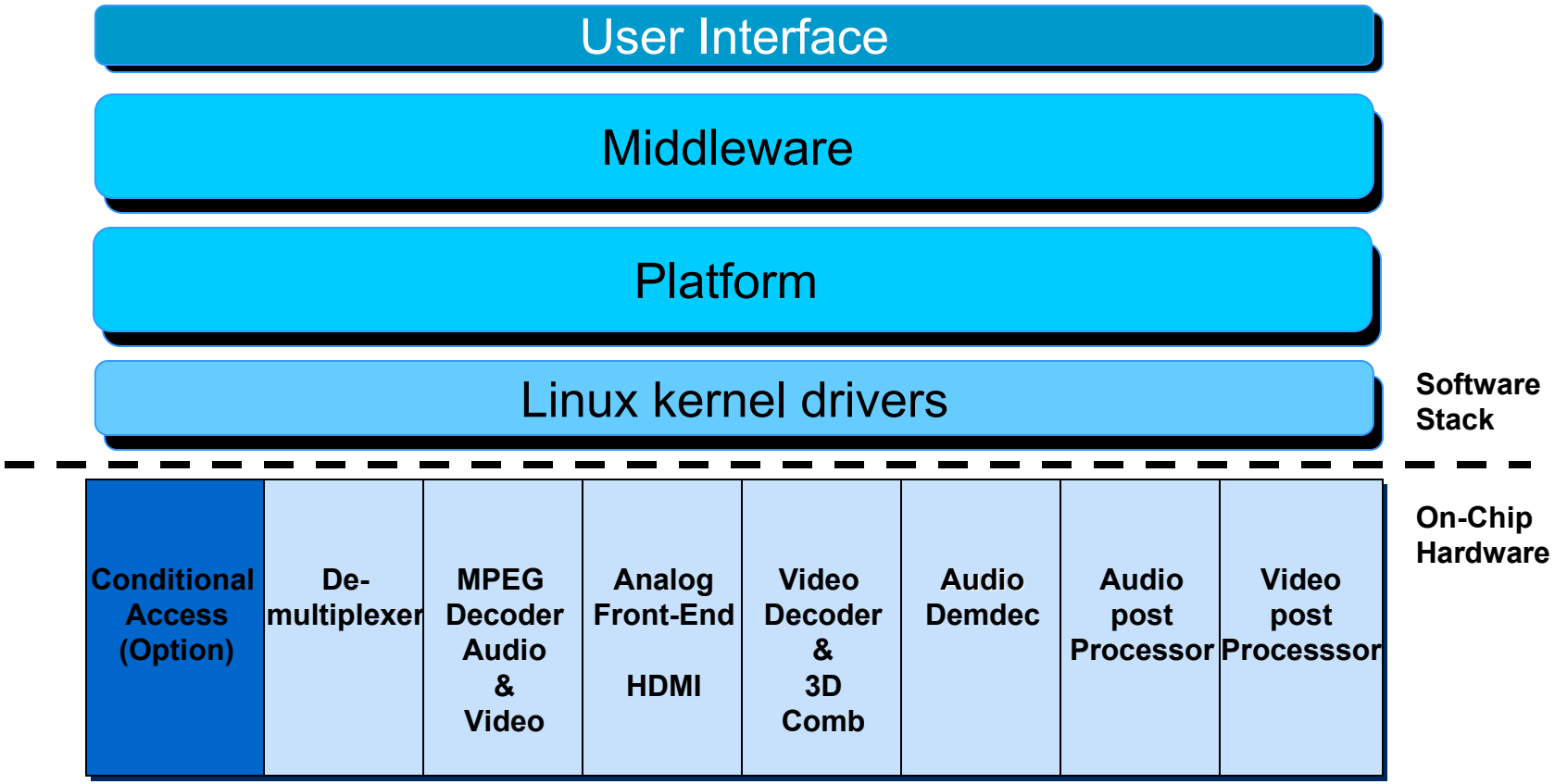
Power Balls : 144

Thermal Balls : 36

Laminate : 4 Layers


utm_2270_1
tm_2270
m4k_hard
i_U2
U2
U5
U6
U4
i_U3
U9
i_U8
U8
i_U1
audio_anatop_mh

Software support



Software support

- Linux drivers
  - Standard drivers for all the different on board hardware peripherals
- Platform
  - Implements hardware independent API for higher levels of software.
  - Provides implementation of automatic behaviour like view modes, muting/blanking
- Middleware/User interfaces
  - Implementation of user functions like channel change.

Summary, conclusions

- PNX8535
  - –Is a highly integrated hybrid television processor.
  - –Combines high performance (high definition) audio/video decoding and processing in a single SOC.
  - –Supports both a general purpose CPU (MIPS) as well as a dedicated media processor (Trimedia).
  - –Combines software and hardware media processing in a single streaming framework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