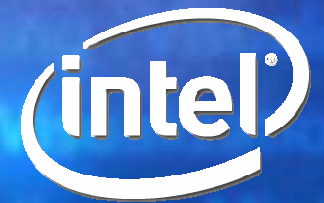


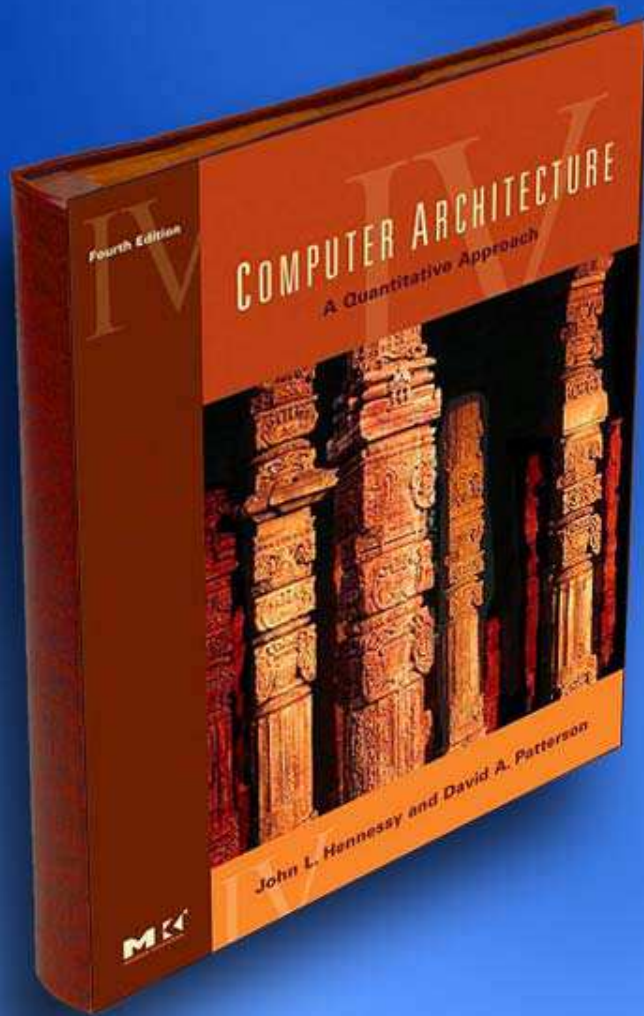
COOL CODES FOR HOT CHIPS: A QUANTITATIVE BASIS FOR MULTI-CORE DESIGN



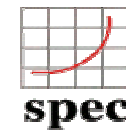
Justin Rattner

Intel Senior Fellow | Chief Technology Officer

Two Decades of Quantitative Design



TPC Transaction Processing
Performance Council



SYSmark® 2004 SE



MobileMark® 2005

3DMARK®06
The Gamers' Benchmark



Multi-Core Transition Accelerating

“We notified customers we’re pulling in both the desktop and server (launch) of the first quad-core processors into the fourth quarter of this year from the first half of 2007”



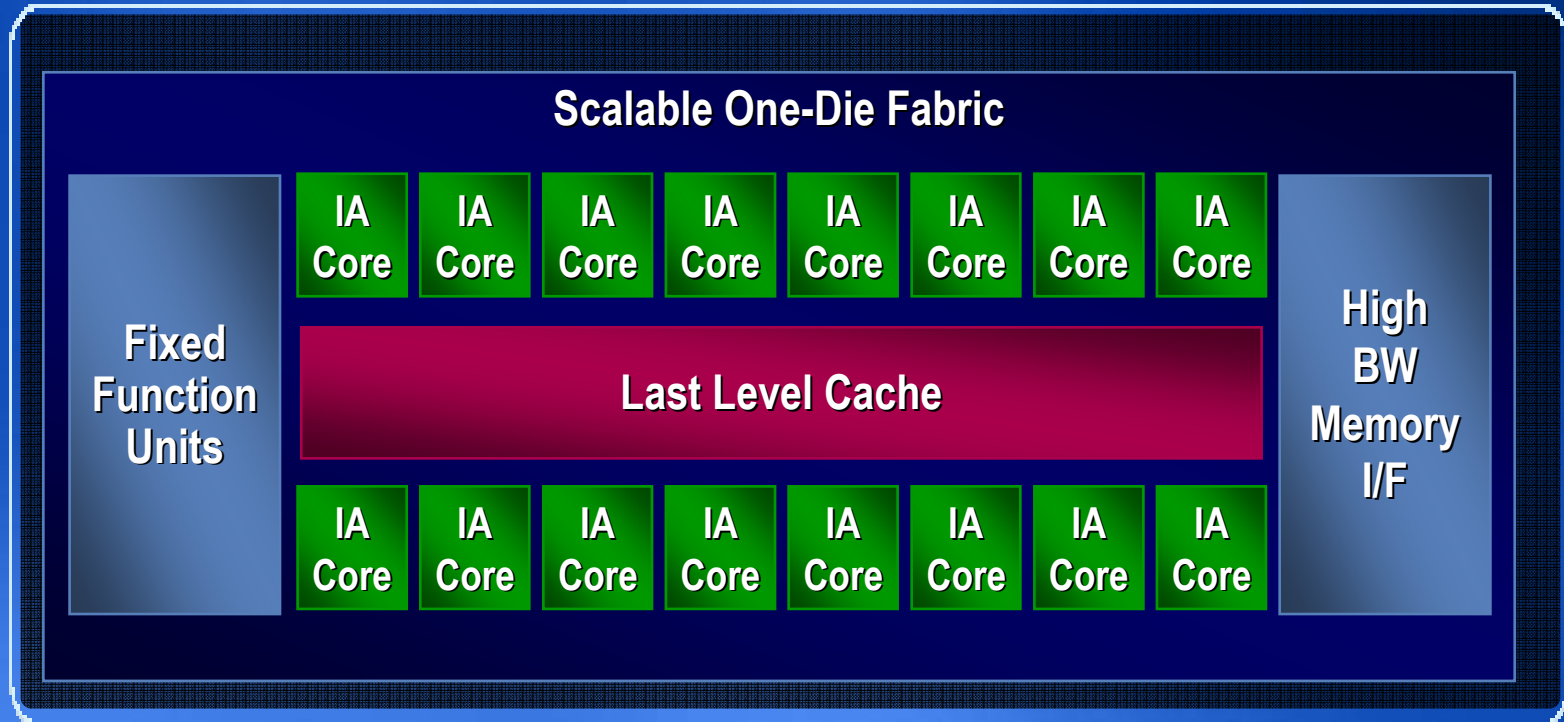
“The UltraSPARC T1 processor with CoolThreads technology is the highest-throughput and most eco-responsible processor ever created.”



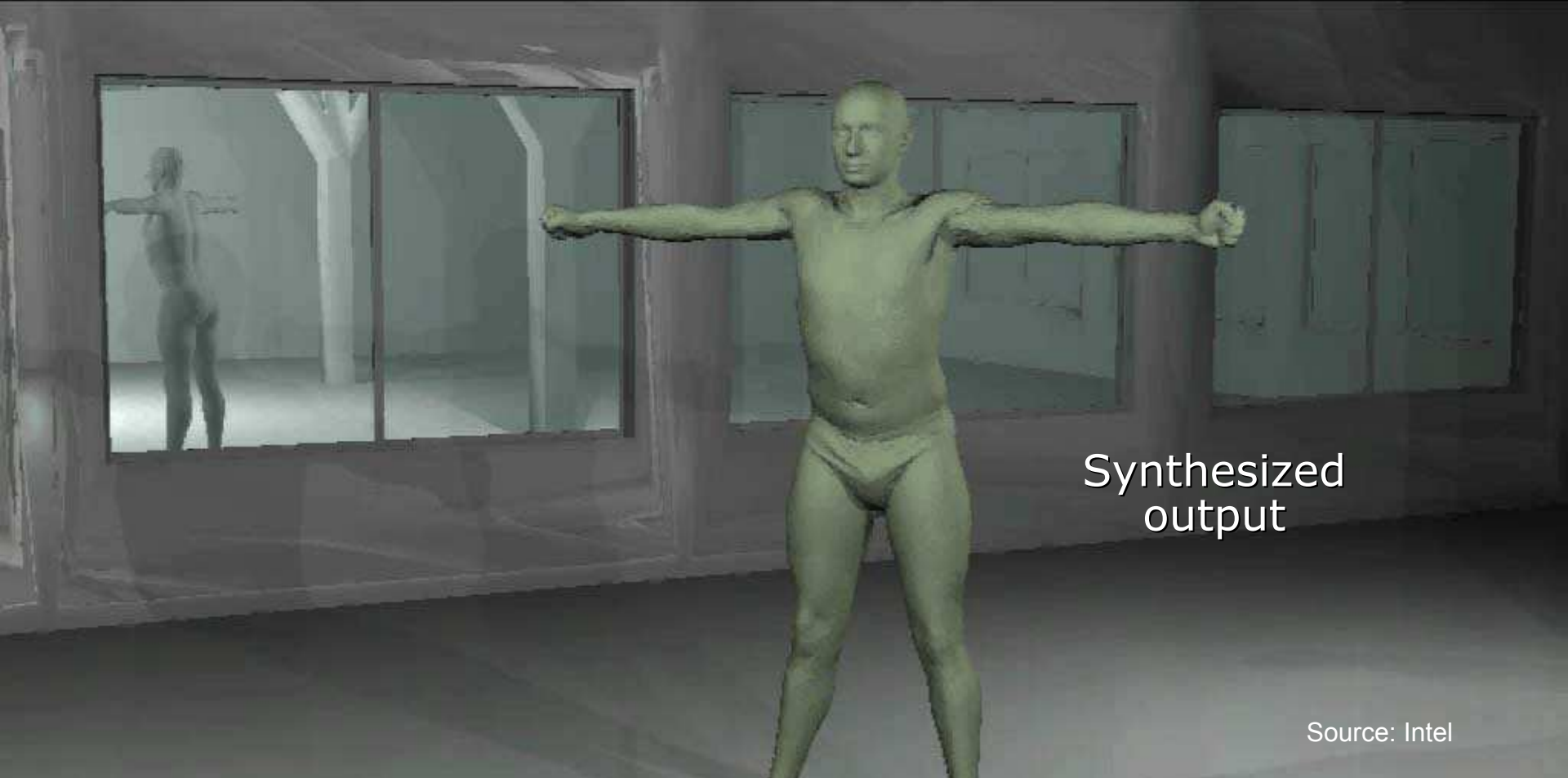
“Azul has been able to pack an industry-leading 24 processor cores on a single-chip, which means that each processor is able to run 24 simultaneous parallel threads”



Tera-Scale Strawman



Opening up new classes of applications



Source: Intel

Camera 1 input

Camera 2 input

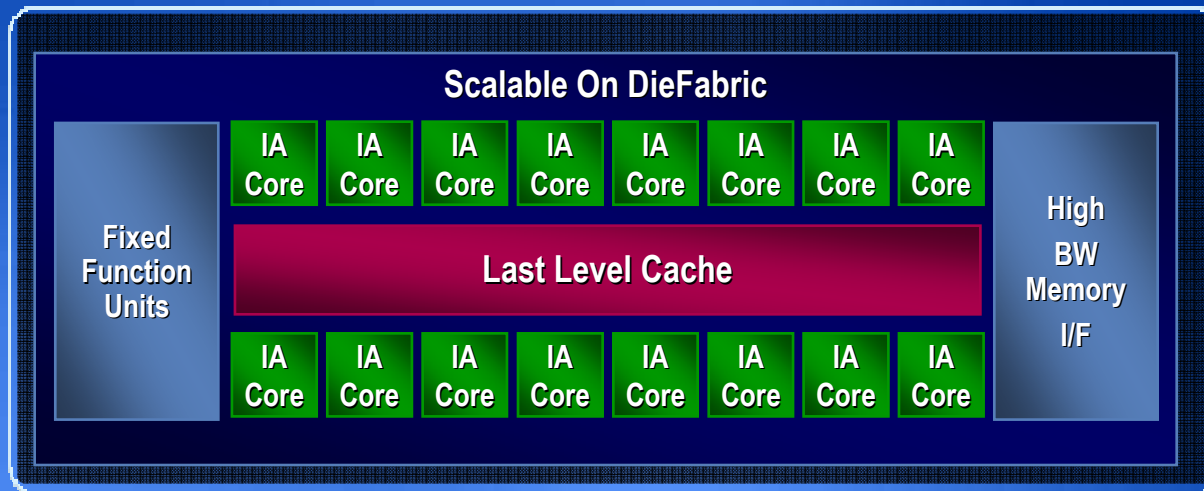
Camera 3 input

Camera 4 input



Design Challenges

- Complex memory hierarchy
- Sophisticated on-die fabrics
- Explicit thread support
- Fixed function acceleration



Lacking The Quantitative Tools...



No Multi-Core Metric?

SPLASH



HPC focused

TPC



Throughput

EEMBC



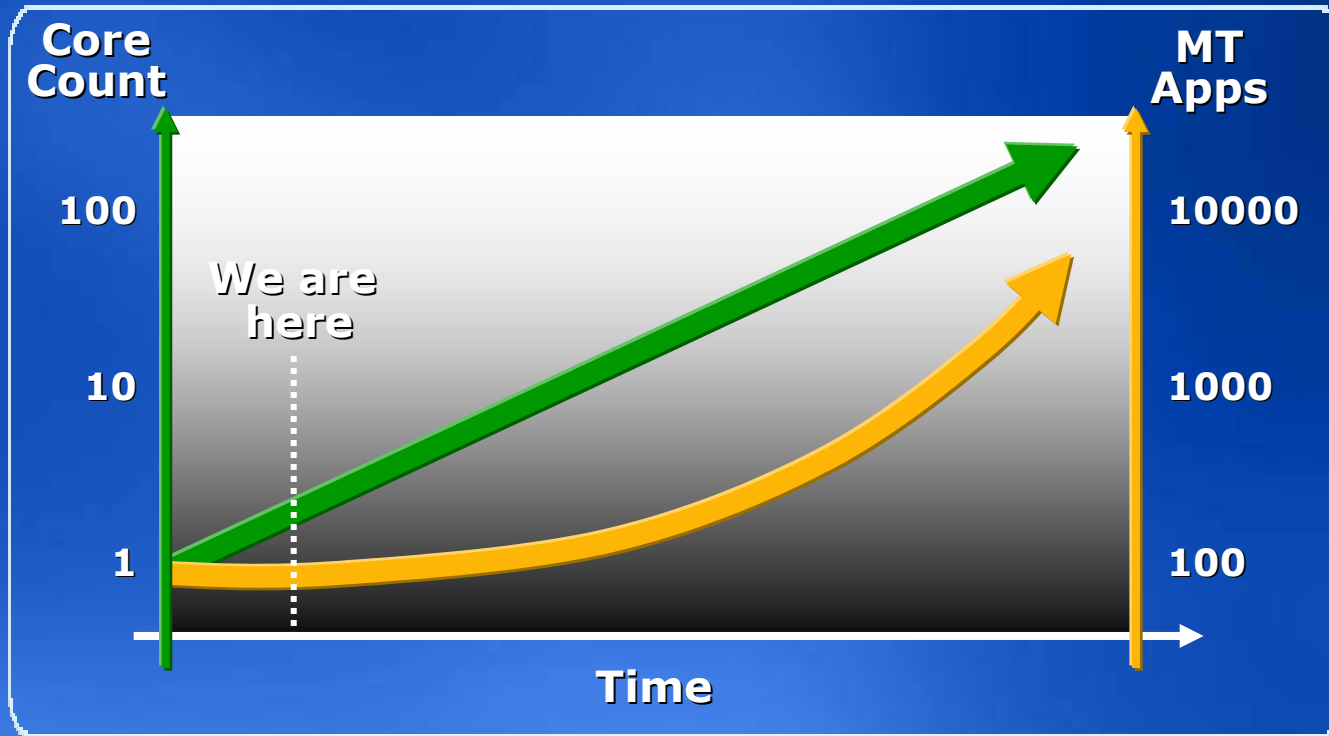
Embedded

3DMark



Single domain

The Waiting Game



Designing **2010** Processors Today

Must **Anticipate** Future **Applications**

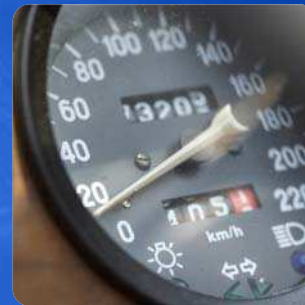


Creating a Multi-Core Benchmark

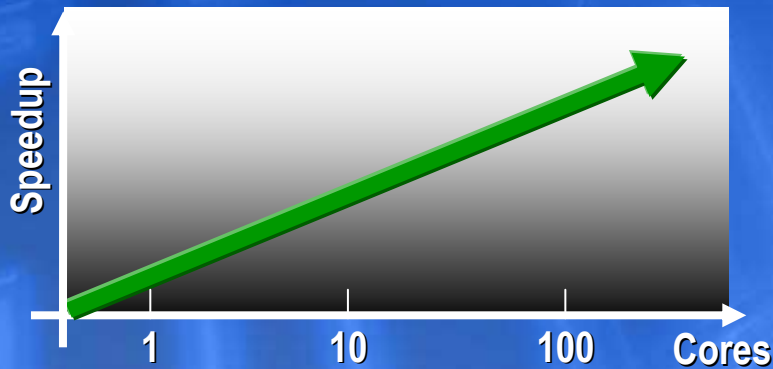
Established & Emerging



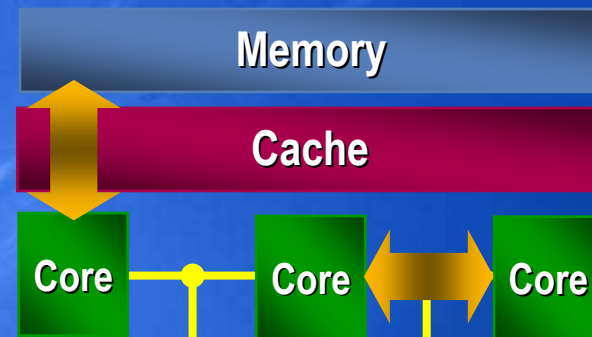
Performance & Energy Aware



Highly Threaded & Scalable



Differentiated and Stressful



Unique Challenges

Do We Target...

Bigger *OR* Smaller Cores

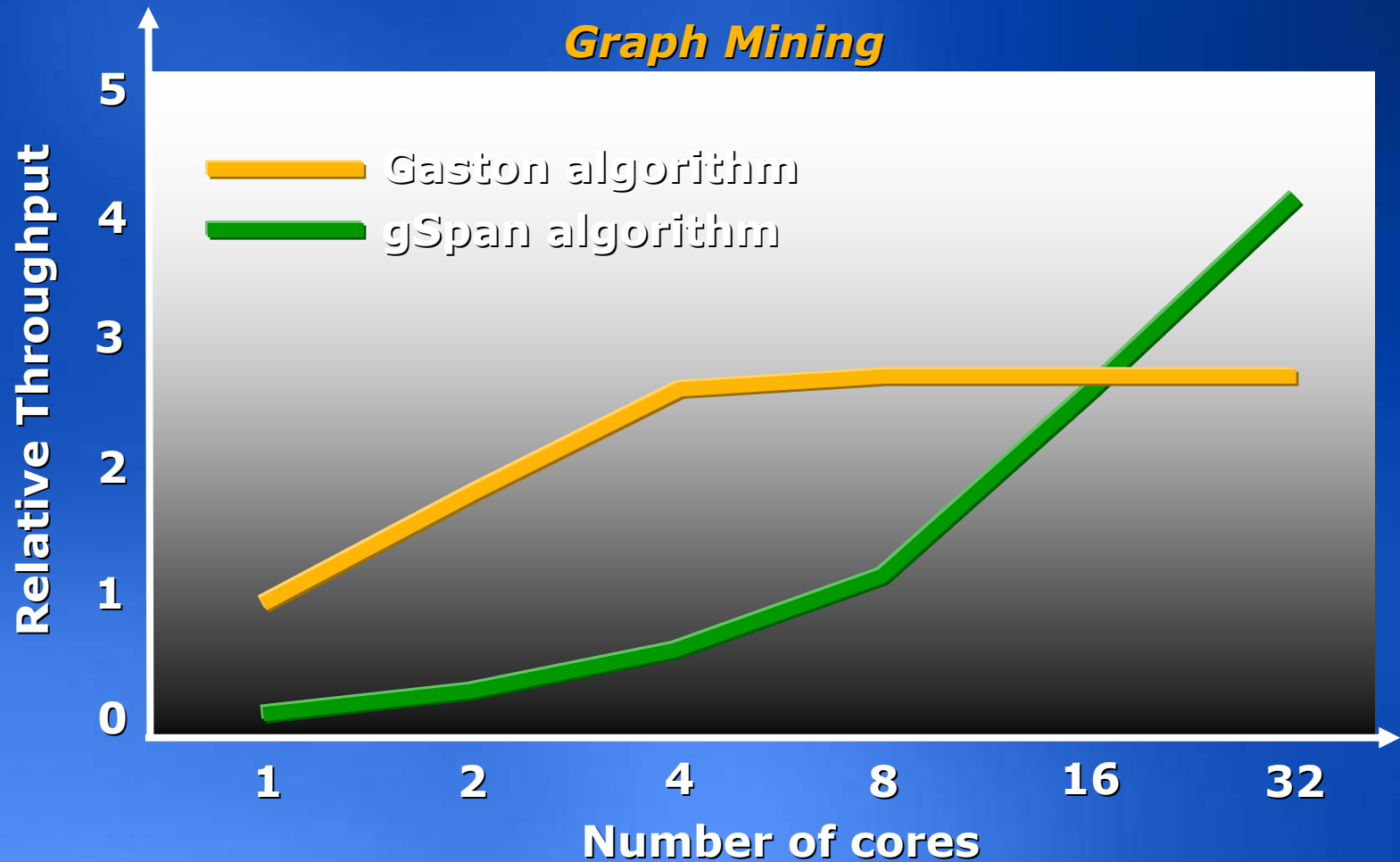
Performance *OR* Scalability

Compute *OR* I/O Intensive

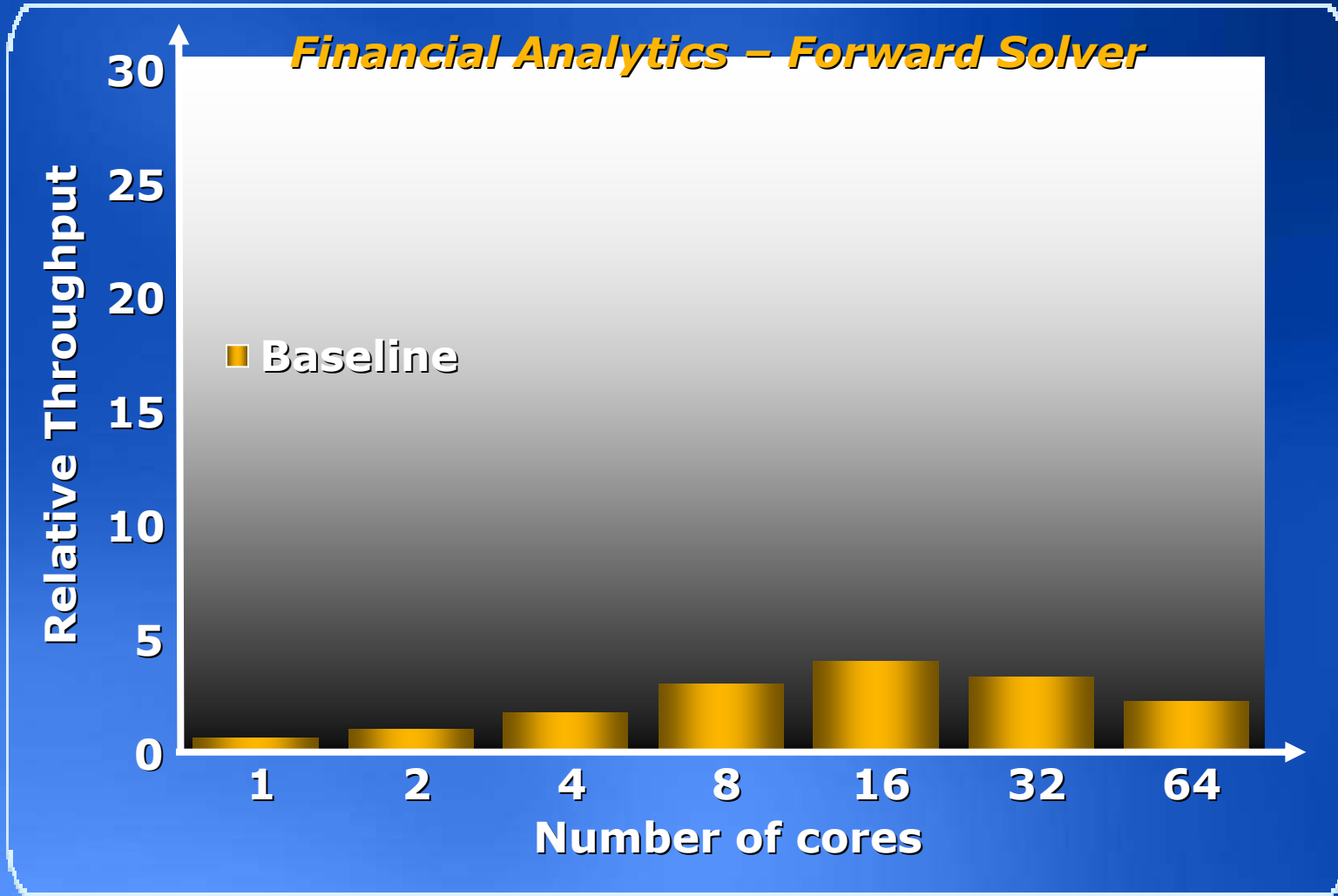
Cache Friendly *OR* Memory Intensive



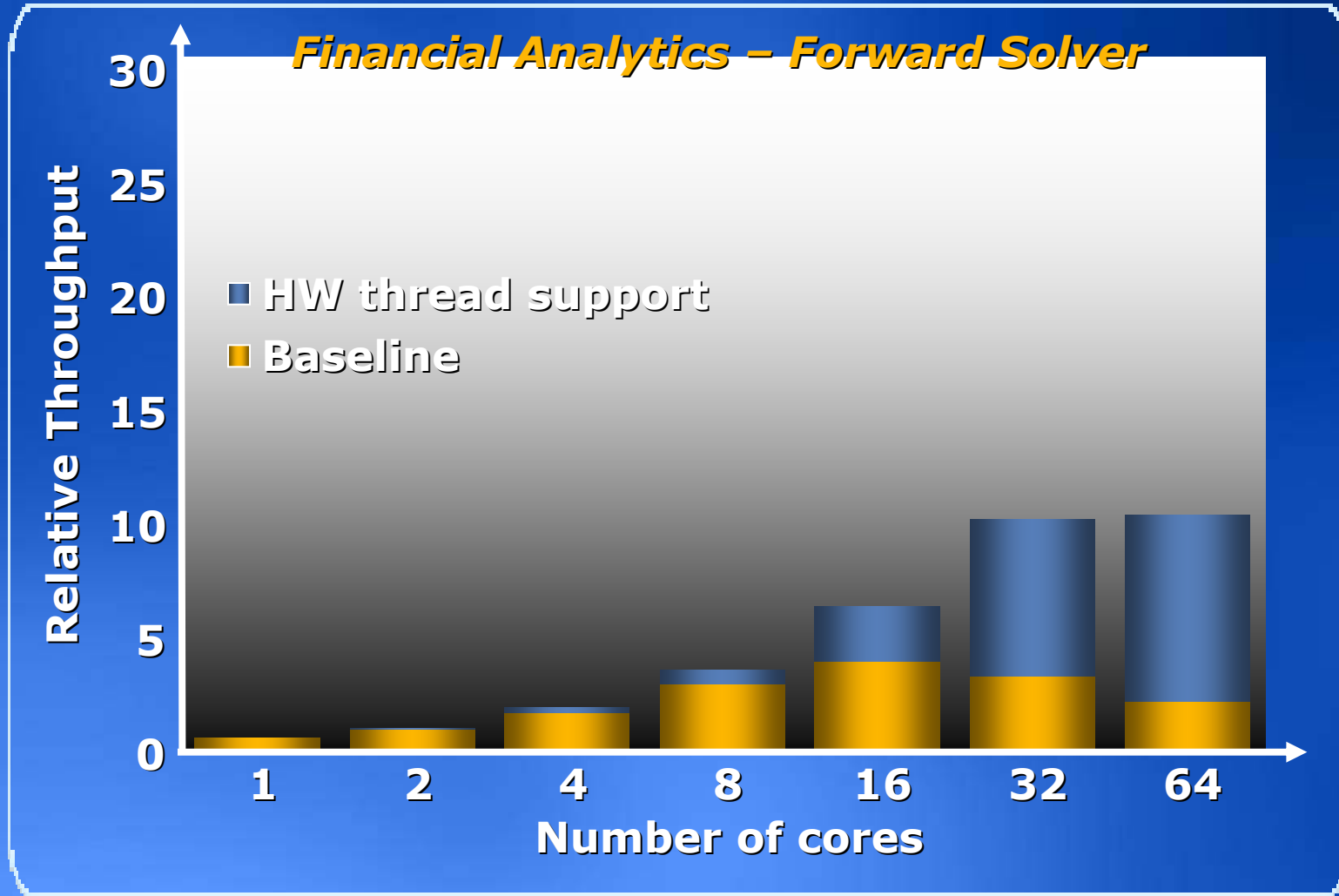
Performance vs. Scalability



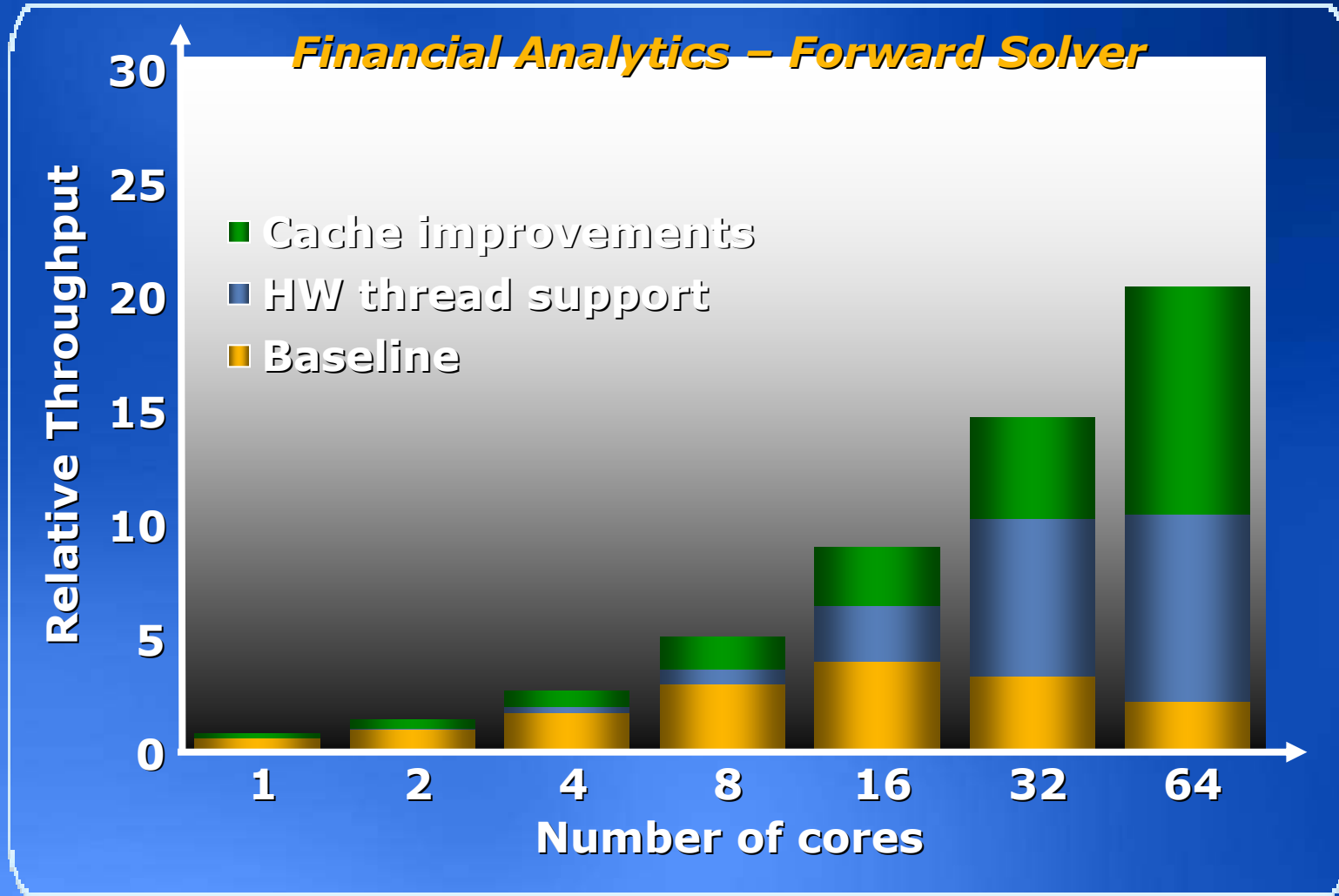
Architecture-Algorithm Co-Design



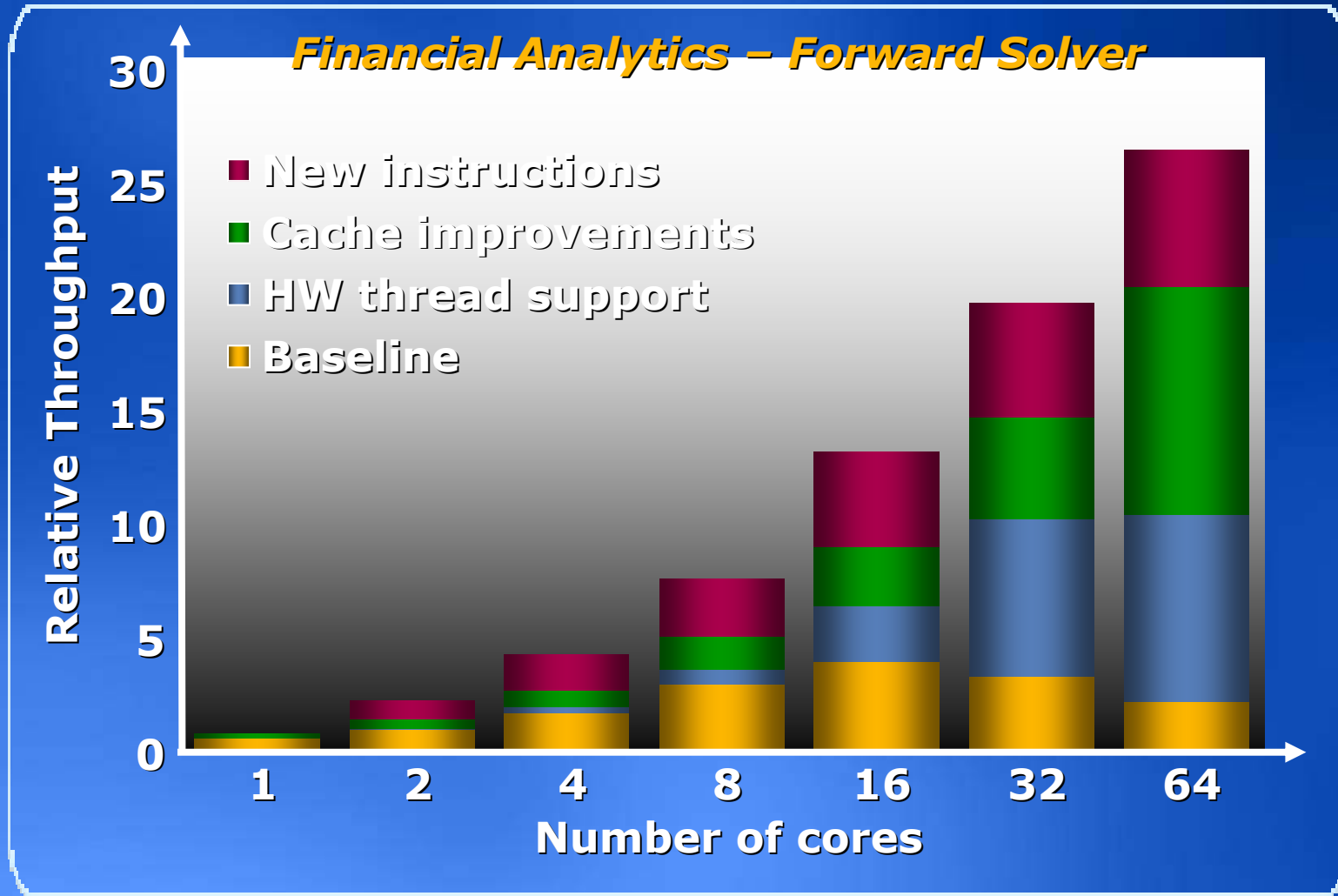
Architecture-Algorithm Co-Design



Architecture-Algorithm Co-Design



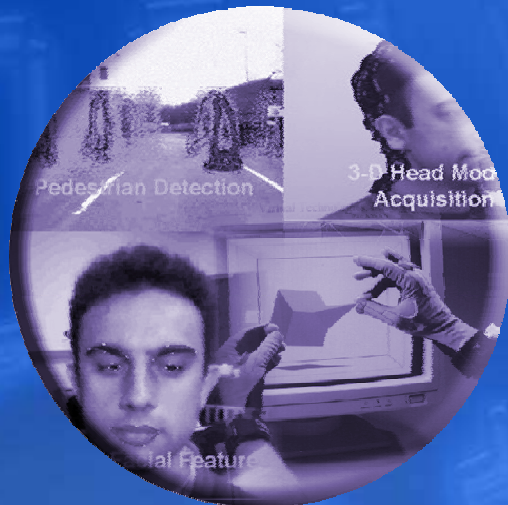
Architecture-Algorithm Co-Design



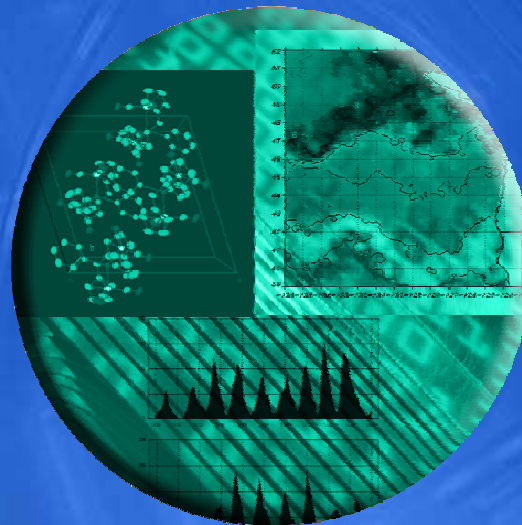
Emerging 'Killer' Applications

The RMS Suite

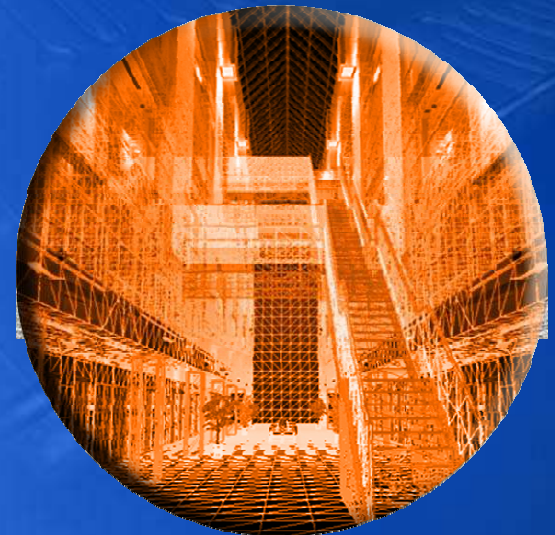
Recognition



Mining



Synthesis



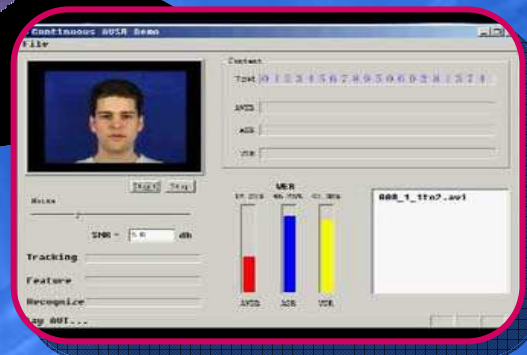
Emerging “Killer Apps” (R)



Recognition

“What is it?”

Modeling and identifying using multi-modal data



Source: Intel

Nefian, et. al, “Dynamic Bayesian networks for audio-visual speech recognition,” Journal of Applied Signal Processing, 2002

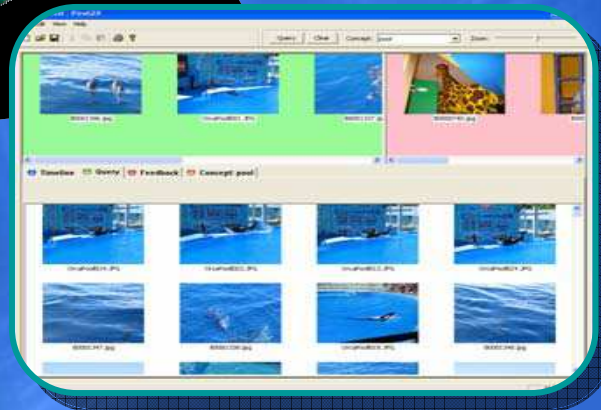


Emerging “Killer Apps” (M)



Mining

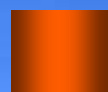
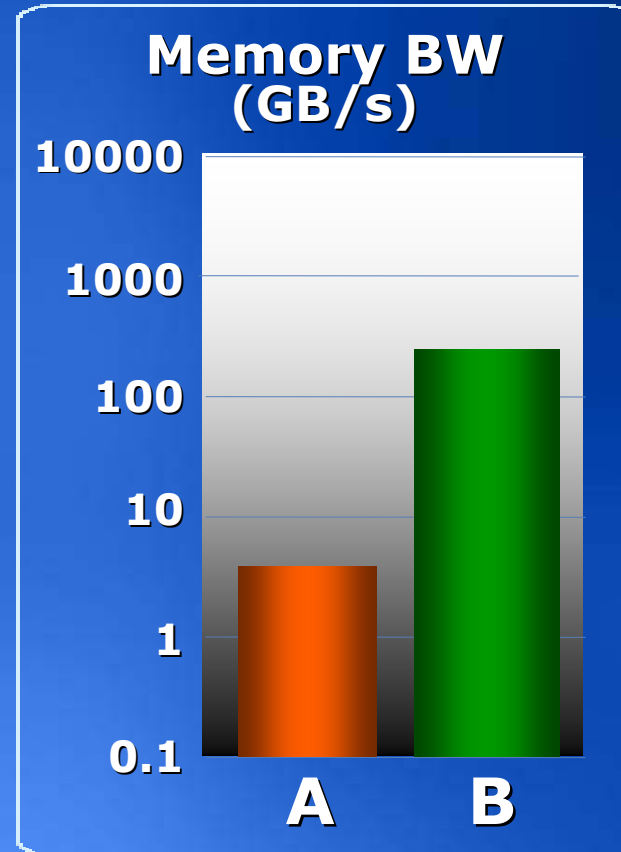
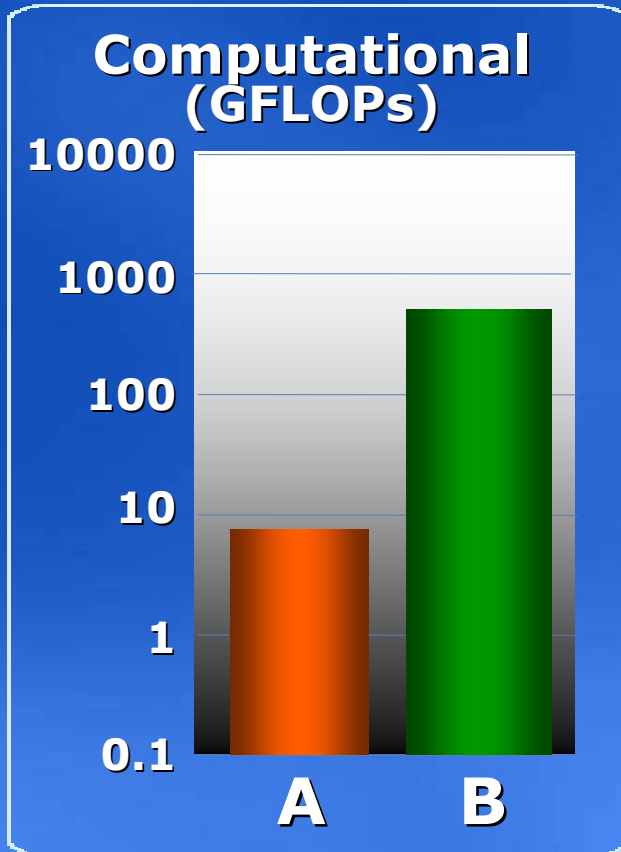
“Where is it?”
Search for a similar instance



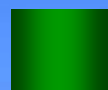
Source: Intel



Computer Vision



A: Video surveillance, 2 web cams



B: Body tracking, 4 DV cameras



Emerging “Killer Apps” (S)

Synthesis

“What if?”

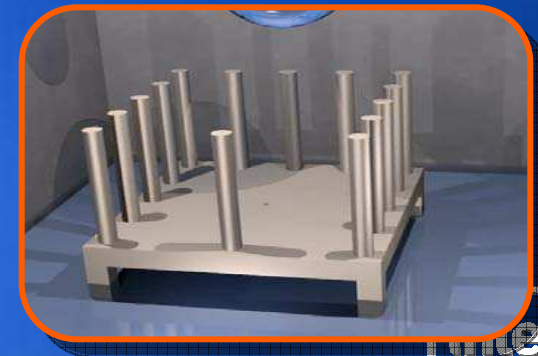
Creating new model instances



Source: Intel



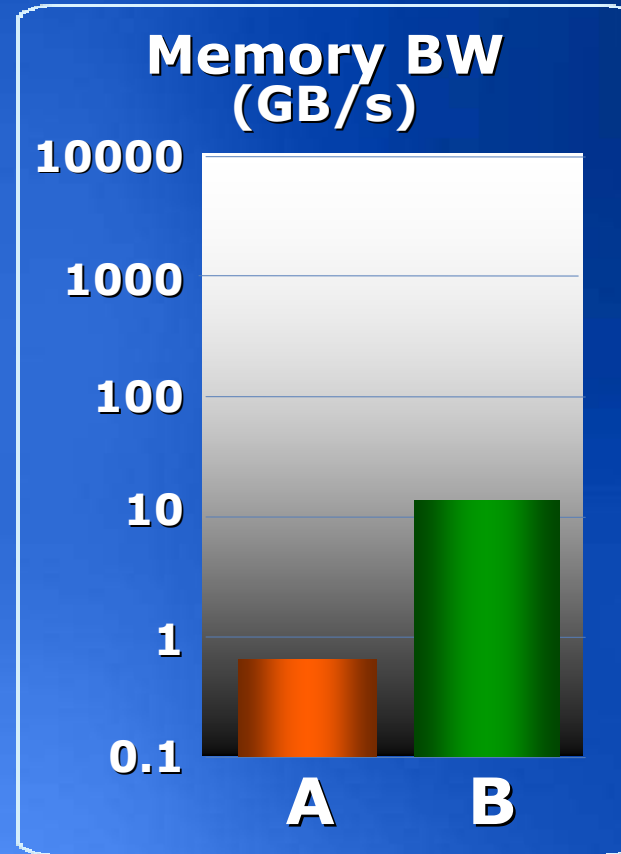
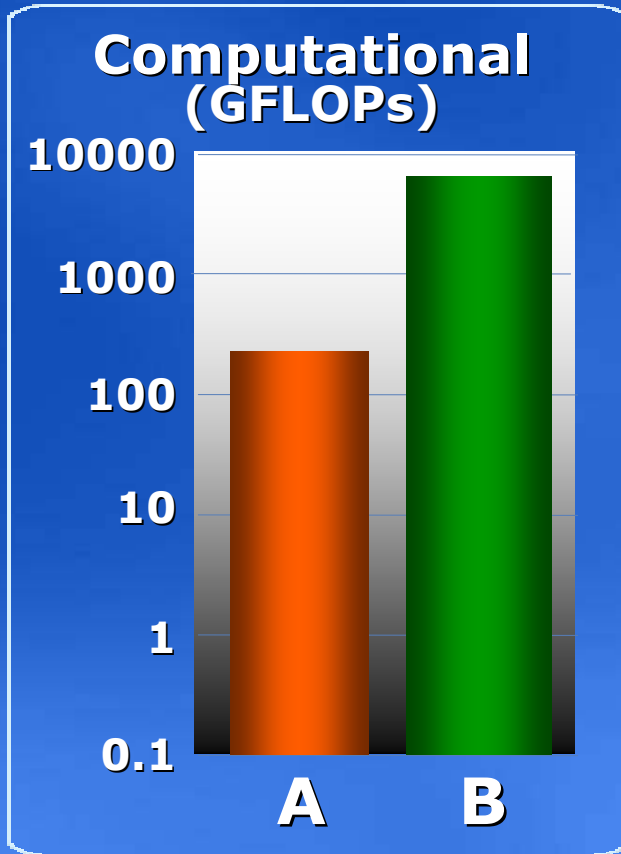
Source: InTrace

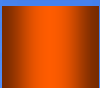



Source: Stanford

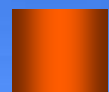
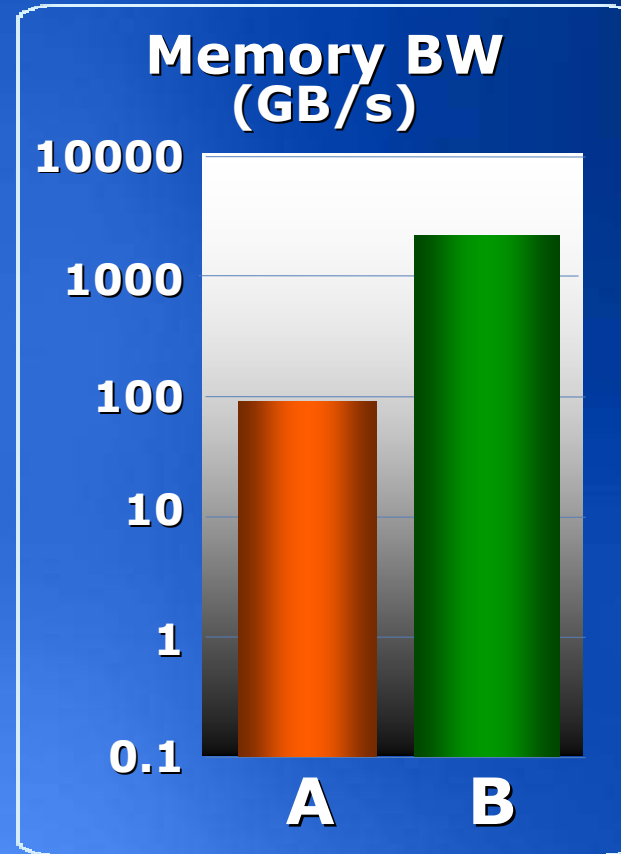
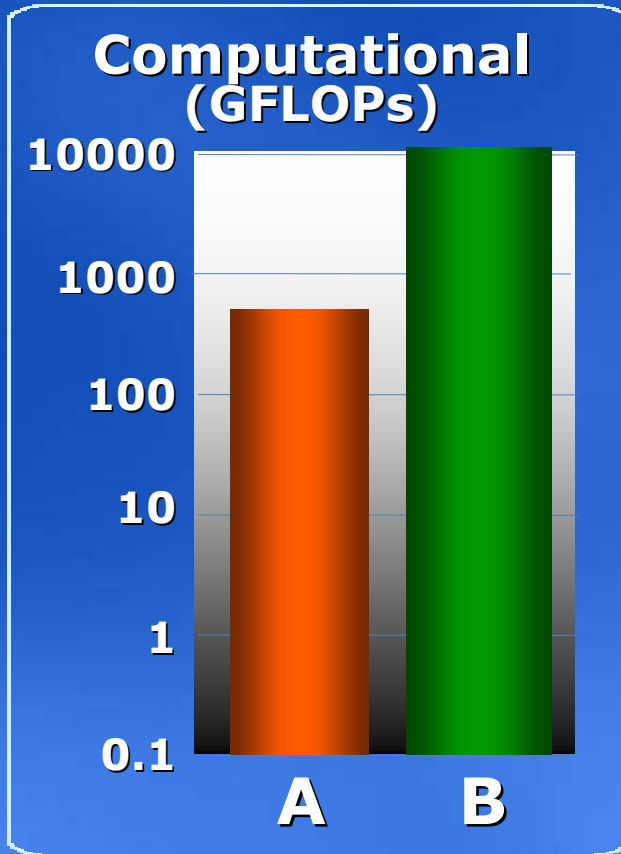


Ray-Tracing

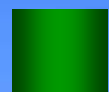


-  A: Bar scene, 1 mega-pixel
-  B: Beetle scene, 1 mega-pixel

Physical Simulation



A: CFD, 75x50x50, 10 fps



B: CFD, 150x100x100, 30 fps

Intel's RMS Application Suite

Ray tracing / Global illumination

Rigid body game physics

Fluid simulation

Facial animation

Cloth simulation

Full body tracker

Face detection

Audio-visual speech recognition

Multi-document summarization

Text indexer

Mortgage based security valuation

Portfolio management

Bioinformatics suite

Graph mining

Frequent itemset mining

Sports video highlight extraction



Intel's RMS Primitives Suite

Interior point method

Signal / image processing

Combinatorial optimization

Partitioning structure collision tests

FG/BG and Canny edge detection

Convex optimization

Partitioning structure build/traversal

Level set/fast marching method

Machine learning primitives

Numerical integration suite

Finite element/difference/volume

Dense matrix primitives

Sparse matrix primitives

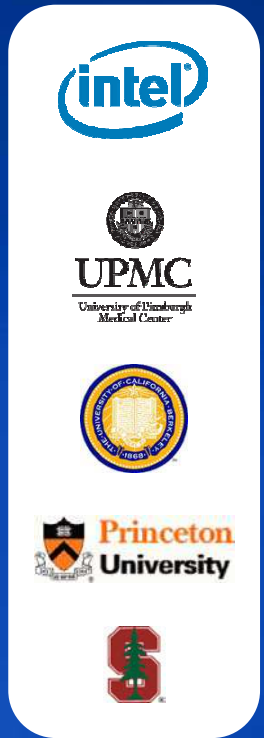
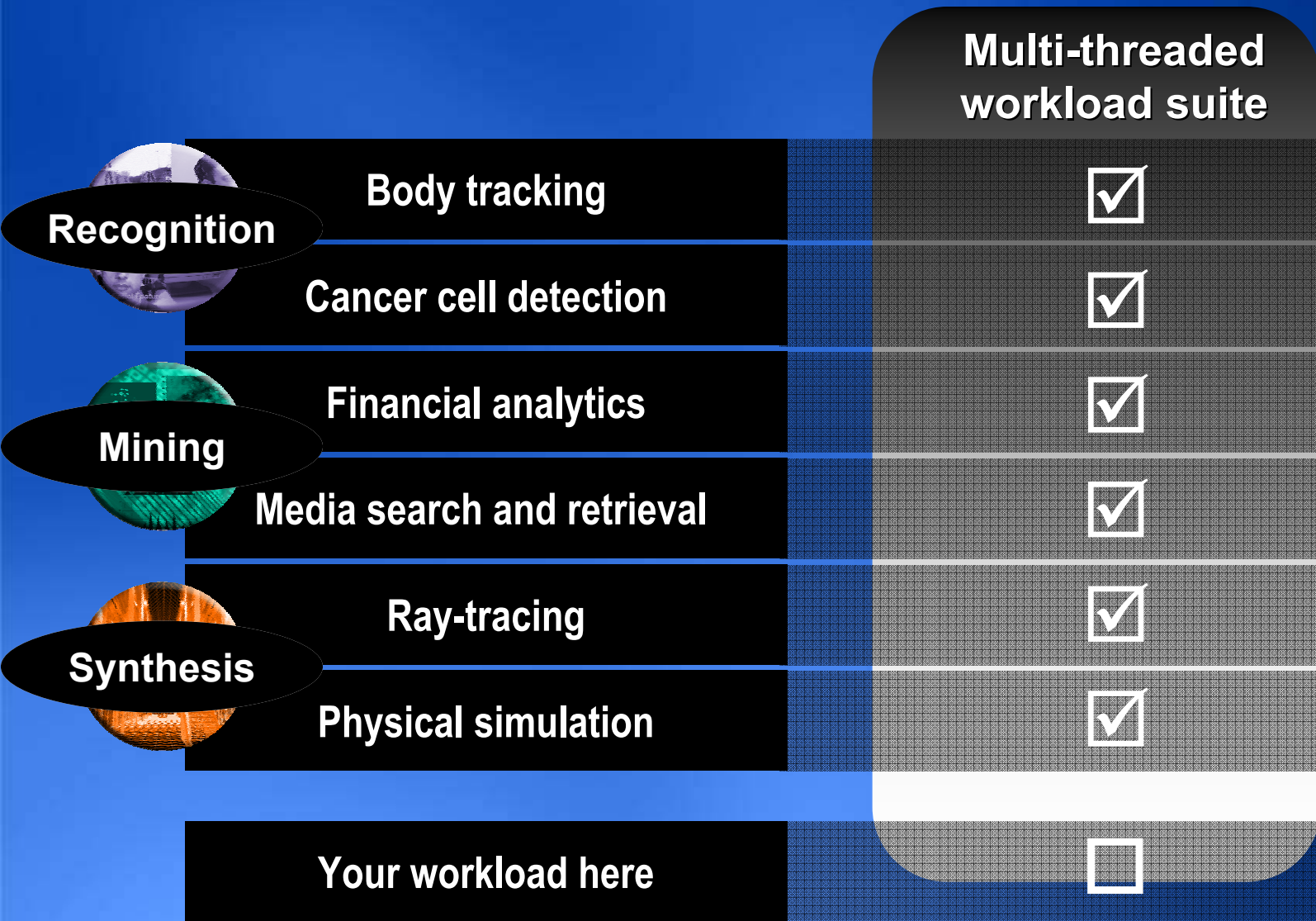
Stochastic optimization

PCG/Jacobi/Gauss-Siedel/PSCR

Black-Scholes/American options



Creating a Public RMS Suite



*Third party marks and brands are the property of their respective owners

Suite Repository and Working Group



Professor Kai Li

Charles Fitzmorris Professor
Department of Computer Science

Professor J. P. Singh

Department of Computer Science





***The Future of Multi-core
Processors is in Our Hands***



