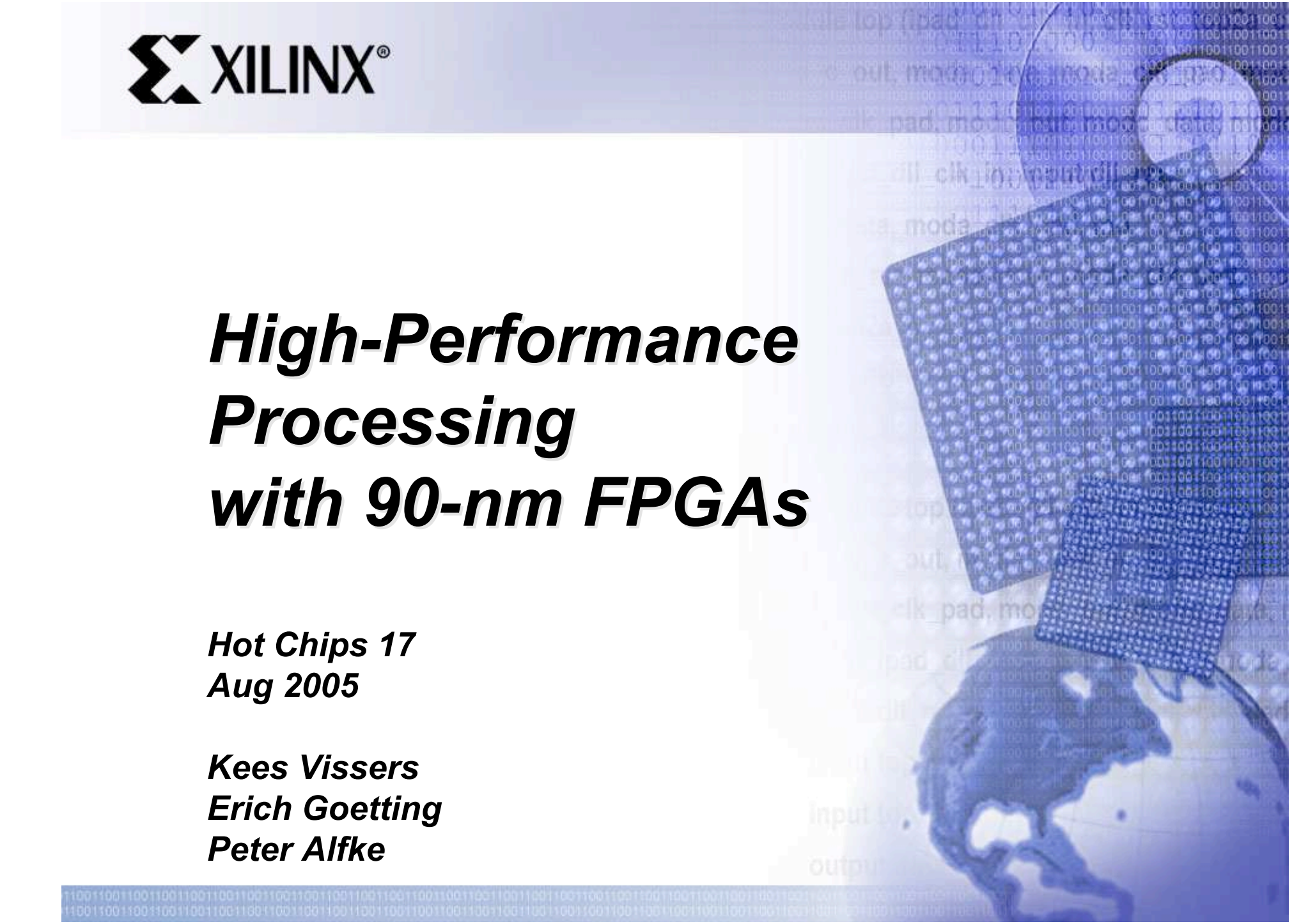


High-Performance Processing with 90-nm FPGAs

Hot Chips 17
Aug 2005

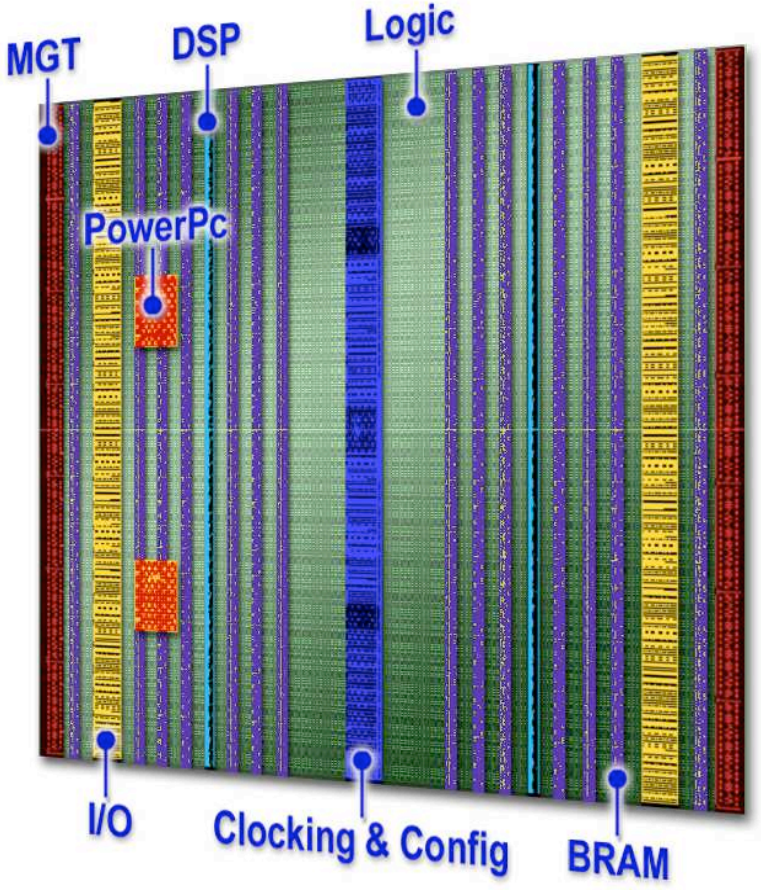
Kees Vissers
Erich Goetting
Peter Alfke

Agenda

- *Virtex4 Overview*
- *Processor and FPGA performance*
- *Three Examples*
  - *Cellular Telephone Basestation*
  - *Scientific Co-Processor*
  - *Image Enhancement for Movies*
- *Conclusion*

ASMBL Using Flip-Chip

- **A**pplication-**S**pecific **M**odular **BL**ock Architecture
- Groups specific circuit blocks in dedicated columns
  - Logic, DSP, BRAM, Clocking, DCMs,
    I/O, MGTs, PowerPC, Configuration
- I/O columns distributed throughout the device (Flip-Chip)



Three Virtex-4 Families

- Application-Specific Modular Block Architecture makes it easier to create sub-families
  - **LX** has logic, BlockRAMs, DSP-Blocks, I/O
  - **SX** has more DSP Blocks and BlockRAMs, less logic
  - **FX** adds powerful system features:
    - PPC, Ethernet controller, 11 Gbps transceivers

Virtex-4 = eight 'LX, three 'SX, six 'FX circuits

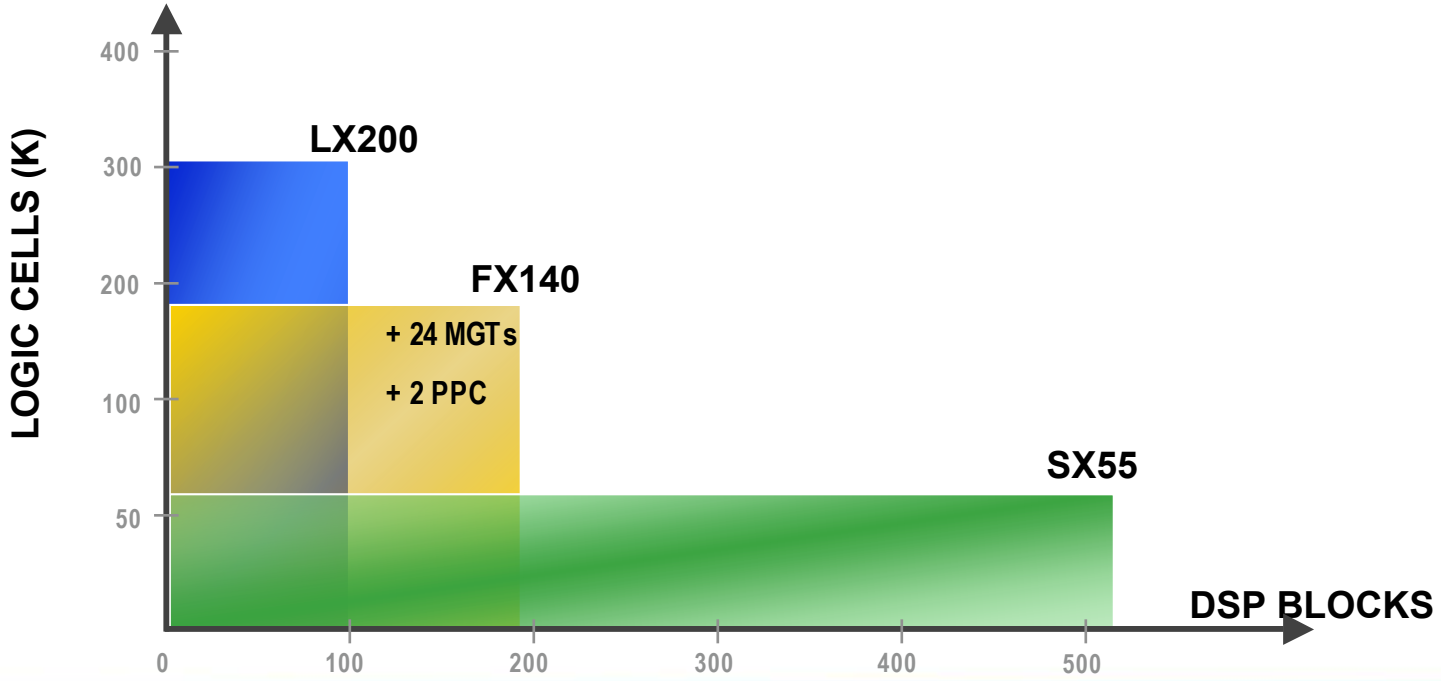
17 family members available in 2005

3 Families = Scalable Performance

LX 15, 25, 40, 60, 80, 100, 160, 200

FX 12, 20, 40, 60, 100, 140

SX 25, 35, 55 (name = number of Logic Cells x 1000)



Dedicated Circuits in FPGAs

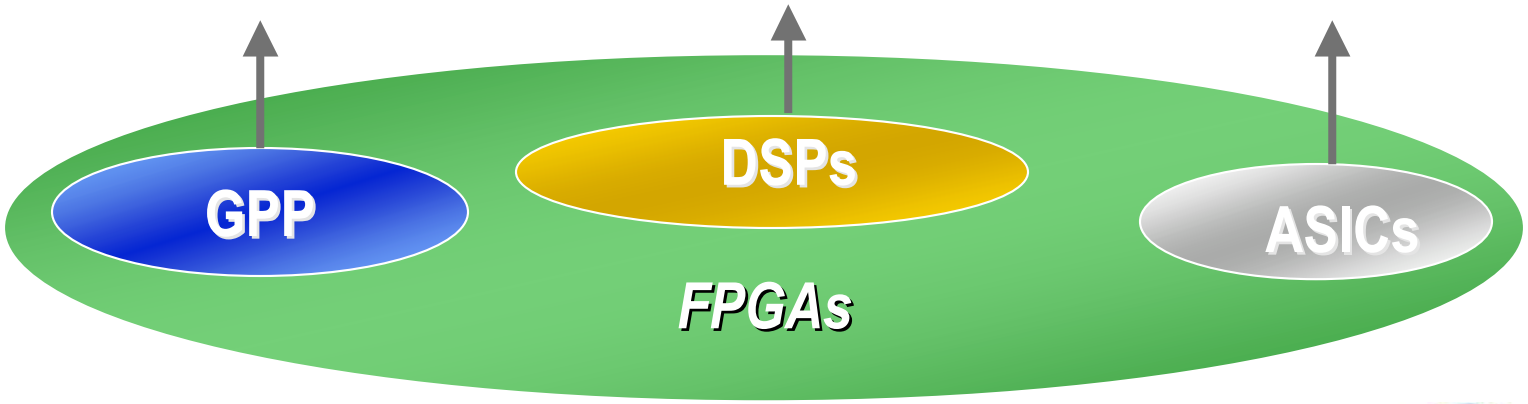
- **"Hard" cores** offer density, speed, lower power
  - Equal to 90-nm ASICs, but far less expensive
- Expandable, pipelined **Multiplier/Accumulator**
- Dual-ported **BlockRAM** with **FIFO** controller
- ChipSynch **I/O serializer/ deserializer + IDELAY**
- **Multi-Gigabit transceivers**, 0.6 to 11 Gbps
- PowerPC **µProcessor** with co-processor interface (APU) and **Ethernet** controller

Dedicated circuits provide a big performance boost

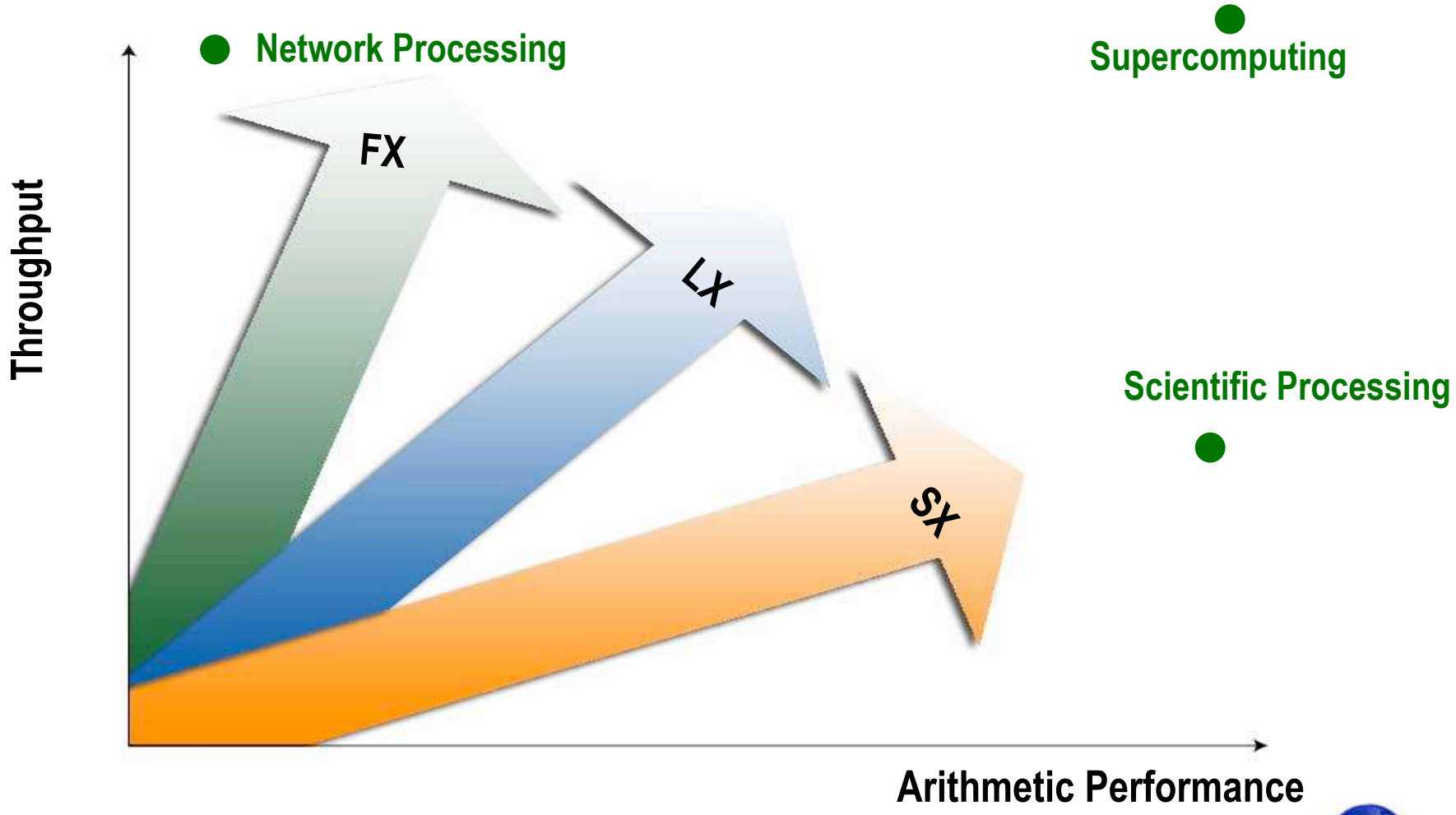
Processor and FPGA Performance

1000:1 Performance Range

Element	PPC	PPC + APU	Interleave	LUTs + DSP48
Clocks per sample	1000 : 1	100 : 1	10 : 1	1 : 1
500 MHz clock	500 Ks/sec	5 Ms/sec	50 Ms/sec	500 Ms/sec
Memory	4-256 KByte	4-256 KByte	10 KByte	1 KByte
Applications	control → audio →	mobile video →	HDTV →	communications

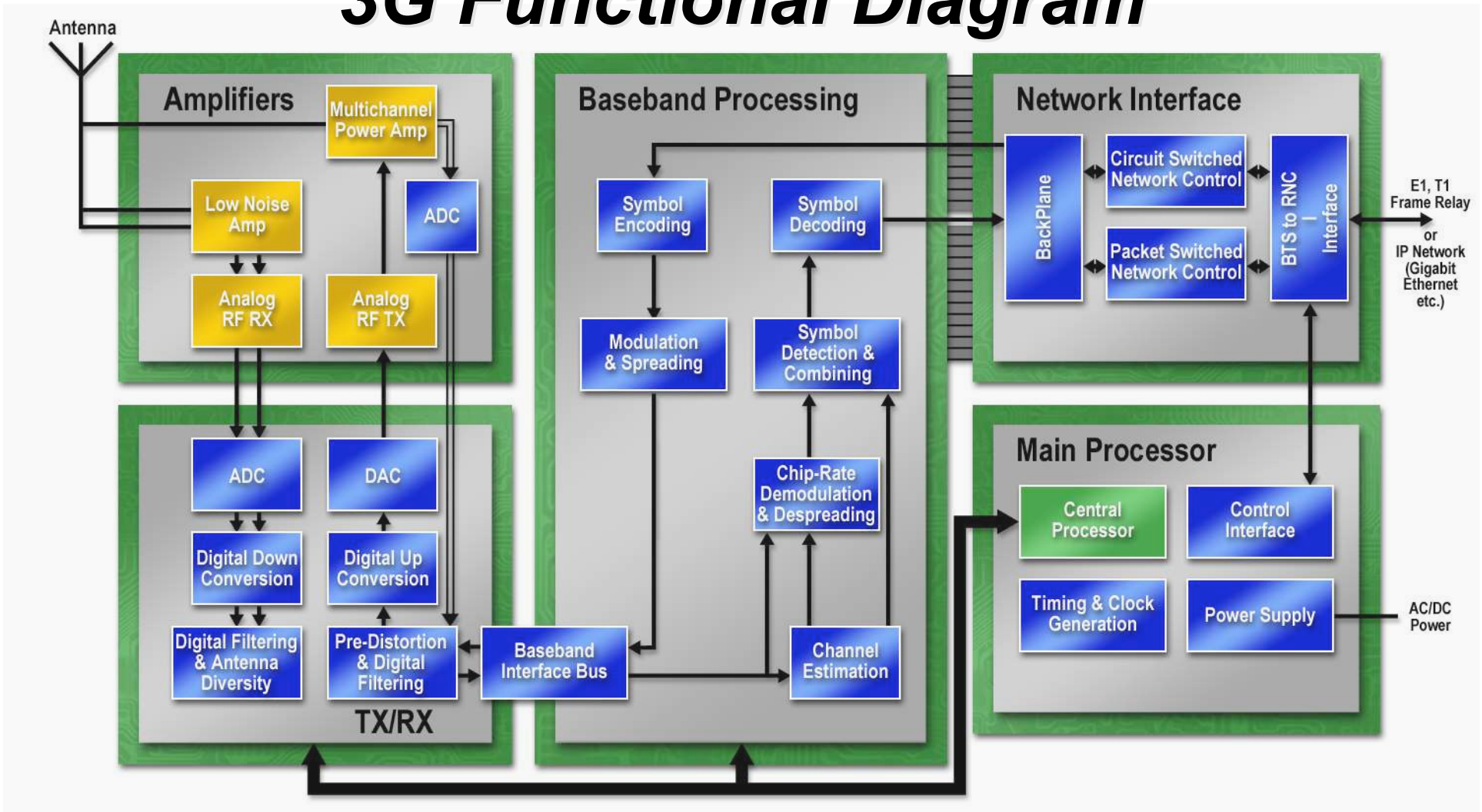


Covering a Wide Range



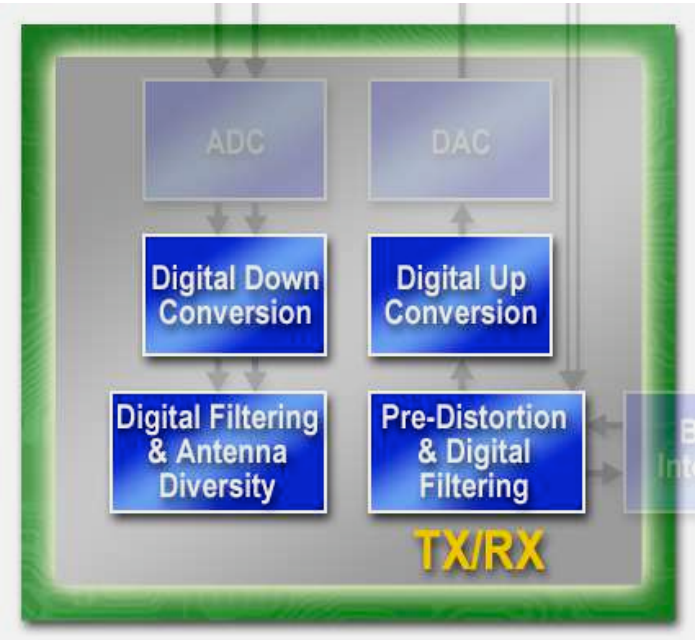
Example: Cellular Telephone Base Station

Wireless Base Station
3G Functional Diagram



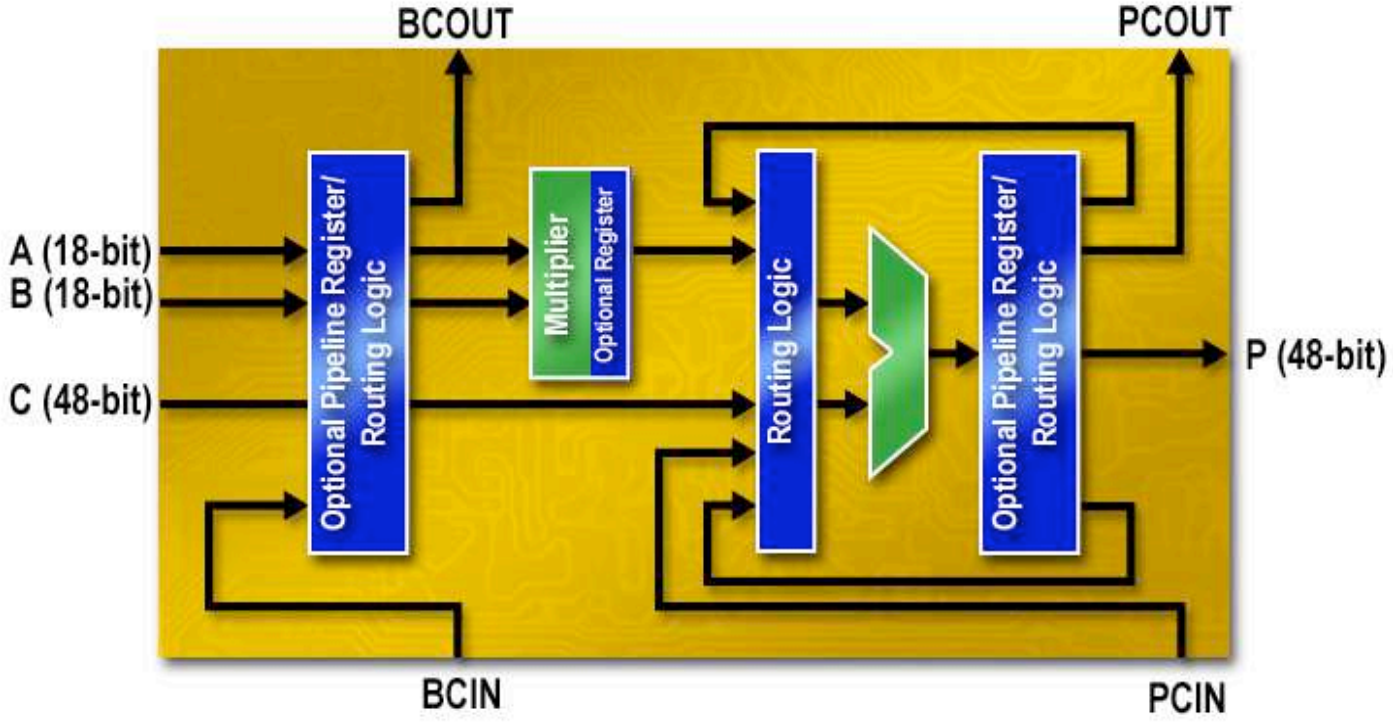
TX/RX Implementation

- 3G specification: each channel has a sample rate of 3.84Ms/sec
  - Digital Filtering at 491 MHz
    - 128 channels
      using 128x the sample rate
  - Digital Up/Down Conversion
  - Pre-Distortion and Digital Filtering
    - Up to 512 18x18 multipliers + accumulators
      to build massively parallel filter implementations



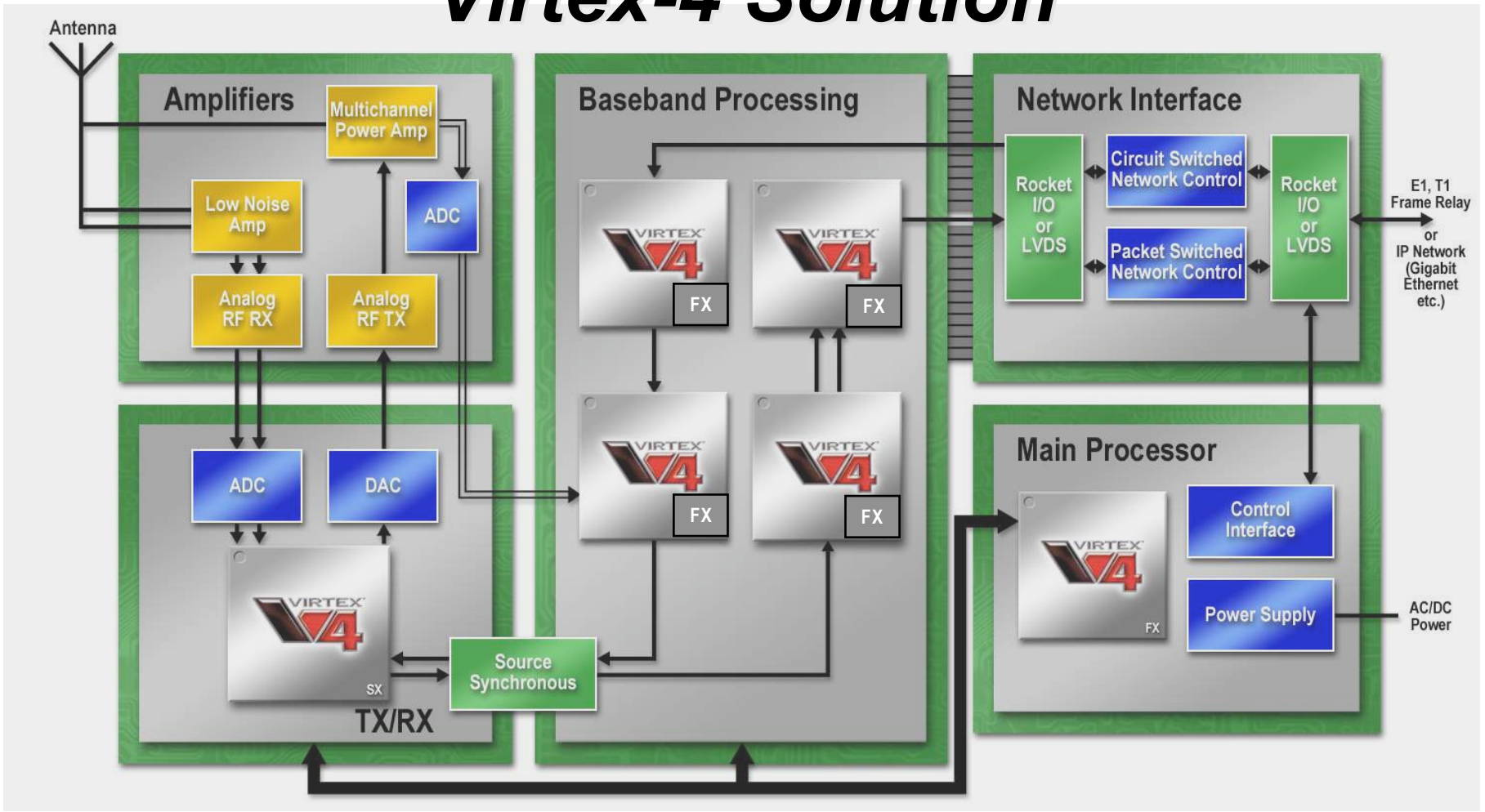
DSP Block

- Evolution from embedded multipliers:
  - Pipeline registers enable 500 MHz performance
  - Cascade logic enables sustained 500 MHz performance throughout DSP column
  - Build high-speed multi-level filters using DSP Slices
  - ***Achieve 128x the sample rate of 3.84 Ms/sec (491.5 MHz clocking)***



Wireless Base Station Example

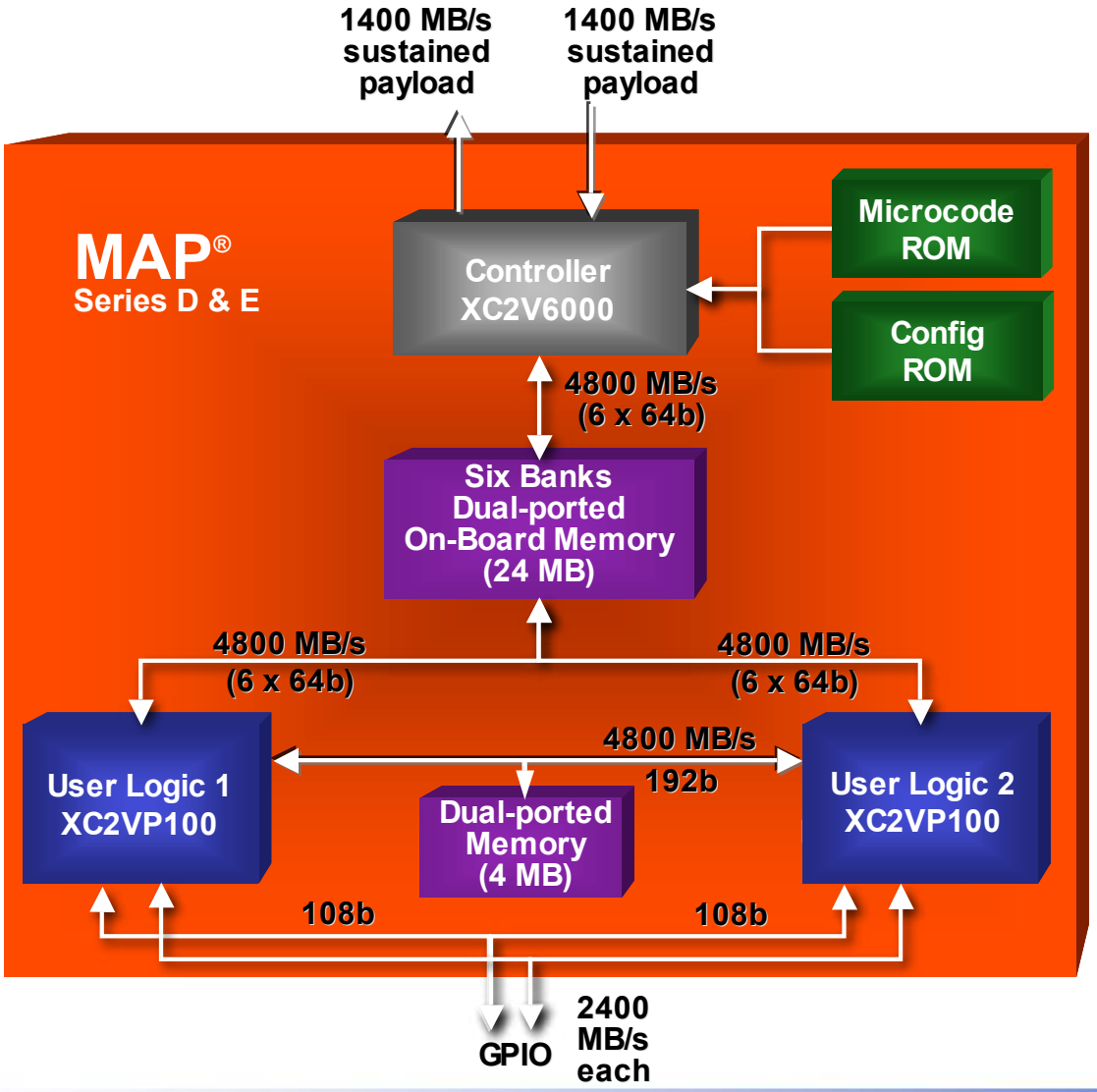
Virtex-4 Solution



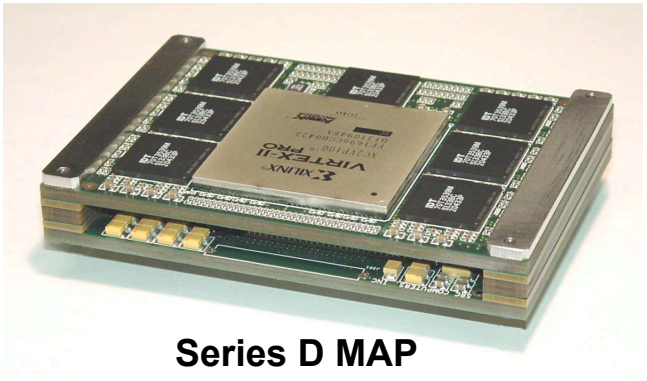
Support for 128 channels using Virtex-4 FPGAs

Example:
Scientific Co-Processor

Supercomputer



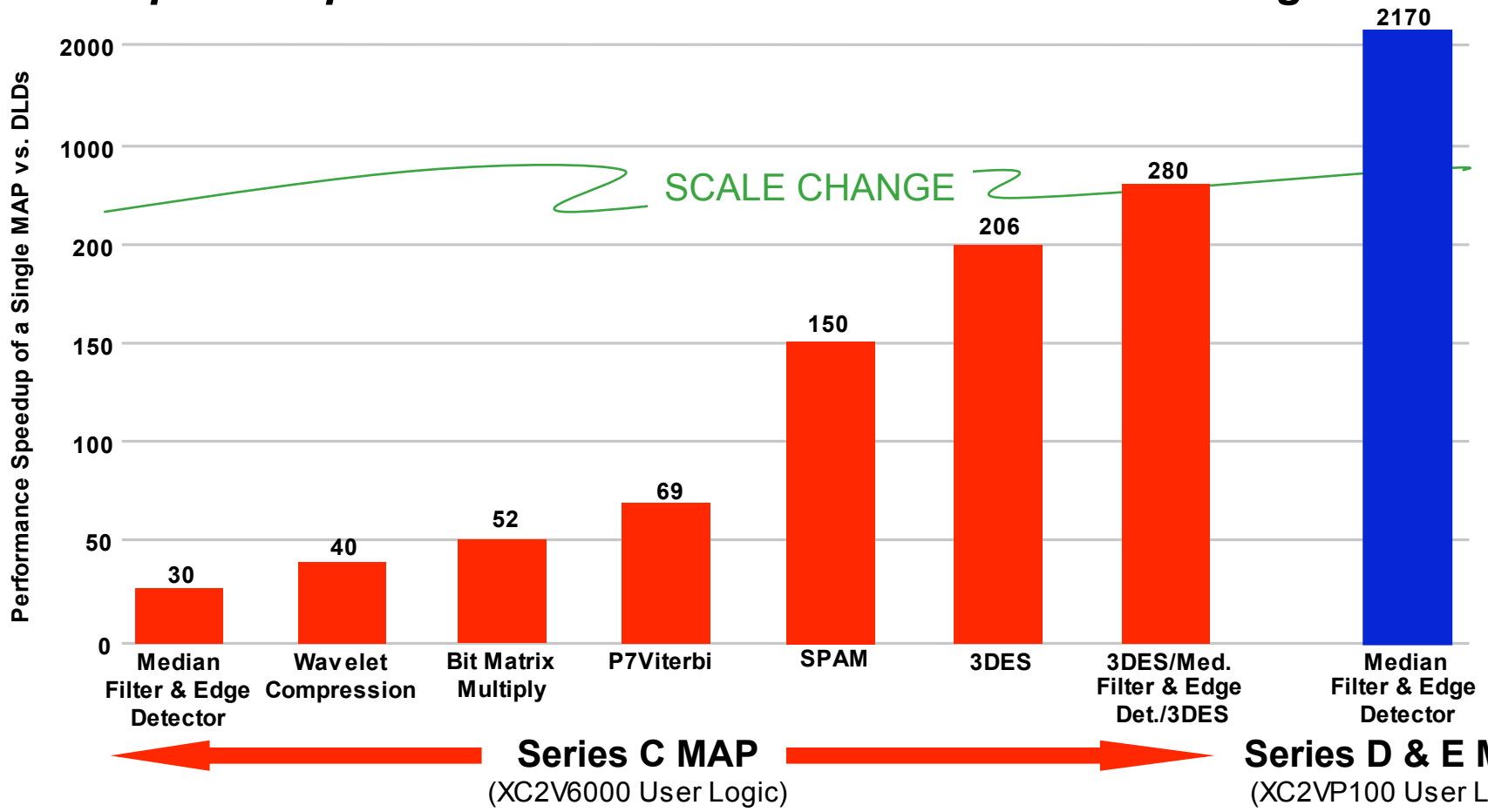
- Programmed with Carte™ tools, using C or Fortran
- Overlap of DMA and computing



Series D MAP

MAP® Logic Performance

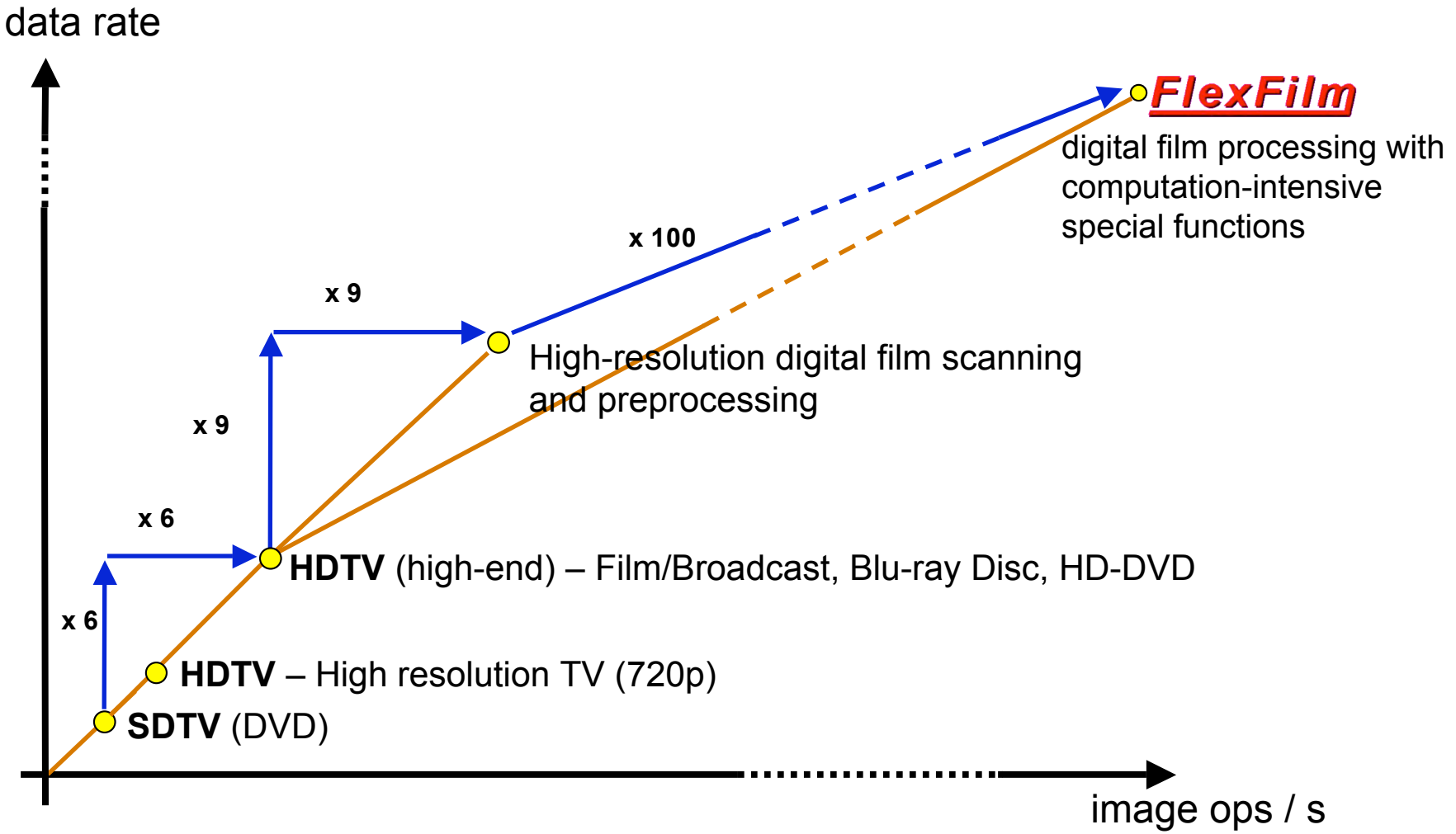
Number of 2.8 GHz microprocessors required to equal the performance of one SRC MAP® on select algorithms



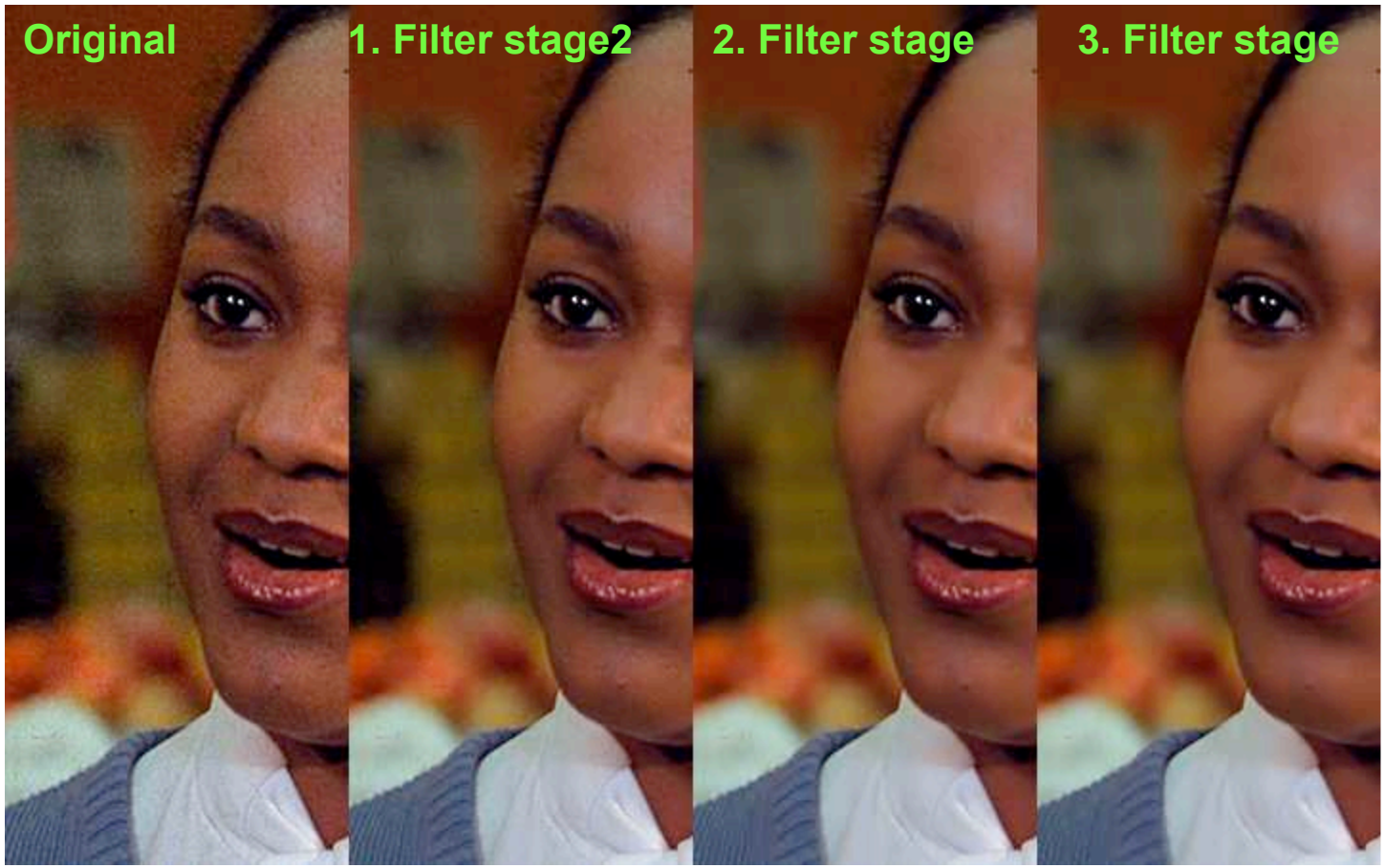
Source: SRC Computers, Inc. - Comparisons are based on measured single microprocessor and single MAP processor performance

Example: Image Enhancement for Movies

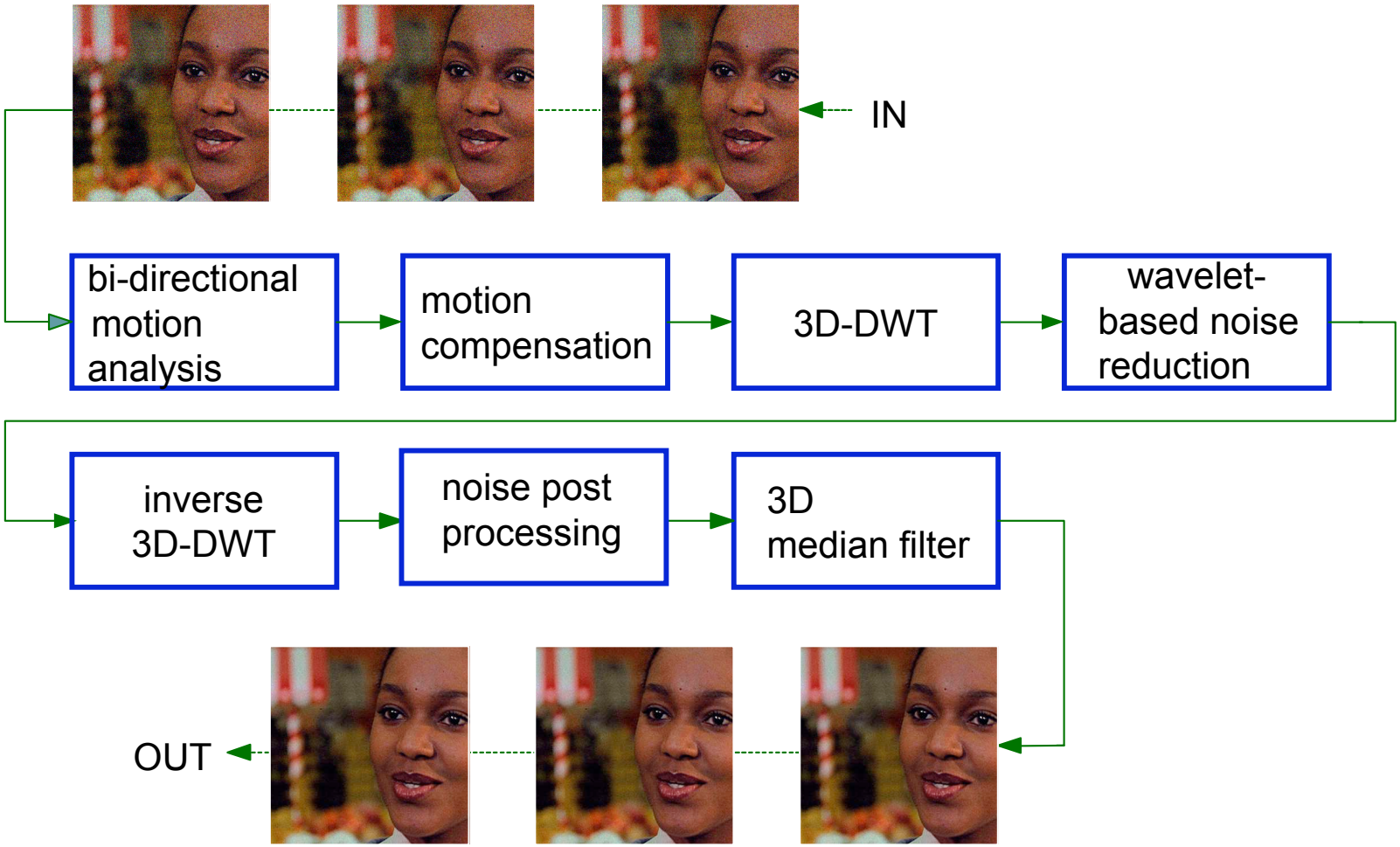
Digital Film Processing



Application: Noise Reduction



Application: Noise Reduction



Film Processing Statistics

Image 2048x2048, 10bits per RGB component =30 bits/pixel

2D intra-frame algorithm

- **Software** solution: compiled from Matlab -> C/C++,
  on Pentium IV 2.4GHz, 1.5GB RAM, 10.2 Specint2000
  Performance: 70 seconds per frame

- **Hardware** solution: One XC2VP50-6*, 120 MHz, synthesis,
  Performance: 24 frames per second

Operations	Add	Multiply	Compare	**FPGA speed-up**
Giga-ops	9.44	5.81	3.62	**1,680**

* an XC2VP50 is comparable to a Virtex-4 LX40

Film Processing Statistics

Image size 2048x2048, 10 bit per RGB component

3D motion estimation/compensation inter-frame algorithm

- **Software** solution: compiled from Matlab -> C/C++,
  on Pentium IV 2.4GHz, 1.5GB RAM, 10.2 Specint2000
  Performance: 11 minutes per frame

- **Hardware** solution: Four XC2VP50-6, 120 MHz, synthesis,
  Performance: 24 frames per second

Operations	Add	Multiply	Comp	**FPGA speed-up**
Giga-ops	179.61	11.63	11.88	**15,840**

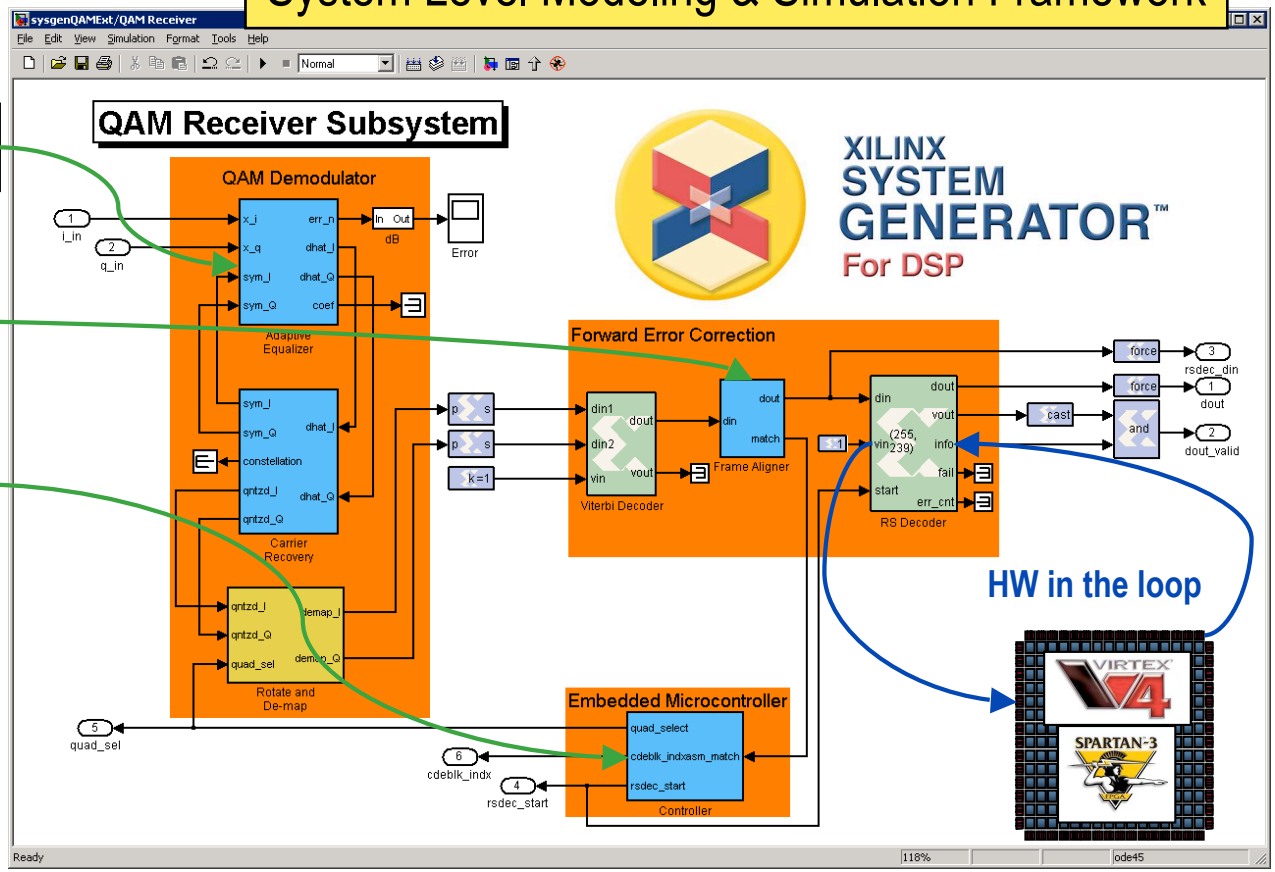
DSP Programming Model

Work in the language of your problem

MATLAB → AccelChip

HDL

C → Embedded Development Kit



Methodology re-couples behavior with implementation (while abstracting hardware details *whenever possible*)

Conclusion

- FPGAs combine configurable logic, fast I/O, processors, DSP elements, and hard cores
- Virtex4 has a family of scalable solutions
- For high-performance applications, the speed-up over a good general purpose processor can range from tens to several thousands
- Excellent FPGA-based solutions exist for base-stations, video-applications, networking, and high performance compute platforms

Acknowledgements

- The whole V4 team of the Advanced Product Division at Xilinx, see www.xilinx.com
- SRC Computers, Inc. for data on the compute platform, see www.srccomp.com
- University of Braunschweig, Prof. Rolf Ernst and Amilcar Lucas for the film processing data, see www.flexfilm.org

Appendix : Virtex-4 Family

Device	Logic Cells	Block RAM [Kb]	DCM	SelectIO	XtremeDSP Slice	PowerPC	10/100/ 1000 EMAC	RocketIO Transceiver
XC4VLX15	13,824	864	4	320	32	-	-	-
XC4VLX25	24,192	1,296	8	448	48	-	-	-
XC4VLX40	41,472	1,728	8	640	64	-	-	-
XC4VLX60	59,904	2,880	8	640	64	-	-	-
XC4VLX80	80,640	3,600	12	768	80	-	-	-
XC4VLX100	110,592	4,320	12	960	96	-	-	-
XC4VLX160	152,064	5,184	12	960	96	-	-	-
XC4VLX200	200,448	6,048	12	960	96	-	-	-
XC4VSX25	23,040	2,304	4	320	128	-	-	-
XC4VSX35	34,560	3,456	8	448	192	-	-	-
XC4VSX55	55,296	5,760	8	640	512	-	-	-
XC4VFX12	12,312	648	4	320	32	1	2	-
XC4VFX20	19,224	1,224	4	320	32	1	2	8
XC4VFX40	41,904	2,592	8	448	48	2	4	12
XC4VFX60	56,880	4,176	12	576	128	2	4	16
XC4VFX100	94,896	6,768	12	768	160	2	4	20
XC4VFX140	142,128	9,936	20	896	192	2	4	24