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A 1-GHz Configurable Processor Core
— MeP-h1 —

Takashi Miyamori, Takanori Tamai,
and Masato Uchiyama
SoC Research & Development Center,
TOSHIBA Corporation

MeP
Media embedded Processor

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Outline

- Background
- Pipeline Structure
- Bus Interface
- Implementation

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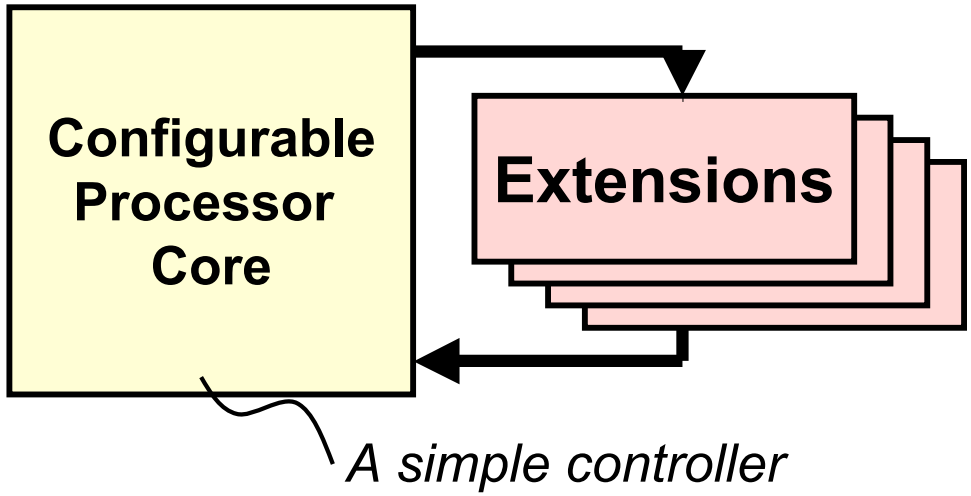
Configurable Processor

- Customize a processor during RTL design
- Configurations
  - Cache config., Local RAM config., bus width, etc.
- Extensions
  - User customized instructions (DSP instruction extension)
  - Self-running hardware blocks (Hardware engines)



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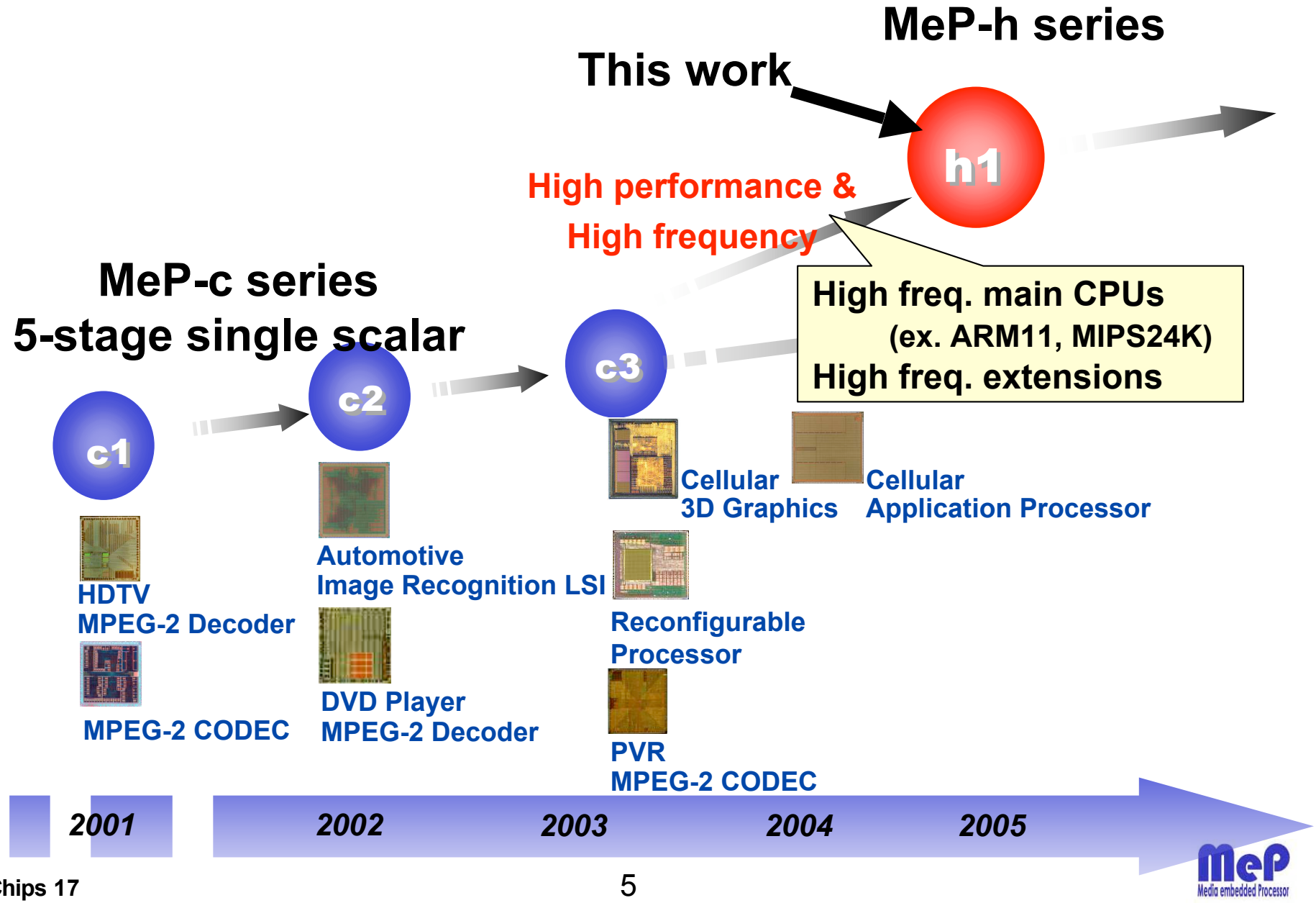
MeP Processor Roadmap



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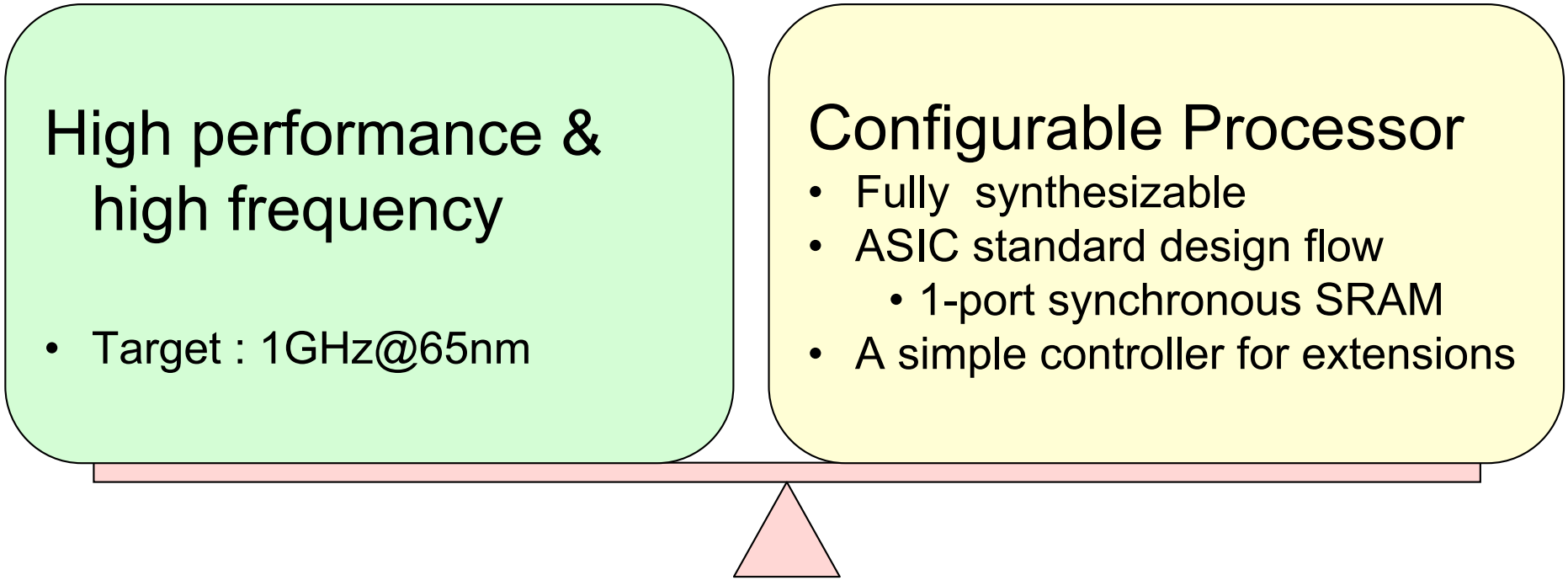
MeP-h1 Design Trade-off



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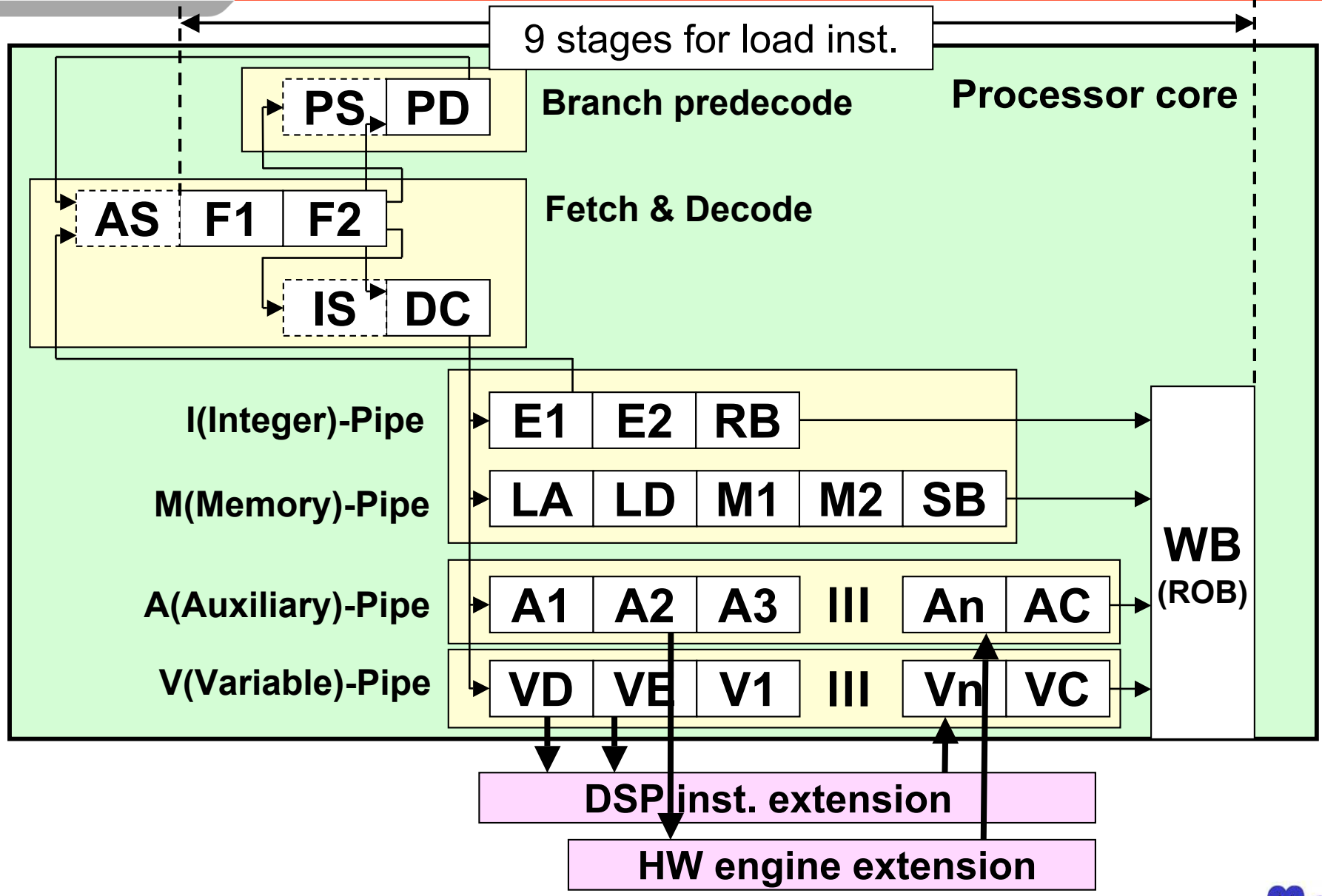
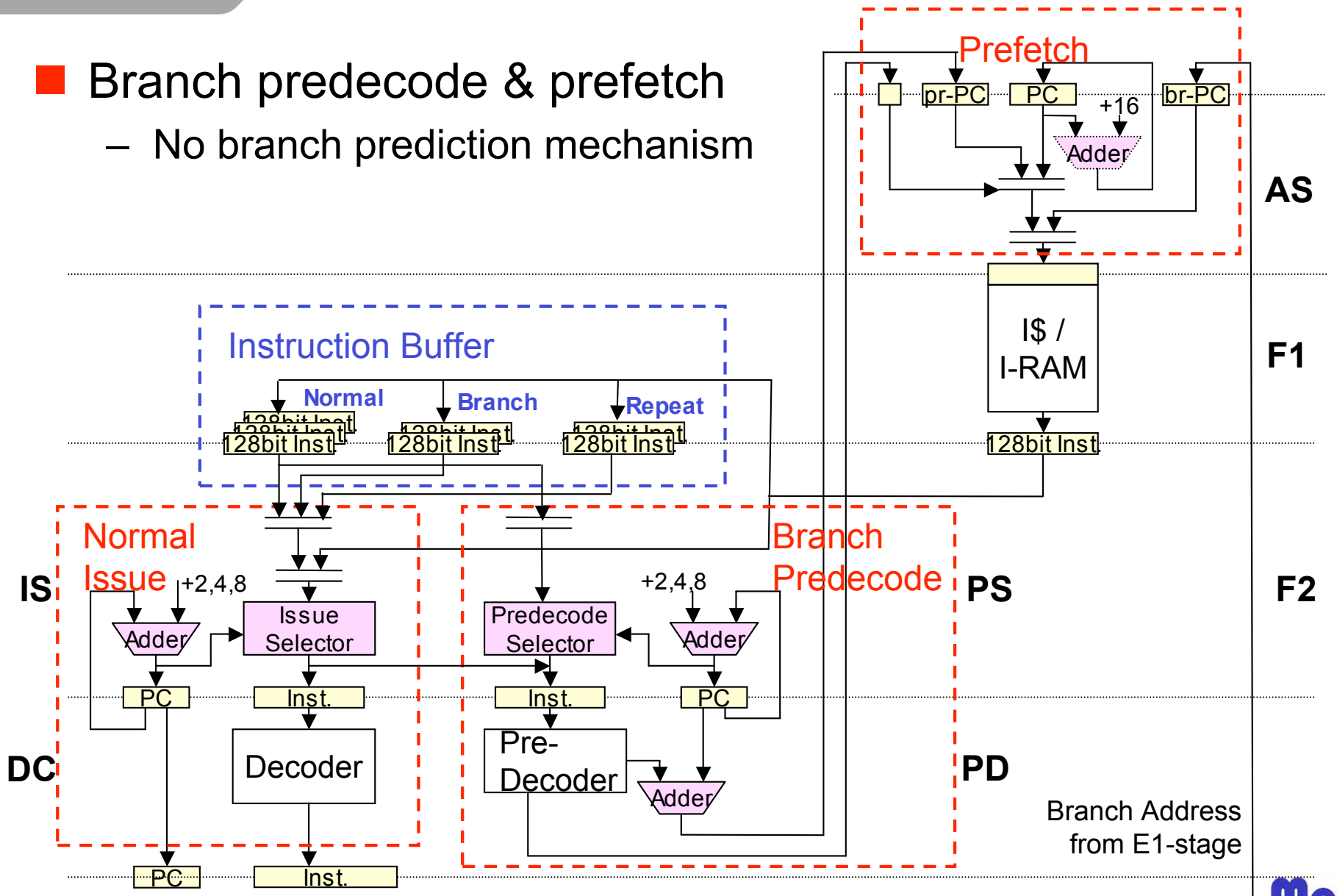
Pipeline Structure



MeP Media embedded Processor

Instruction Fetch Unit

- Branch predecode & prefetch
  - No branch prediction mechanism



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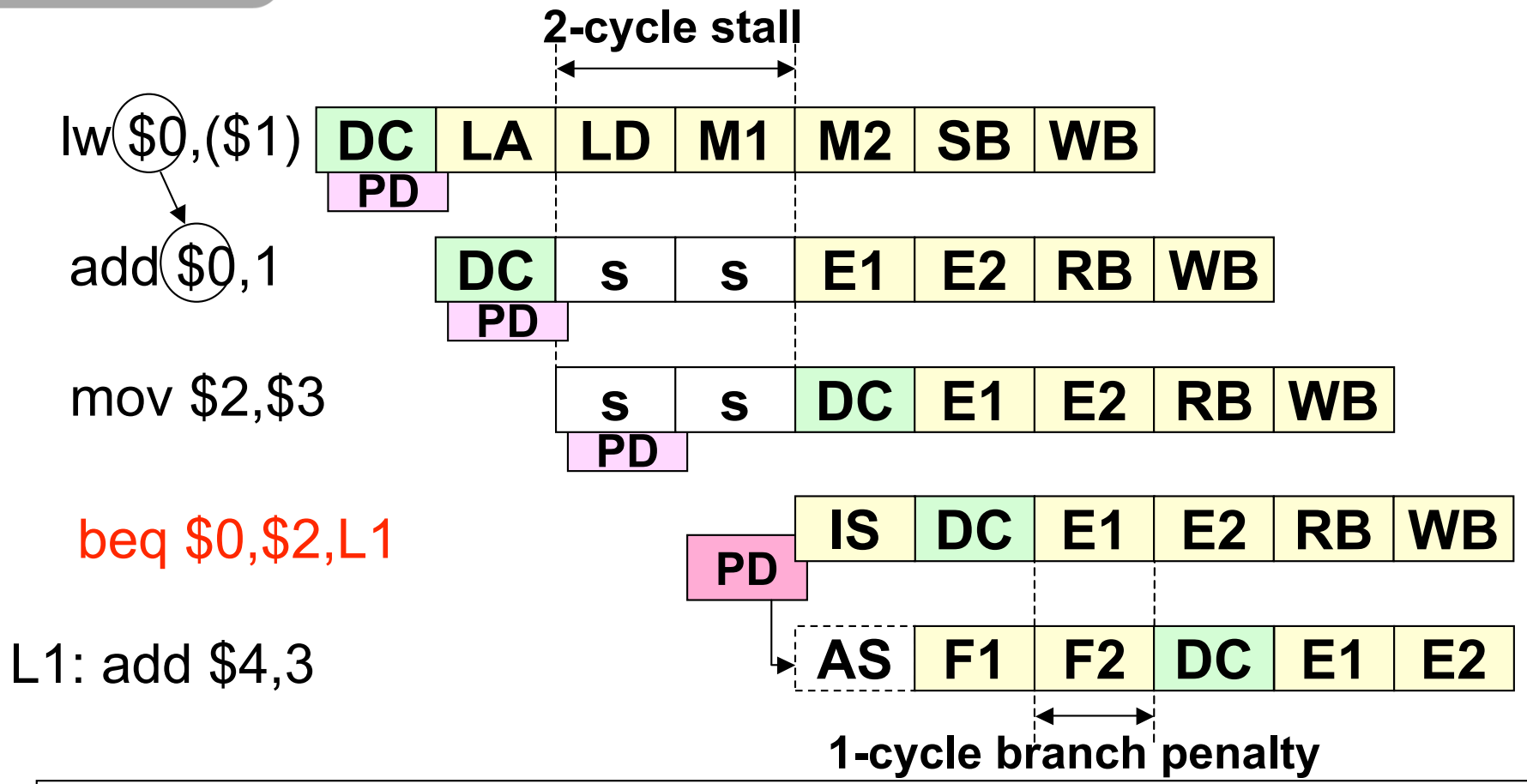
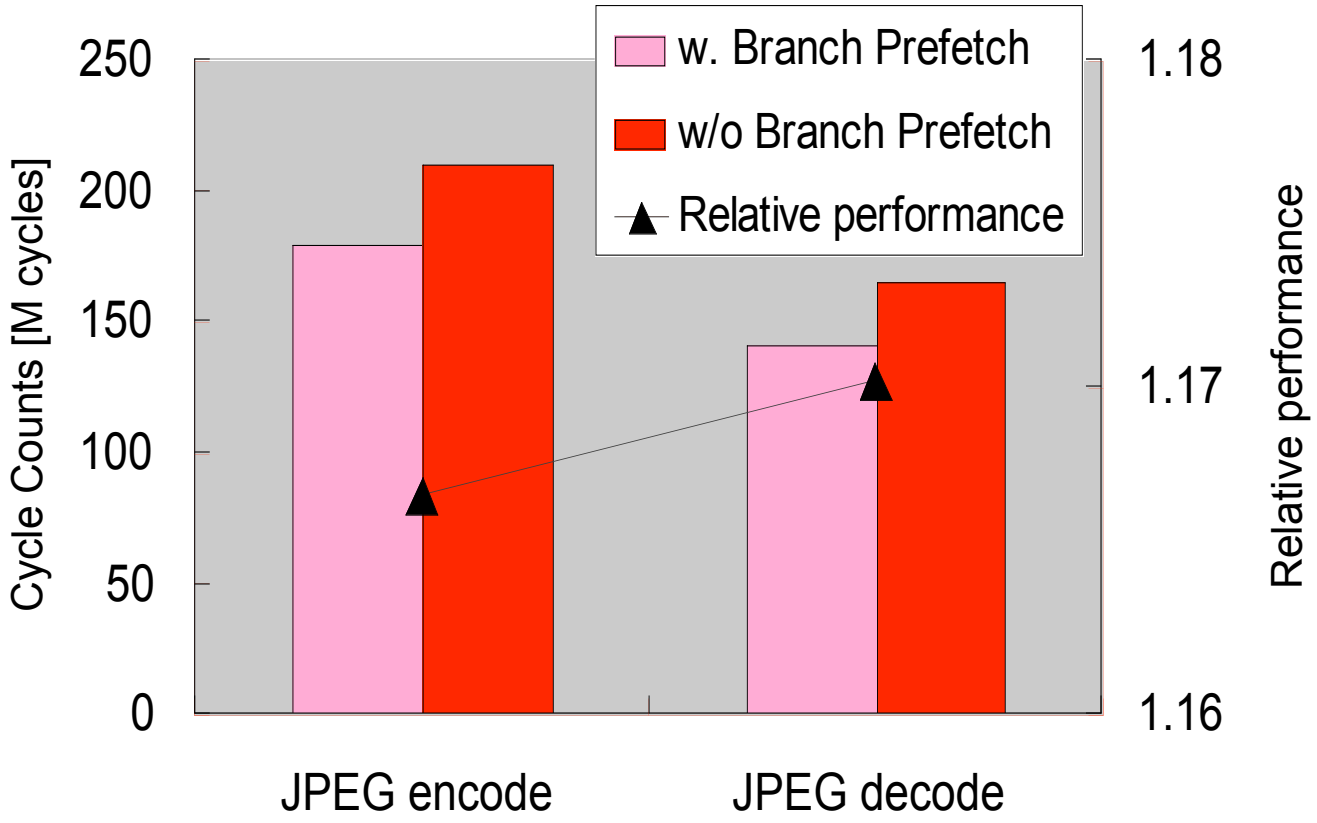
Branch Prefetch



- Branch penalty
  - Branch taken : 1 – 4 cycles (cf. 4 cycles w/o branch prefetch)
  - Branch not-taken: 0 cycles
- Repeat (loop) inst. iteration penalty : 0 cycles

Branch Prefetch Evaluation



- Average branch penalty: 1.8 cycles
- More than 80% of branch penalty is less than or equal 2 cycles

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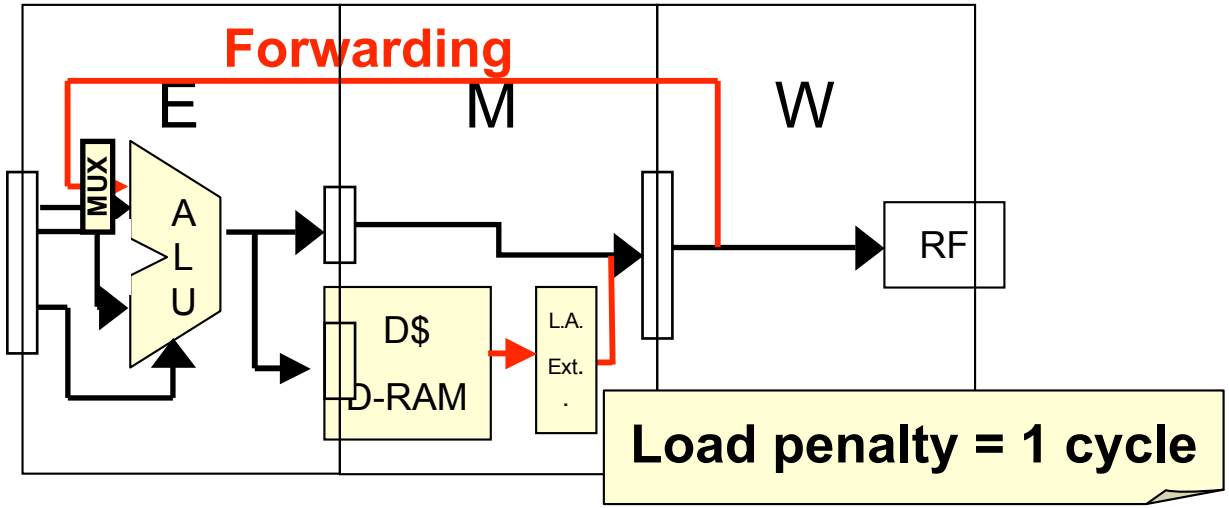
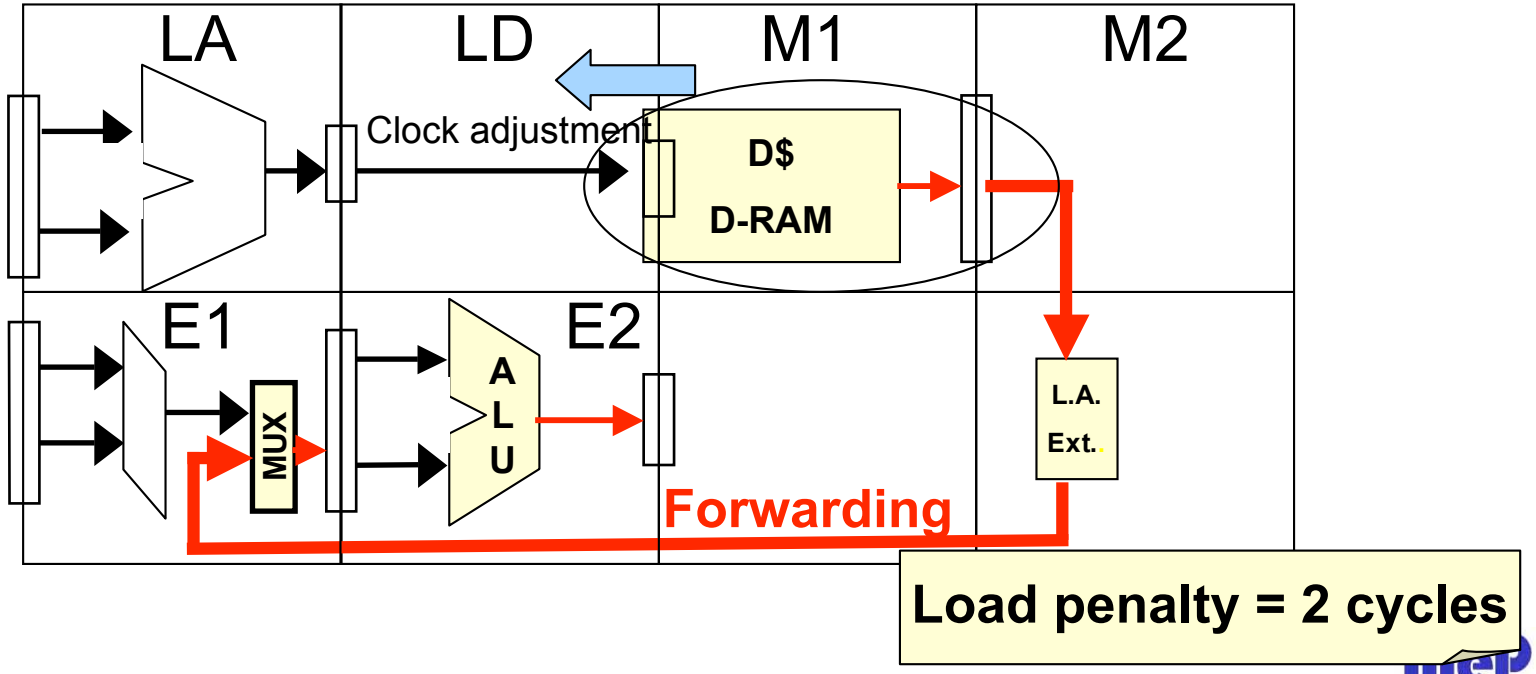
Load Data Forwarding

MeP-c3

- 5-stage pipeline



MeP-h1



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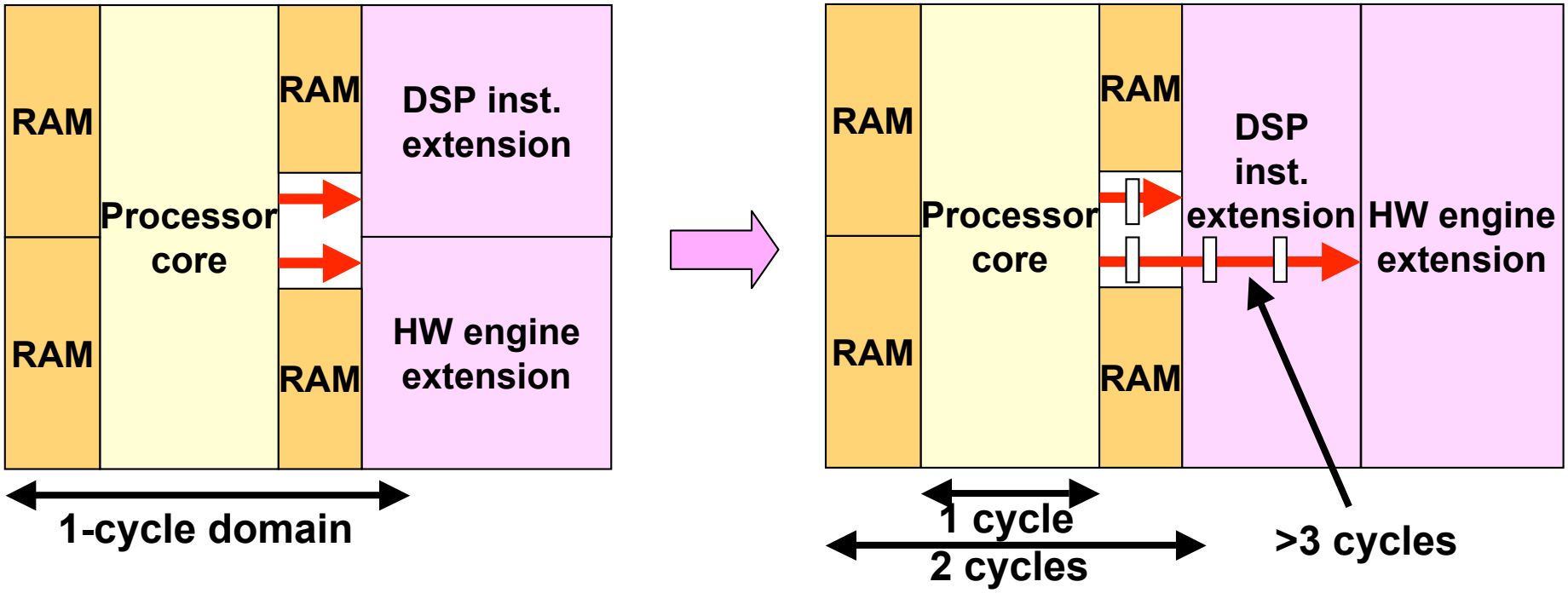
Extension I/F Latency

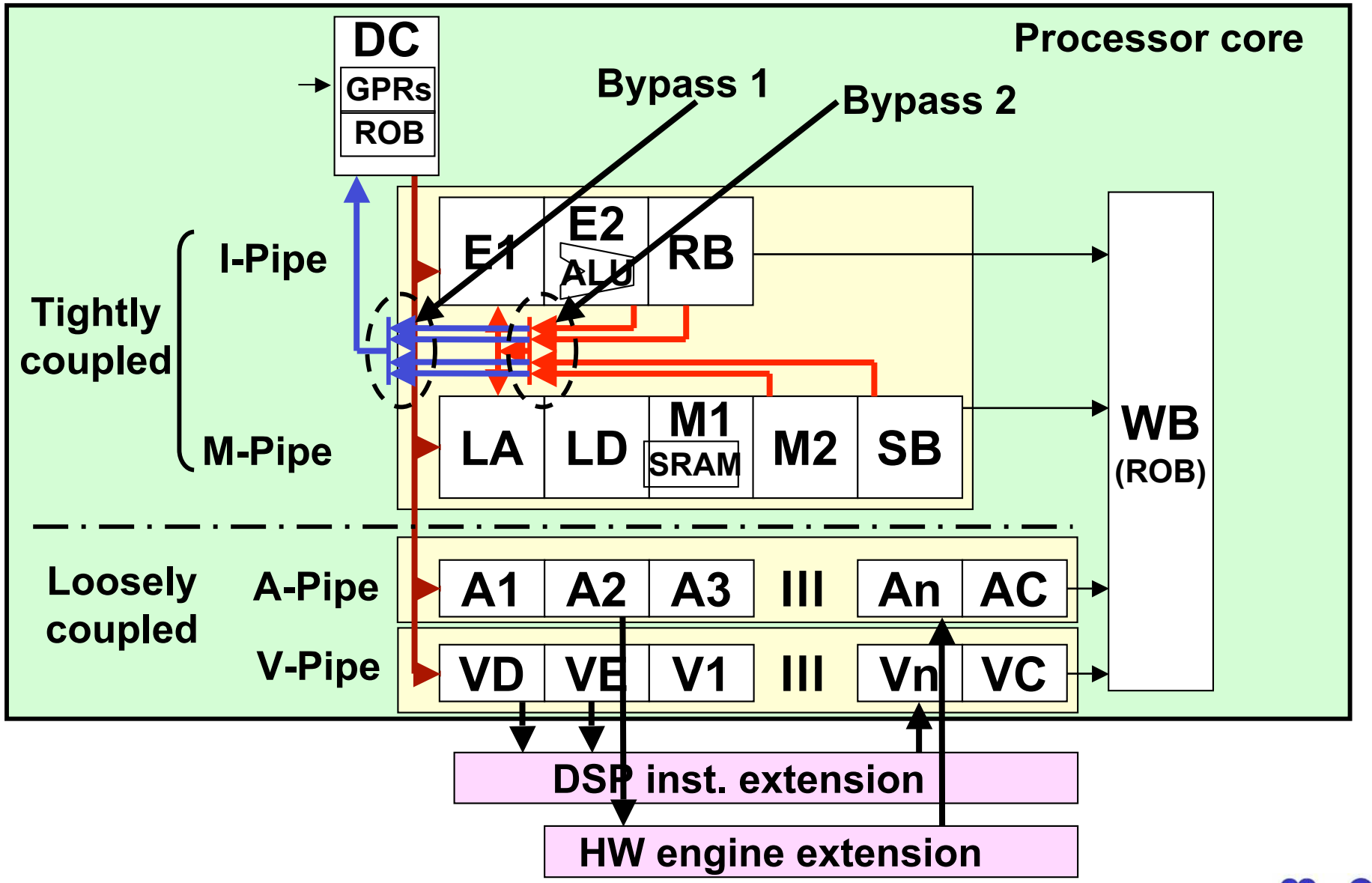
- MeP-c3
  - ex. 350-400MHz@90nm
- MeP-h1
  - ex.1GHz@65nm



→ Tightly coupled extensions

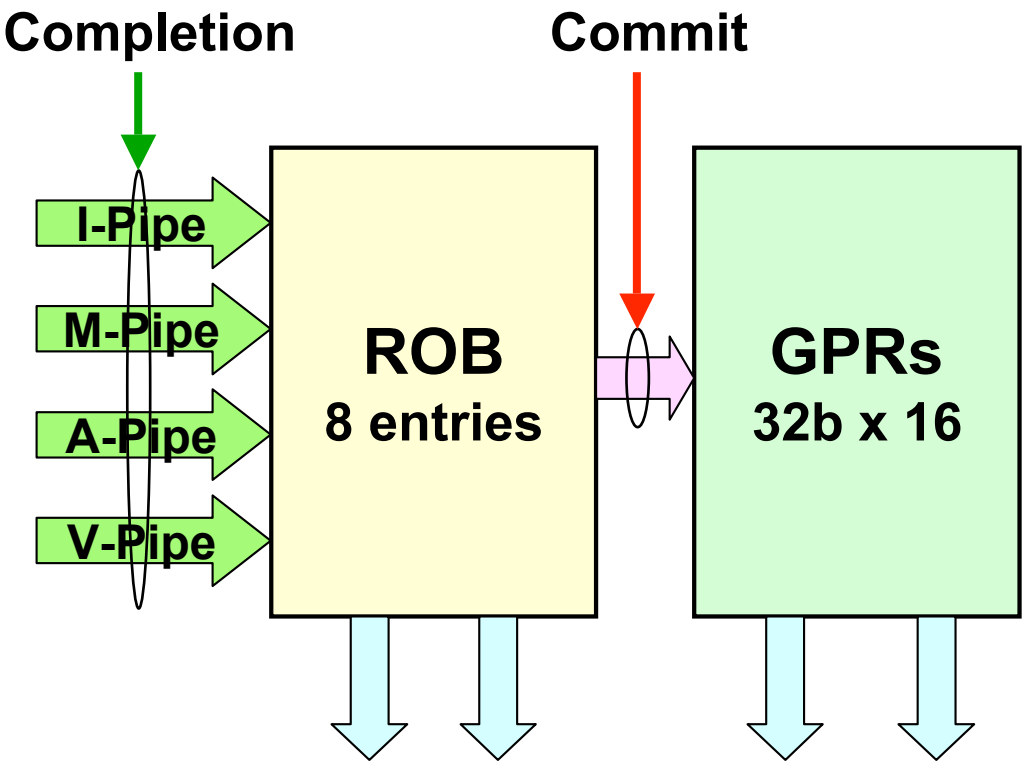
→ Loosely coupled extensions

Tightly / Loosely Coupled Pipelines

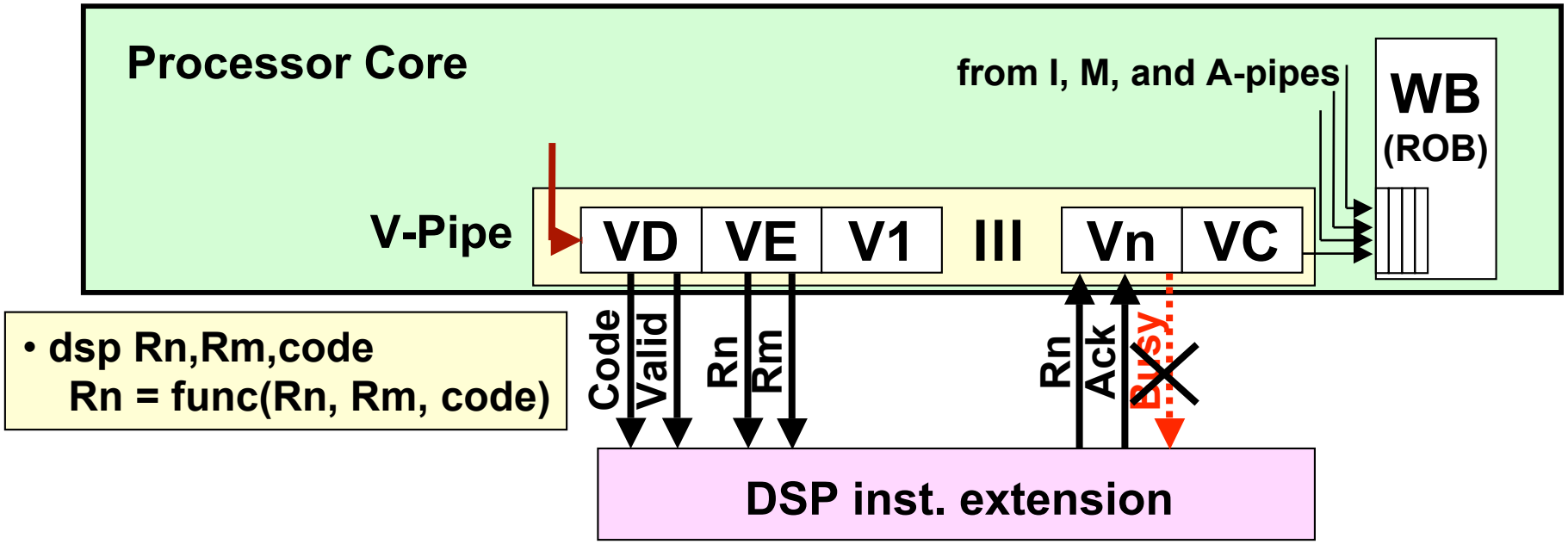


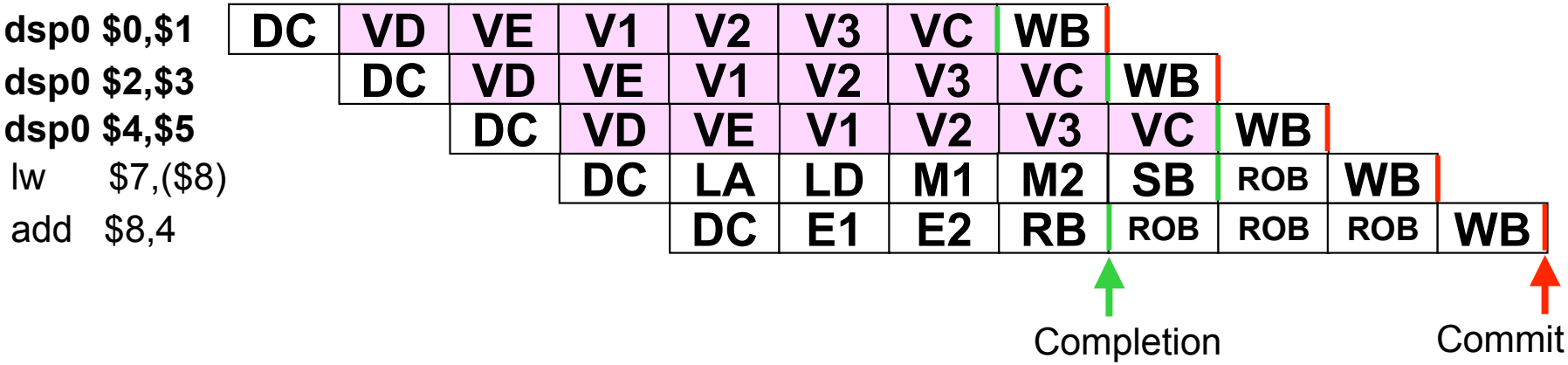
Structure of ROB and GPR

- **ROB** (Reorder buffer)
  - 8 entries
  - 4 write ports
  - 3 read ports
- **GPRs**
  - 32 bits x 16 words
  - 1 write port
  - 2 read ports



DSP Extension Interface





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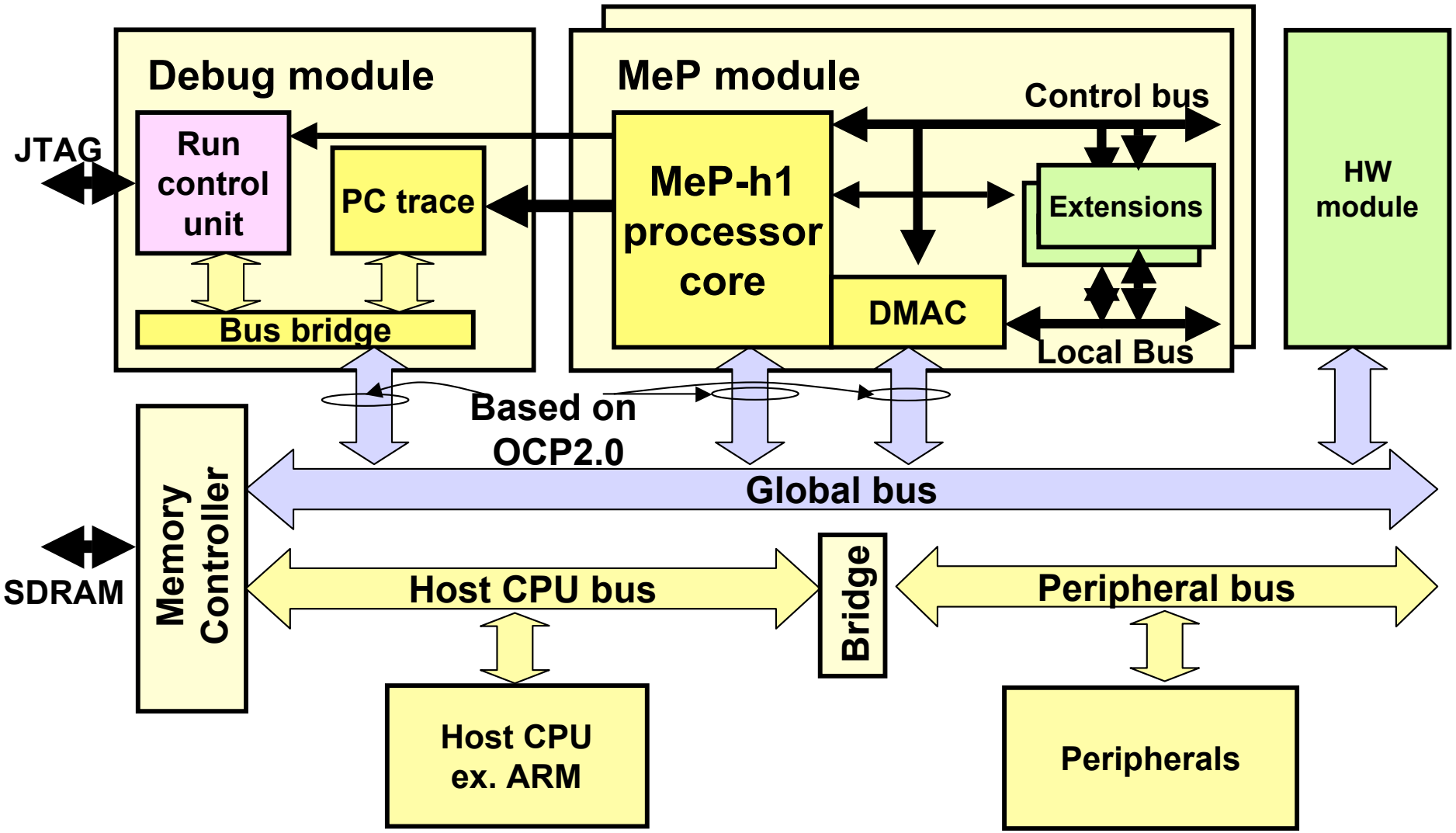
SoC Architecture



MeP Media embedded Processor

Bus Interface

- Based on OCP* 2.0 Protocol
  - Split bus transaction
  - Single request burst
  - Posted write
  - Pipelined request and response
    - 2 outstanding requests
  - Master bus reset and slave bus reset

*) OCP : Open Core

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Configurations

- Configurations

I$:	8KB, direct-mapped
I-RAM:	4KB
D$:	8KB, direct-mapped
D-RAM:	4KB
Bus width:	64 bits

Debug function:

Hardware breakpoints,
Single step
PC trace(8KB trace memory), etc.

- Extensions

DSP instruction extension
4 hardware engines

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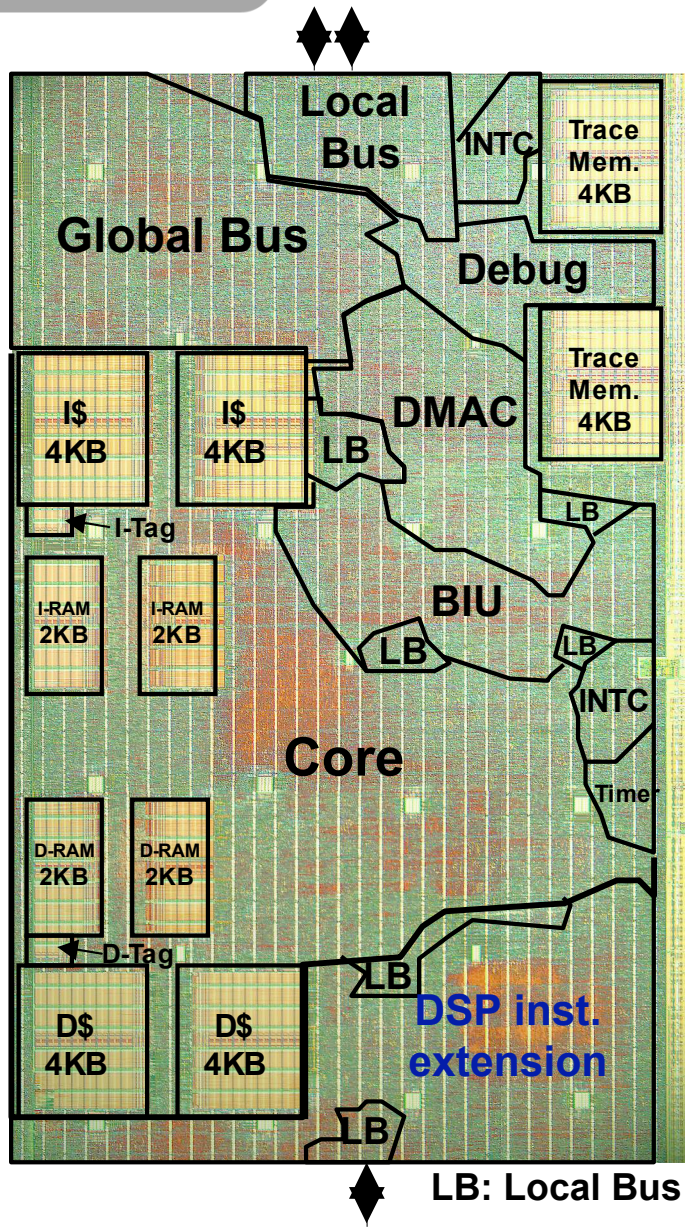
First Implementation

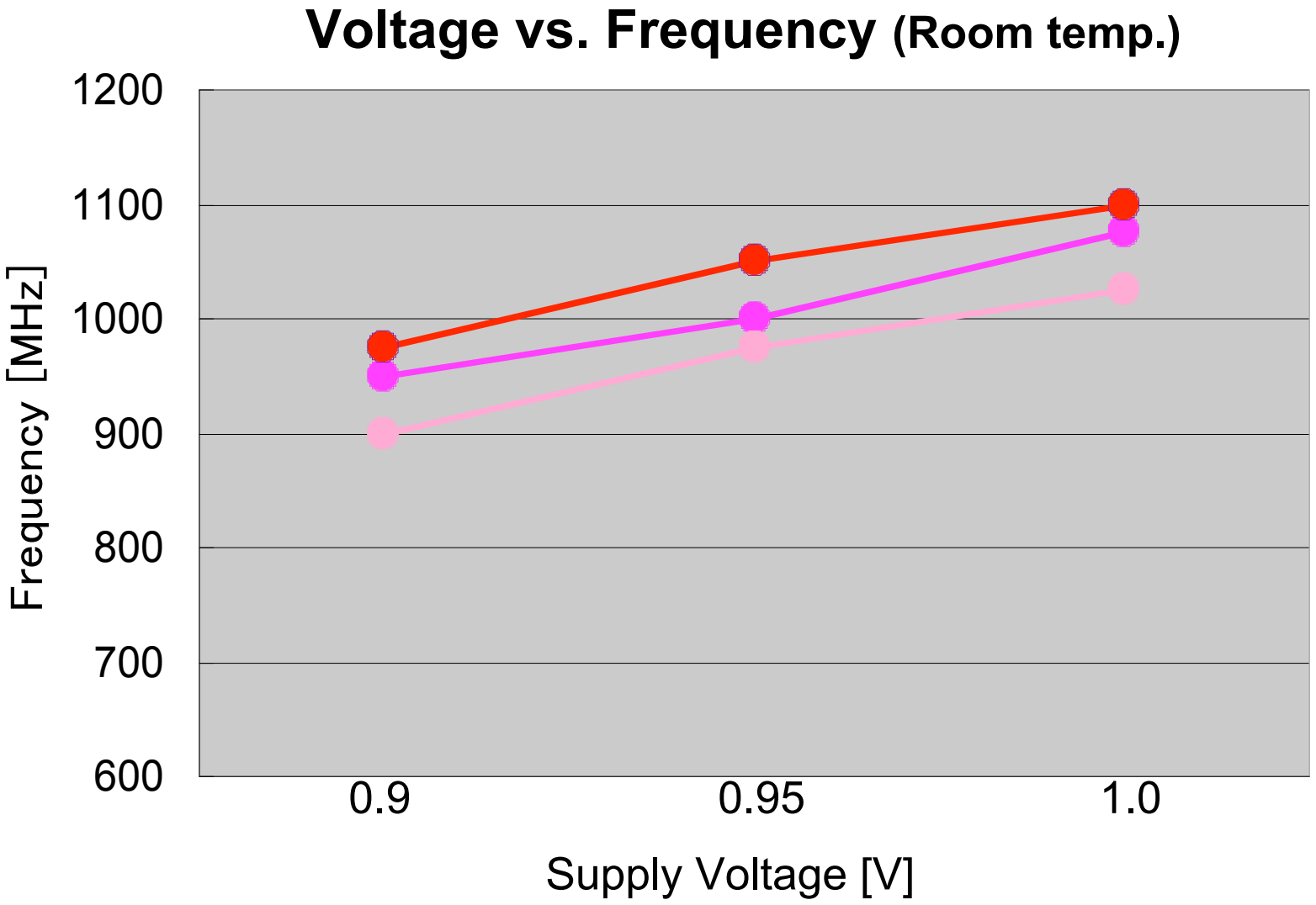


- Toshiba 65nm CMOS process
- Size: 1.58 mm x 2.96 mm
- Gate counts : 250K gates (core only)
- Power consumption*
  about 1W @ 1GHz, w/o clock gating
  *) estimated by total of Tr. sizes and wire loads.
- Static Timing Analysis result

Clock margin	= 80 ps
Critical path delay	= 918 ps
Total	= 998 ps →*1GHz*

MeP Media embedded Processor

Lab. Result


Voltage vs. Frequency (Room temp.)
1200
1100
1000
900
800
700
600
Frequency [MHz]
0.9
0.95
1.0
Supply Voltage [V]

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Conclusion

- Configurable processor aims to high performance & high operating frequency
- Pipeline design
  - Deeper pipeline stages
  - Branch predecode and prefetch
  - Relaxed local memory (SRAM) timing
  - Loosely coupled extensions using ROB
- First implementation
  - Fabricated by 65nm CMOS and can operate at 1GHz

Thank you!