Low-Power, Networked MIMD Processor for Particle Physics

Outline

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- The MIMD Processor
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- Summary

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Introduction to High Energy Physics

- The following slides give a brief overview of the scientific environment of the application for the MIMD Processor
- One goal of the experiments under construction is the generation of a quark/gluon plasma, which can only be created by colliding nuclei at very high kinetic energies
- The following slides show a schematic overview of an appropriate experiment, capable of detecting the reaction products of such collisions
- The photo shows the experiment at its current state. It is scheduled to take first experimental data in Q2 2007



Top

Big Bang. Now they are found only in cosmic rays and accelerators

Force

These

four

particles

particles

transmit the

fundamental forces of nature although

gravitons

have so far not been discovered

Tau in 1975

Gluons

Carriers of the

between quarks

strong force

Heavier still; it is extremely unstable. It was discovered

Tau neutrino believed to exist

Photons

force

force

Particles that

make up light;

they carry the

electromagnetic

not yet discovered but

elt by:

Electricity, magnetism and chemistry

are all the results of electro-magnetic

quarks and charged leptons

Heavier still Intermediate vector bosons

Carriers of the weak force Felt by: quarks and leptons

Some forms of radio-activity are the result of the weak force



Bottom

Heavier still; measuring

bottom quarks is an important

test of electroweak theory

All the weight we experience is the result of the gravitational force

Introduction to High Energy Physics

Felt by:

quarks

The explosive release of nuclear

energy is the result of the strong force

Introduction to High Energy Physics

LHC and the Geneva Area









Introduction to Triggers

Introduction to Triggers

- The large number of particles, created in every interaction and the statistical nature of the reaction on one hand and the large amounts of data, exceeding 10 TB/sec on the other hand require intelligent selection functionality, allowing to select the specific reactions, the experiment is looking for
- Such on-line selection functions, trigger the readout and archival of the data associated to a given event and are therefore called triggers
- Triggers can be classified according to the event size and event rate they are capable of processing



Introduction to Triggers

Existing and planned Trigger Systems

Exp.	Acc.	Trigger	Physics Signature	Selectivity	Channels #	(Inp)Event Rate	Processing Time	Event Size	URL
ALICE	LHC	0-2	MinBias Dimuon	1/A	π	N 12	μο	ND	
	20	TRD	Pt, transition radiation	1000	1200	150	6	30 MB	www.kip.uni-hd.de/TRD
		HLT	-,						
LHCb	LHC	L0 (HW)	Et, Pt, Ninter, Ntracks	10		10000	4		hcb.web.cem.ch/hcb/
		L1 (PC farm)	large ImpPar, high Pt	25	170k	1000	<1 ms>	5 kB	
		HLT (PC farm)	B selection	80		40	<50 ms	50 kB	
ATLAS	LHC	L1 (HW)	Calorimeter + Muon	900	7k + 800k	40000	<2.5		atlas.web.cern.ch/Atlas/Welcome.html
		L2	Rol in all detectors	35		75	<10 ms	30 kB	
		L3 (Event Filter)	Full event reco	10		2	~1 s	1.5 MB	
CMS	LHC	L1 (HW)	Cal., Muon	400		40 MHz	<3.8		cmsinfo.cern.ch/Welcome.html/
		HLT (PC farm)	All detectors	1000		100 kHz			
H1	HERA	L1 (HW)	Vertex, Cal, Muon	300000		10 MHz	<2.3		www-h1.desy.de/
		L2 (HW)	Correlation (ANN)	1		30 Hz	20		
		L3 (RISC, Event Filter)		3		30 Hz	<0.8 ms		
		L4 PC Full reco		3		10 Hz	100 ms		
ZEUS	HERA	FLT (HW)	Global properties	20000		10 MHz	~0.7		www-zeus.desy.de/
		SLT (INMOS transputers)	Regions	10		500 Hz	10 ms		
		TLT (Farm)	Full data	10		50 Hz	none		
HERA-B	HERA	FLT HW (Rol)	Muon, ECAL, track	200		10 MHz	_10		www.hera-b.desy.de
		SLIPC (Rol) Vertex	Sec. Vertex (Rol)	100		50 kHz	7 ms		
		ILI PC Vertex	Sec. Vertex	10		500 Hz	100 ms	450 10	
DUENUV			Event selection	~2.5	0501	50 HZ	4 S	150 KB	and the second second second
PHENIX	RHIC			. 0	~350K	TUKHZ/TUMHZ		400 10	www.pnenix.bni.gov/
OTAD				>0			4 5	100 KB	and the balance of
SIAR	RHIC		CTB, ZDC, MWYPC			10 MHZ	~1.5		www.star.dni.gov/
							~100		
		L_2 (HVV)				5 LI-	~200 m		
PHOROS			Deddle counter		1504104	200 H-	~200 116		www.phohoo.hpl.cov/
FIIODOS	RHIC		Choronkov onto ZDC		150K+2K	200 112			www.phobos.bhi.gov
BRAHMS	RHIC			10	~4k	~1 2 kHz			www.4 rcf.bpl.gov/brabms/W/W/W/
Browning	14110	11	200, 000	10	ЧК				www.a.ioi.biii.gov/biaiiiib/vvvv/
D0	FNAL	L1 (HW)	Fiber tracker (Pt)	1500	~1000k	7.6 MHz	~2.5		www-d0.fnal.gov/
		L2 (HW)	Silicon Track Trigger	5		5 kHz			
		L3 (PC farm)	Full data	20		1 kHz		250 kB	
CDF	FNAL	L1 (HW)	Calo, Muon, Track	150		7.6 MHz	~5.5		www-cdf.fnal.gov/
		L2 (HW)	Calo, Muon, Track	150		50 kHz	20		
		L3 (SW)	On-line reco	4		300 Hz		200 kB	
BTeV	FNAL	L1 (500 FPGA+2500 DSP)	Detached vertex	100	30M	7.6 MHz	330	200 kB	www-btev.fnal.gov/
		L2/3 (2500 PC Linux farm)		~20		4 kHz (out)	300 ms	100 kB	-

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Introduction to Triggers



ALICE TRD Trigger Architecture

- The Transition Radiation Trigger is built to select high energy electron/positron pairs, which are created very rarely in the center of the quark gluon plasma
- The over all architecture is a cylindrical detector around the interaction vertex, where all particle trajectories are searched for very stiff tracks.
- The following slides show the resulting electronics chain and on-line processing functionality
- The very tight time budget is sketched in the timeline

QGP Simulation (a) 37 fm/c = 1.2•10⁻²²s after interaction





<5% of central collisions contain e+/e- pair

ALICE TRD Trigger Architecture

Transition Radiation Detector - TRD



ALICE TRD Trigger Architecture

TRD Electronics Chain



Tracklet Fit (Tracklet Preprocessor)



During Drift Time:

N = hit count $y_i = position$ $\sum x_i = \text{time bin sum}$ $\sum y_i = position sum$ $\sum x_i y_i = \text{time bin*position sum}$ $\sum y_i^2 = \text{position}^2 \text{ sum}$



ALICE TRD Trigger Architecture 3 T6 **ALICE TRD Trigger Timing** S 75 2 T plane projection electronics electronics amplification ampification + + + + drift drift 3 N radiator radiator 0 T ö TR ö **Global Tracking** Data ship Calculate² fit **Calculate Tracklets** drift pipelineADC output visible drift area drift t 240 5990 Tracklet Tracklet Tracklet Tracklet PASA ADC ⊢ TRD Preprocessor ≁ Preprocessor -➡ GTU ┢ Merger Processor TPP TPP TP ТМ event buffer event buffer

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The MIMD Processor

- All required processing is done on the detector in the active area of the experiment, making material budget, power and radiation tolerance essential requirements
- The following slides outline the most important building blocks, like the ADC, digital filters, multi port memory, etc
- The MIMD architecture is outlined. Four CPUs communicate via a global register file and a global quad port memory. In addition each individual processor interfaces to the fitting preprocessor via a private register file, allowing the preprocessor to project its results directly into the processors register file
- The readout of the 260000 processors is performed using a parallel high-speed push architecture
- The last slide in this section is a die photo with an outline of the different functional regions. The chip is in production. So far 30 wafers have been produced in the UMC 180 nm process.

ALICE TRD MCM



80 120 140 200 CODE of ADC Diff. Input Signa 0.6 0,3 0.2 0. 2.0µ 3.0µ 4.0µ 5.0µ 1.0µ 6.0µ 17

- Deep submicron UMC180nm
- Concurrent operation of 4 120 MHz RISC processors and 21 10-Bit low-power ADCs @9.5 ENOB
- PASA and digitizing/processing chip on same MCM
- Very low cost

ADC



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TRAP – Digital Filter



TRAP – Tracklet Preprocessor



The MIMD Architecture



- ◆ Four RISC HARVARD CPU's
- Coupled by Registers (GRF) and Quad ported data Memory
- Register coupling to the Preprocessor
- Global bus for Periphery
 - Local busses for Communication, Event Buffer
 - read and direct ADC read
- I-MEM: 4 single ported SRAMs
- Serial Interface for Configuration
- IRQ Controller for each CPU
- Counter/Timer/PsRG for each
 CPU and one on the global bus
- Low power design, CPU clocks gated individually

Quad Port Memory

Features

- four independent bidirectional and synchronous ports
- designed for 120 MHz
- Area one bit cell: 5,08 * 4,86 μm
- Overall area less then: 1900 * 800 µm (1024 words with 32+7 bits)





Tracklet Track Trigger (Tracklet Merger)



Programming Model

- Available processing time is 1µs / 120 instructions
- All programming in assembler
- MIMD simulator developed for software development and performance benchmarking
- Initialization and control of the 250000 processors in 65000 chips is performed by 540 single board linux computers, integrated on the detectors





ALICE TRD Global Tracking Unit



- glob al tracking is performed module wise (540 modules).
- input of one GTU are 6*2 2.5GBd optical fiber channel links which are converted into 6*2 16Bit/120Mhz data streams.
- readout order of individual chambers are optimized for histogramming and pattern recognition in parallel.
- histogramming engine fills a data field with tracklet candidates regarding their position.
- looking for patterns with
 - a cluster of at least 4 candidates
 - adequate similar angle
 - high momentum
 - adequate quality
- quality and position of found hit is sent to central trigger processor
- GTU operates also for raw data readout and compression

Tests and Measurements

Tests and Measurements

- The following slides show the integration of the MIMD processor chip with a preamplifier on a multi-chip module, the integration of these MCMs on readout boards and their integration on the chambers.
- A setup of one detector stack in a real beam experiment is shown next. The final detector will encompass 90 stacks.
- The measurement of a particle track, measured by the Processors is shown next. The correct functionality is successfully verified.

Tests and Measurements

Putting things together

MCM = Preamp+TRAP TRAcklet Processor (TRAP) - 21 x 10 bit ADCs, digital filters, 4 RISC CPUs, fast readout

Configuration SBC Trigger & clock distribution, ARM CPU+FPGA, embedded Linux, Ethernet, serial link to the CPUs





Tests and Measurements

A TRD stack event



Summary, Conclusions

- The high processing and integration requirements result in the electronics being integrated with the detector
- The tight latency budget results in a MIMD architecture using multi port memories for communication and synchronization
- Iterative processing is performed by a preprocessor, projecting its results into a read-only part of each processors register file, avoiding load instructions
- All critical data structures and memories implement error correction to compensate for SEUs
- The processor with its complex periphery is fully functional in the system
- Next steps are the construction of the entire detector and the development of the control infrastructure

