40-GHz operation of a single-flux-quantum (SFQ) switch scheduler

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This work was supported by the New Energy and Industrial Technology Development Organization (NEDO) as Collaborative Research and Superconductors Network Device Project

A Symposium on High Performance Chips (HOT CHIPS 17) Aug. 14-16, 2005

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Agenda

- Introduction
- SFQ (single-flex-quantum) circuit technology
  - Device, circuit, and logic
- SFQ network switch application
  - Switch scheduler implementation
- High-speed test scheme
- Test results
- Future switch system image using SFQ technology
- Conclusions

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Introduction

Continuous traffic growth in the Internet

→ Large-capacity network switches (> *100Tbps)*

Bottlenecks of high-performance network switches:

- Switching fabric core → SFQ/Optical devices
- Chip I/O → Optical devices
- Buffering → High-speed and dense memory devices
- Scheduling — *Centralized processing*

SFQ (single-flux-quantum) circuit implementation

- ***High-speed logic operation***
- ***Low power consumption***

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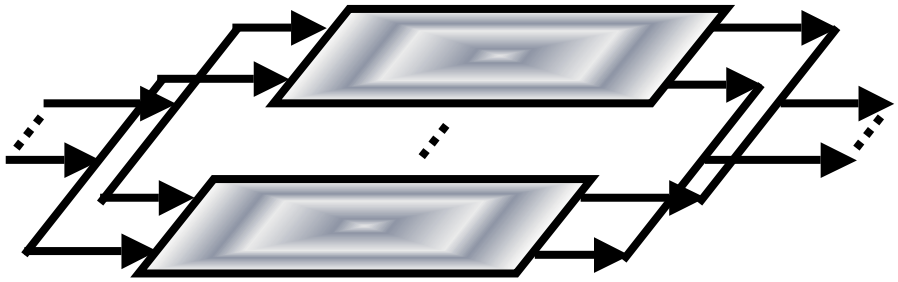
Comparison of SFQ with semiconductor

Semiconductor implementation



- Port speed **>** circuit speed
- Parallelized processing
- Multi-chip system
- Packaging limit
- Heat management

SFQ (Single-Flux-Quantum) implementation

- Port speed **=<** circuit speed
- Centralized processing
- Single-chip system
- Dense packaging

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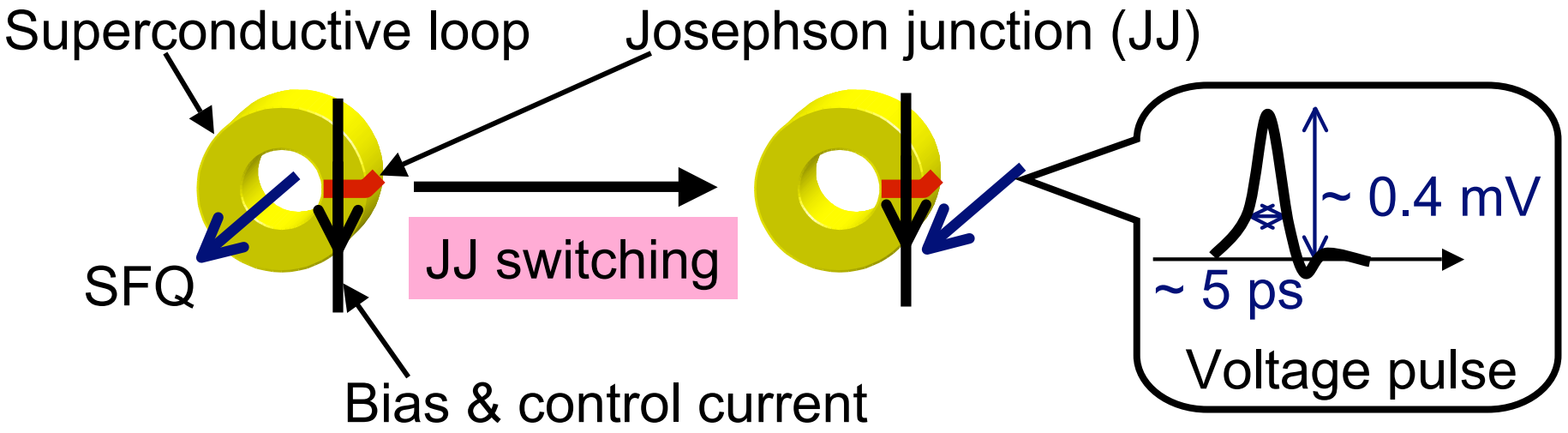
SFQ (single-flux-quantum) circuit technology



- Switching device: Josephson junction
- Quantized pulse signal
- Lossless pulse transmission on superconductive wires
- High speed: ~ 5 ps (2-μm design rule) (Scalable to the design rule)
- Low power: ~ 1 μW/gate

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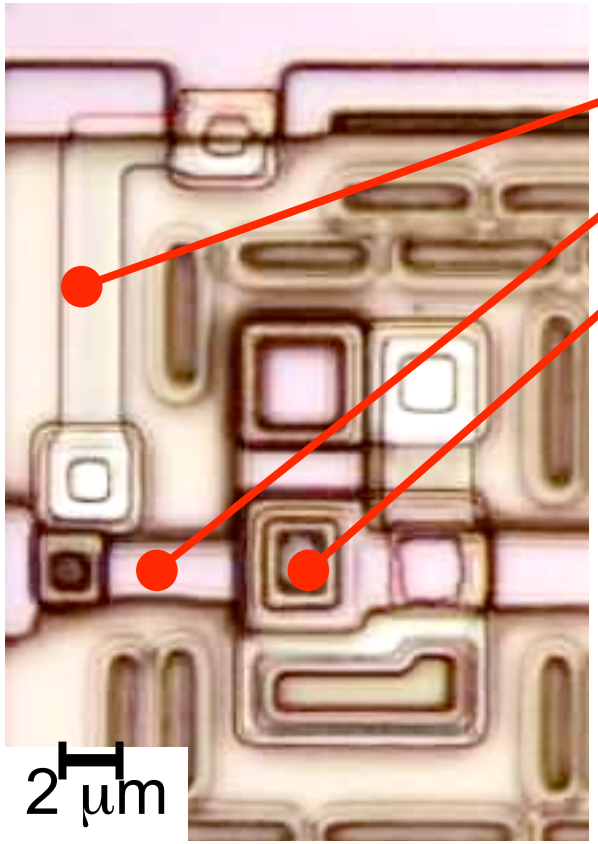
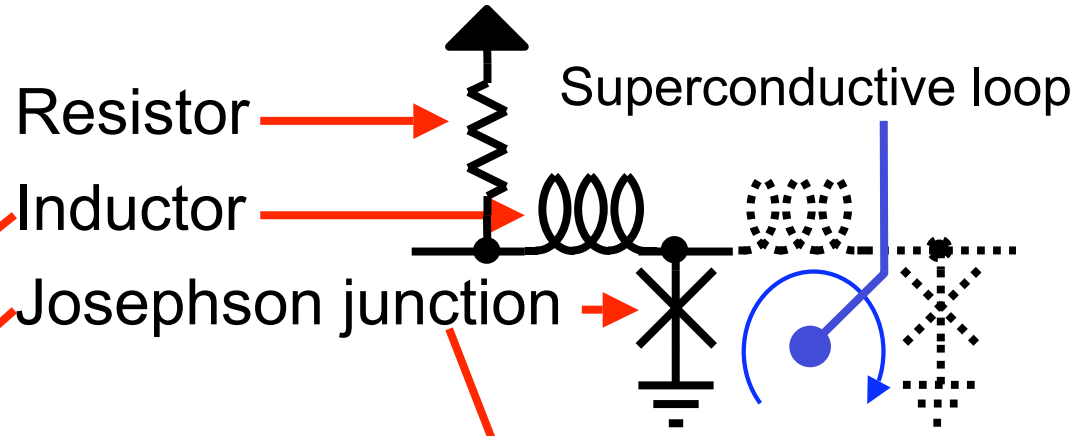
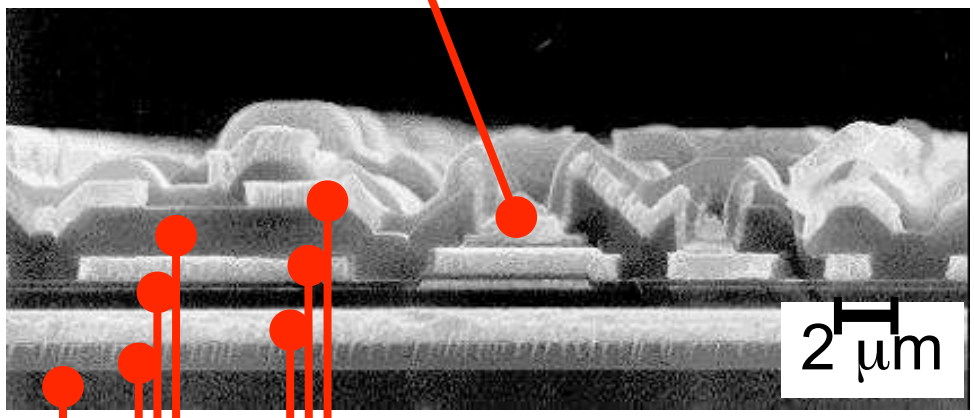
SFQ circuit and device structure







Nb (superconductor)
SiO_2 (insulator)
Si substrate

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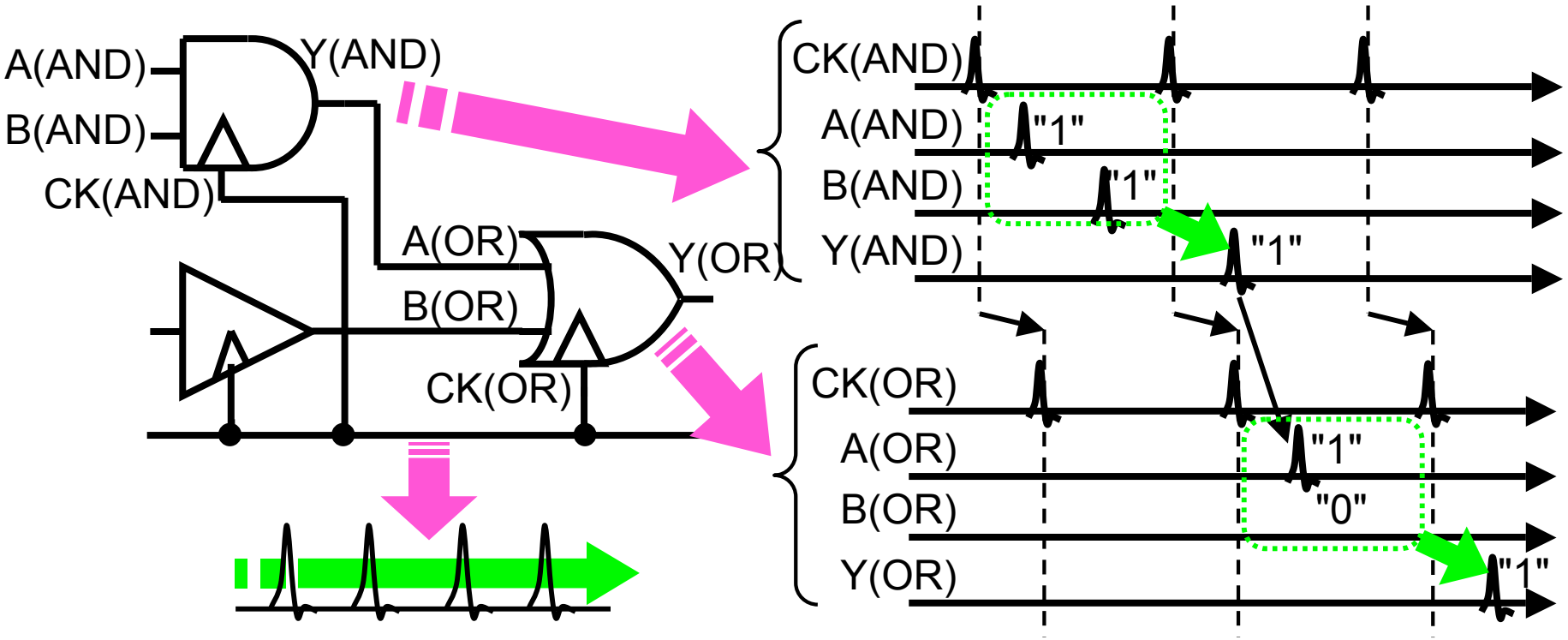
Pulse-driven logic



Multiple pulses can propagate on a superconductive wire.

➡ ***Wire pipelining***

Pulses are stored in logic gates and released by trigger pulses.

➡ ***Gate-level pipelining***

High-throughput operations

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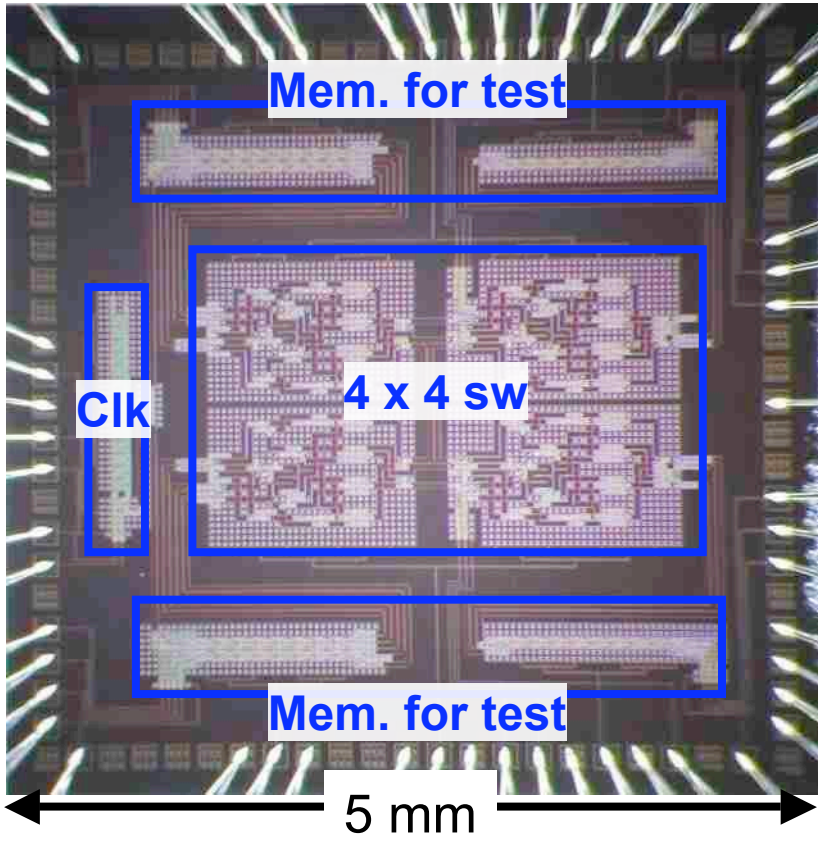
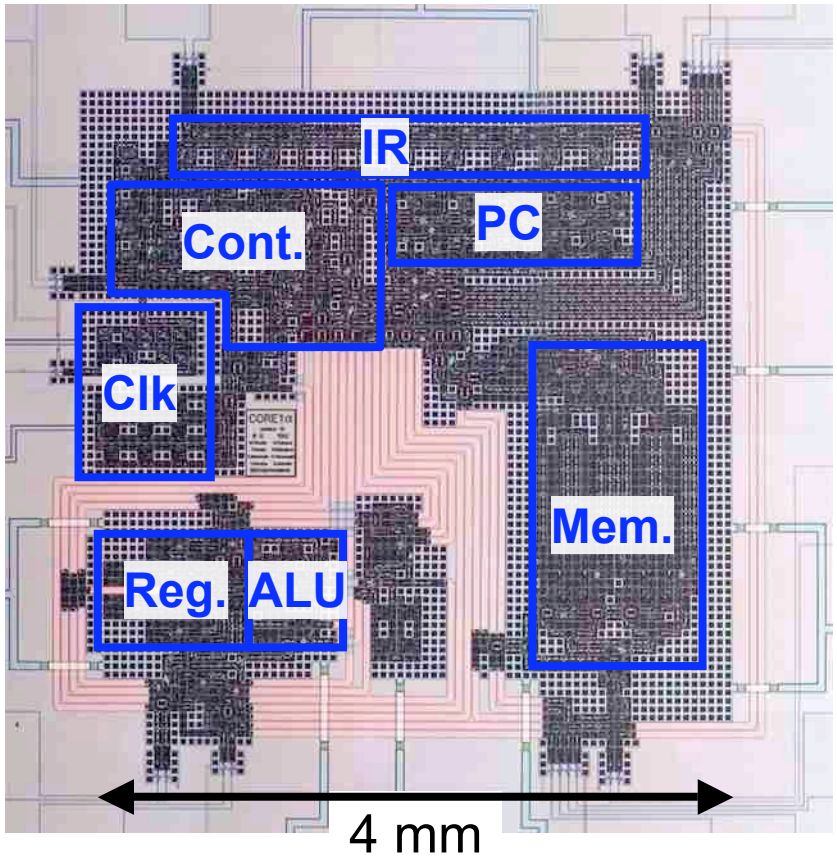
Related works





4 x 4 switch fabric test chip
- 160 Gbps operation
- 2812 JJ

4-bit SFQ processor
- 21 GHz operation
- 7220 JJ

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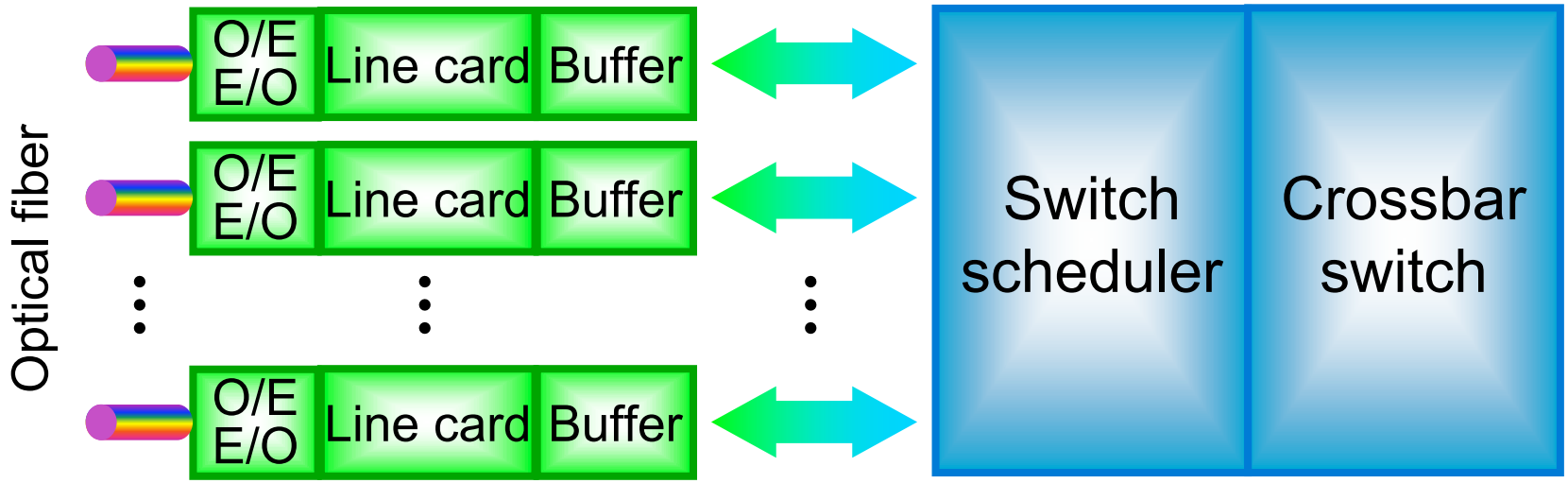
SFQ network switch application



Parallelized system

Centralized system

Semiconductor technology

- Parallel processing
- Optical interfaces
- Packet buffers

SFQ technology

- High-speed centralized processing
- High-throughput processing

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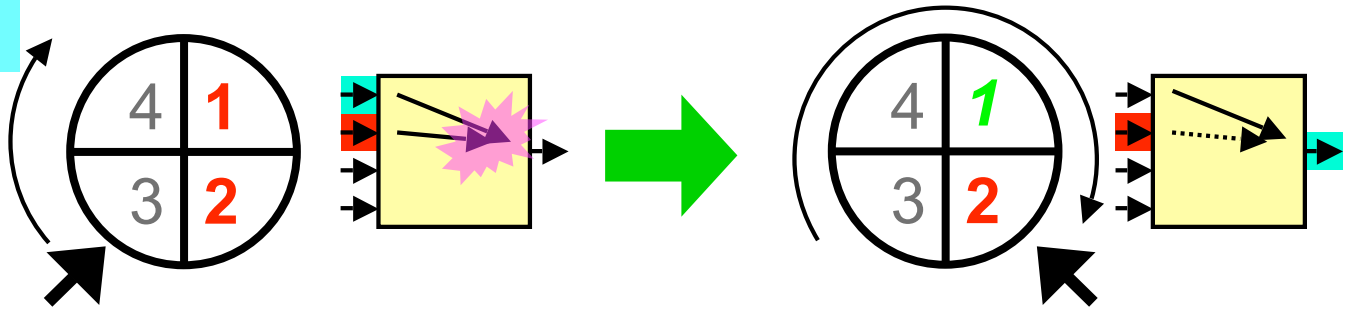
Switch scheduler functions

Objective: Resolving contentions in the crossbar switch.

Algorithm: Round-robin arbitration at each output.

1. Receiving requests.
2. Granting the first request starting from the round-robin priority pointer.
3. Updating the round-robin priority pointer.

Example



Requests = 1, 2
Priority pointer = 3

Grant = 1
Priority pointer = 2

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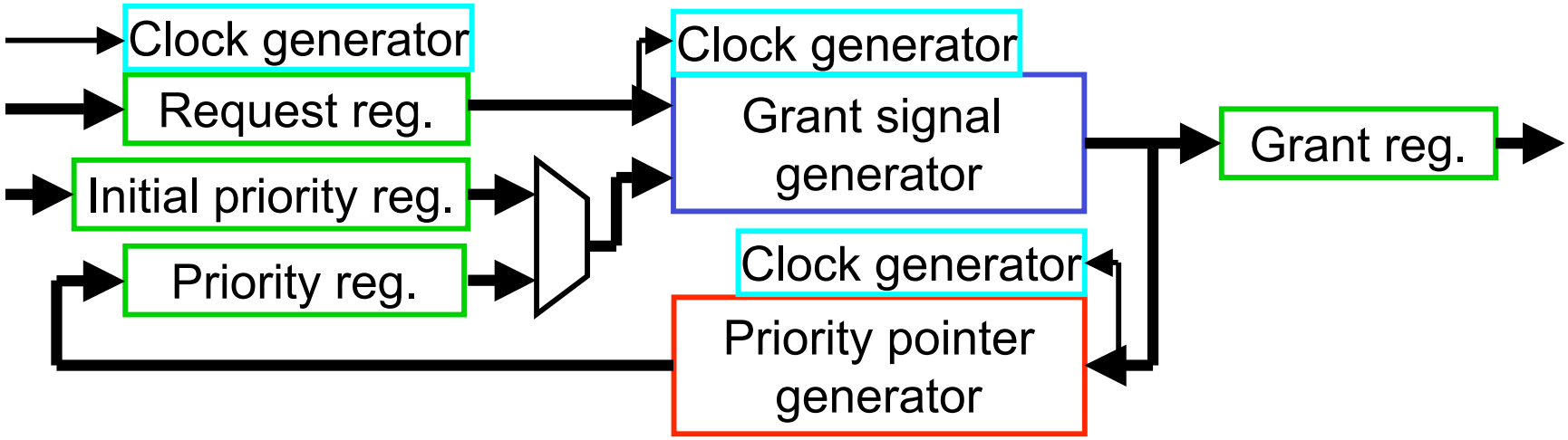
Switch scheduler block diagram



Architecture

- Asynchronous clocking with local clock generators (40 GHz).
- Wire pipelining and gate-level pipelining.
- Serial interfaces and processing.

Design

- Cell-based design using customized EDA tools.
- Extraction and modeling of bias-dependent cell timing.
- Gate-level static timing analysis.

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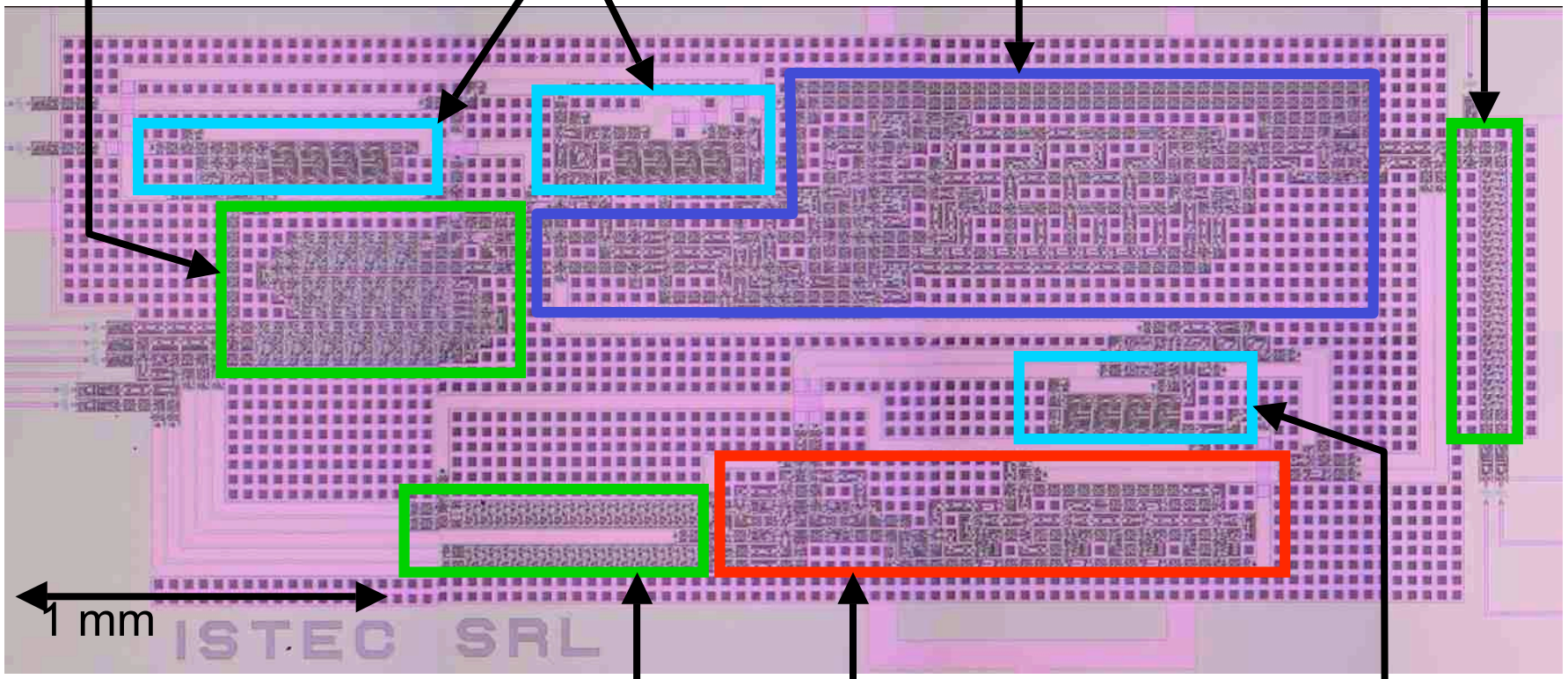
SFQ switch scheduler test chip



For 4 x 4 crossbar switch
Power: 920 μW
Josephson junction: 3071

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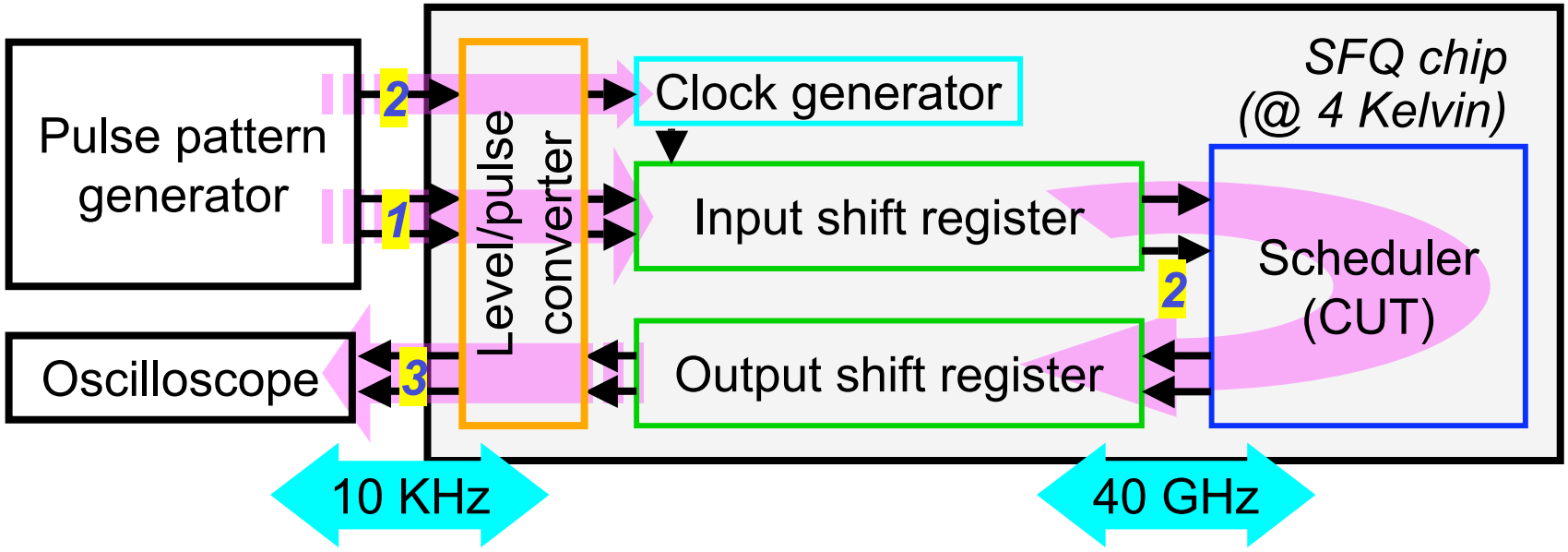
High-speed test scheme



Test procedure

1. Loading test patterns at 10 KHz.
2. Triggering the on-chip clock generator to start high-speed operation at 40 GHz.
3. Reading test results at 10 KHz.

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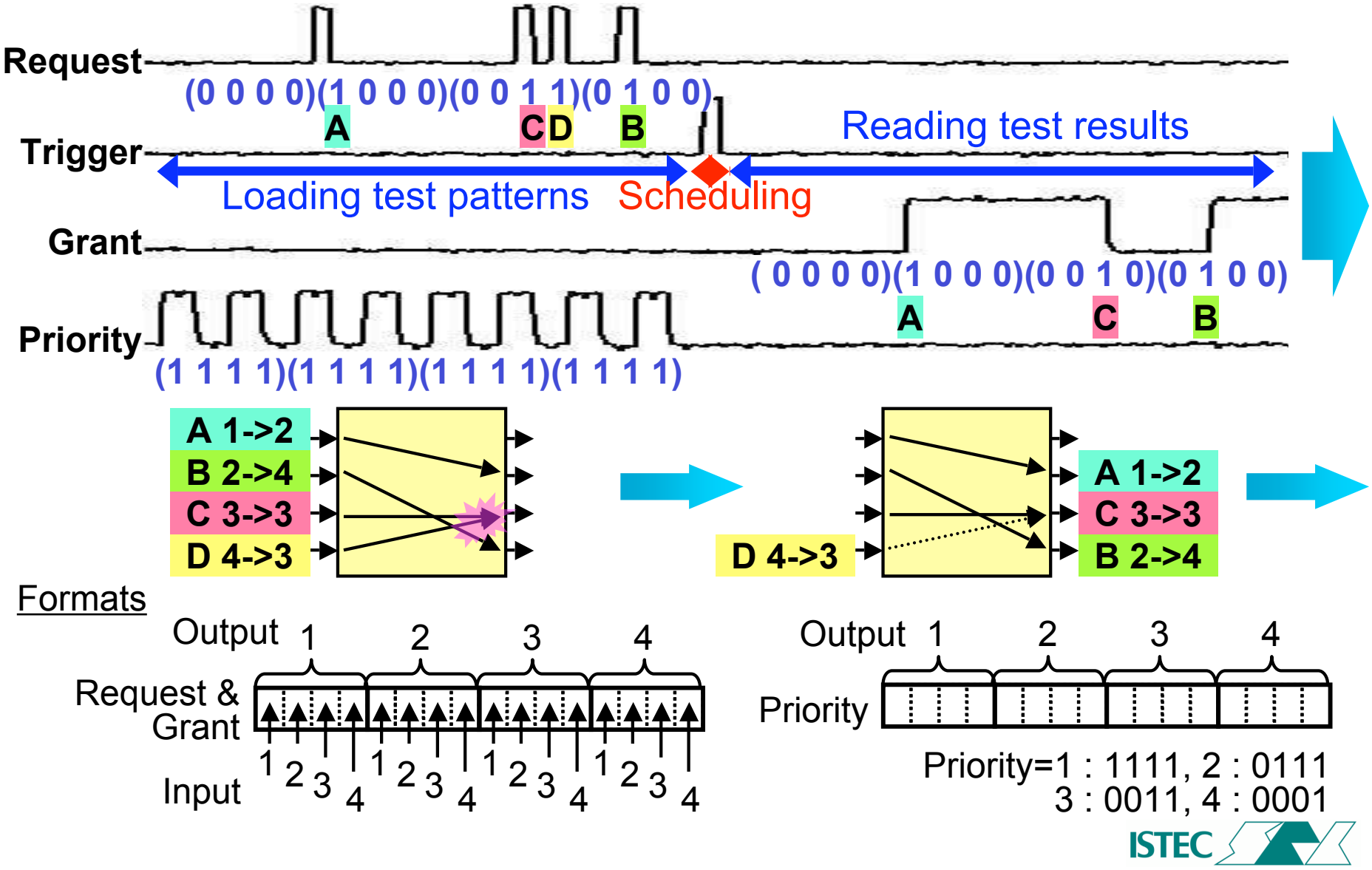
Test results (1)



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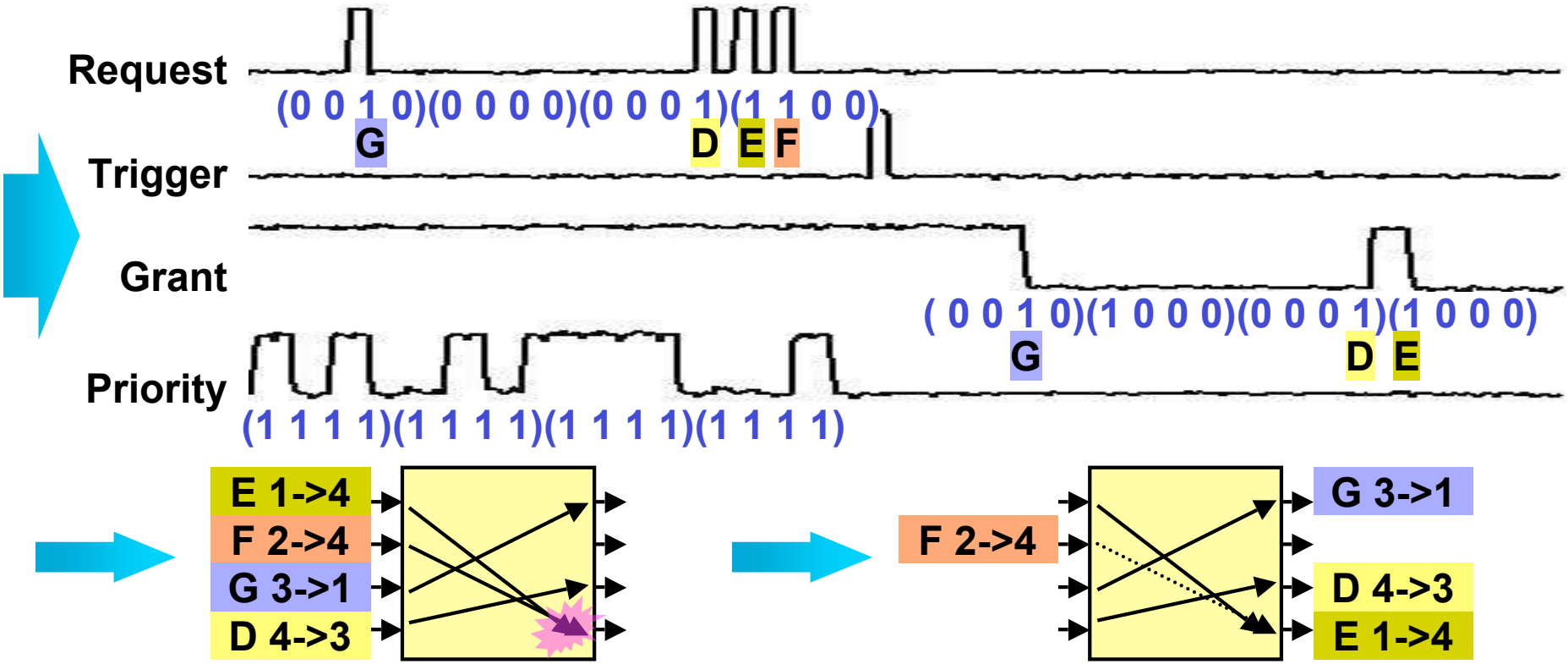
Test results (2)



Correct scheduling at 40 GHz

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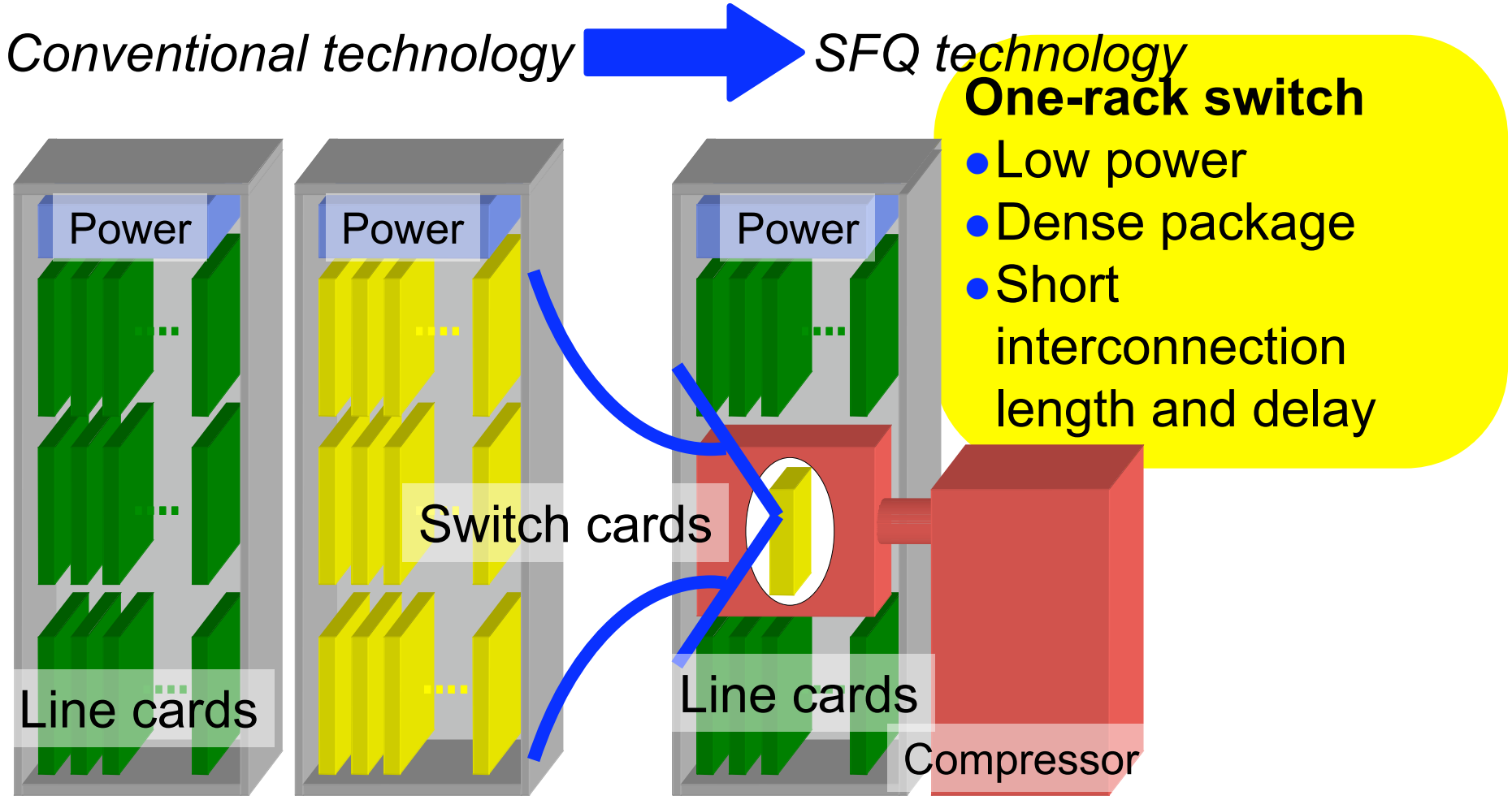
Future switch system image



Conclusions

- Advantages of SFQ circuit implementation
  - High-speed logic operation
  - Low power consumption
- SFQ switch scheduler design
  - Asynchronous clocking
  - Wire pipelining and gate-level pipelining
- 40-GHz scheduling confirmed by experimental test
- One-rack SFQ switch system in the future

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