

## Super Companion Chip with Audio Visual Interface for Cell Processor

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# Outline

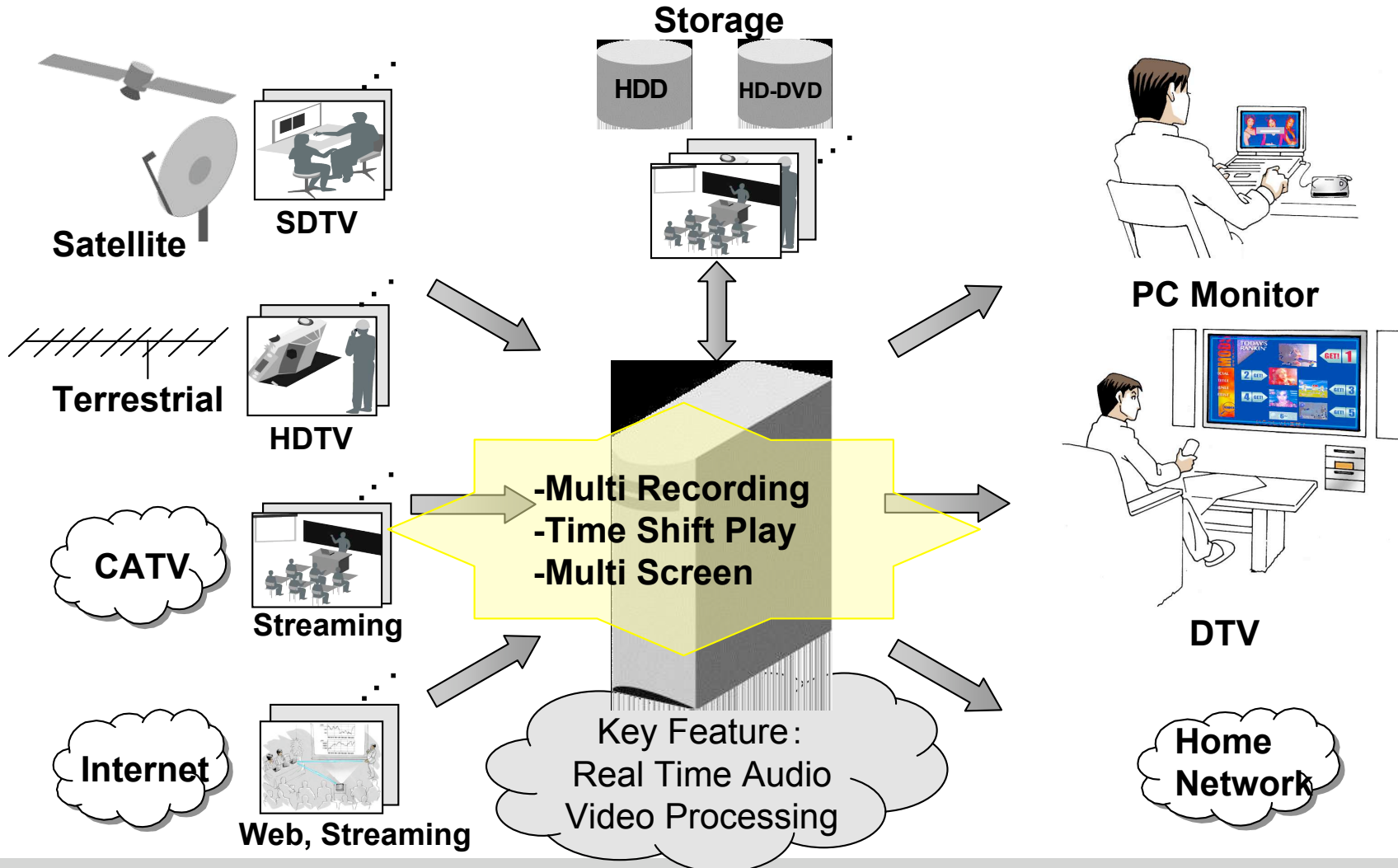
- **Background**
- What is Super Companion Chip(SCC)?
- Processing Flow
- SCC Architecture
- Technology and Chip Implementation
- Conclusion

# Motivation

- **To provide software based digital consumer solution for Cell processor such as Digital TV, Audio Visual Server, etc.**
- **To establish GHz high bandwidth connection between Cell and ultra high speed peripherals on Super Companion Chip (SCC).**

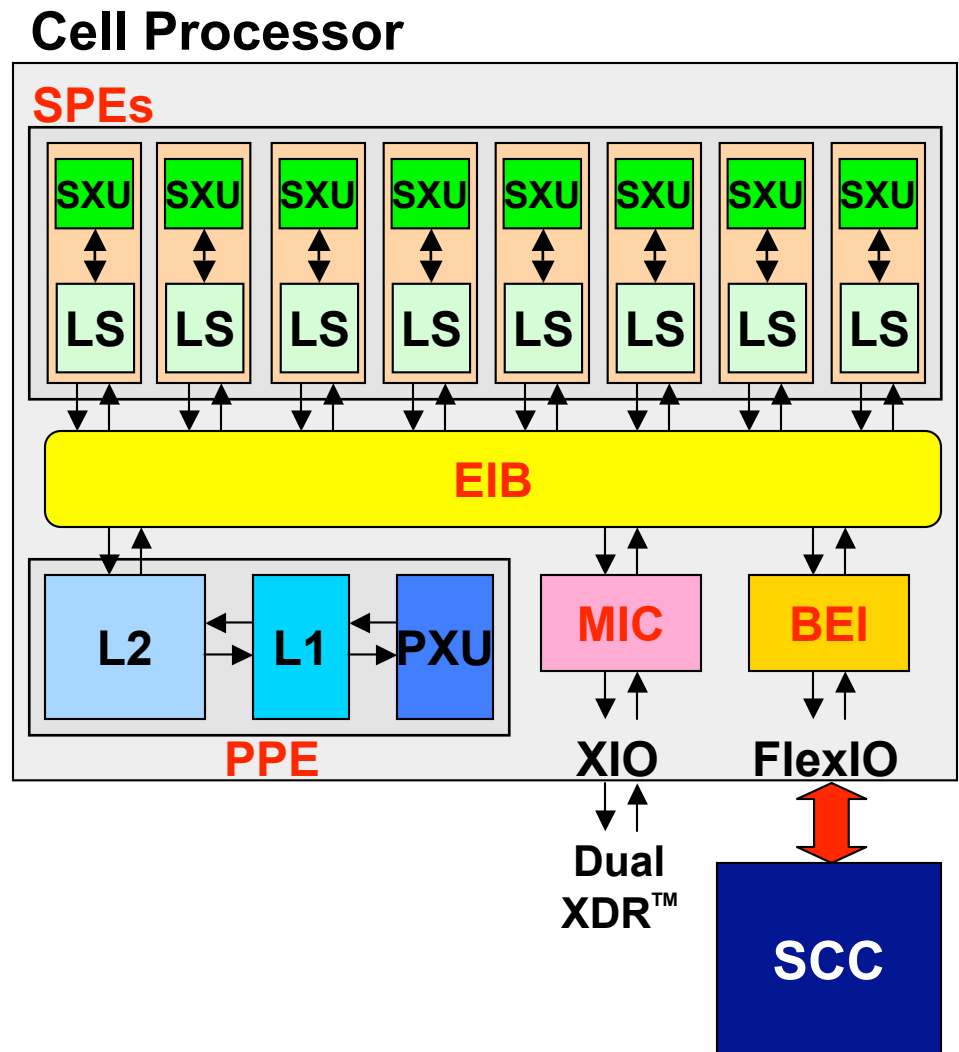
# Requirements from Market

- Multi Tasks Processing Simultaneously -



# Cell Processor Overview

- Power Processor Element (PPE)
- Synergistic Processor Element (SPE)
- Dual XDR DRAM channels
- Flexible I/O Interface
- Element Interconnect Bus



# Features of Cell Processor

## ■ Resource Management Capability

- Reserve Memory & I/O Bandwidth for up to four tasks.

## ■ Isolation Facility

- Each SPE is isolatable from outside for flexible secure programming.

## ■ Multi OS Support

- Run multiple OSs simultaneously.
  - ✓ e.g. Linux + Real-time OS

# Features of SCC

## ■ For Real Time Processing

SCC internal bus has the bandwidth reservation capability for the each resources.

-TDM arbitration

## ■ For Tight Security

The HW random number generator and several kinds of HW Encryption/Decryption functions are implemented.

## ■ For Multi OS Support

Every bus master module have the address space restriction mechanism.

To prevent the IO resource conflict between OSs.

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# SCC I/O Category

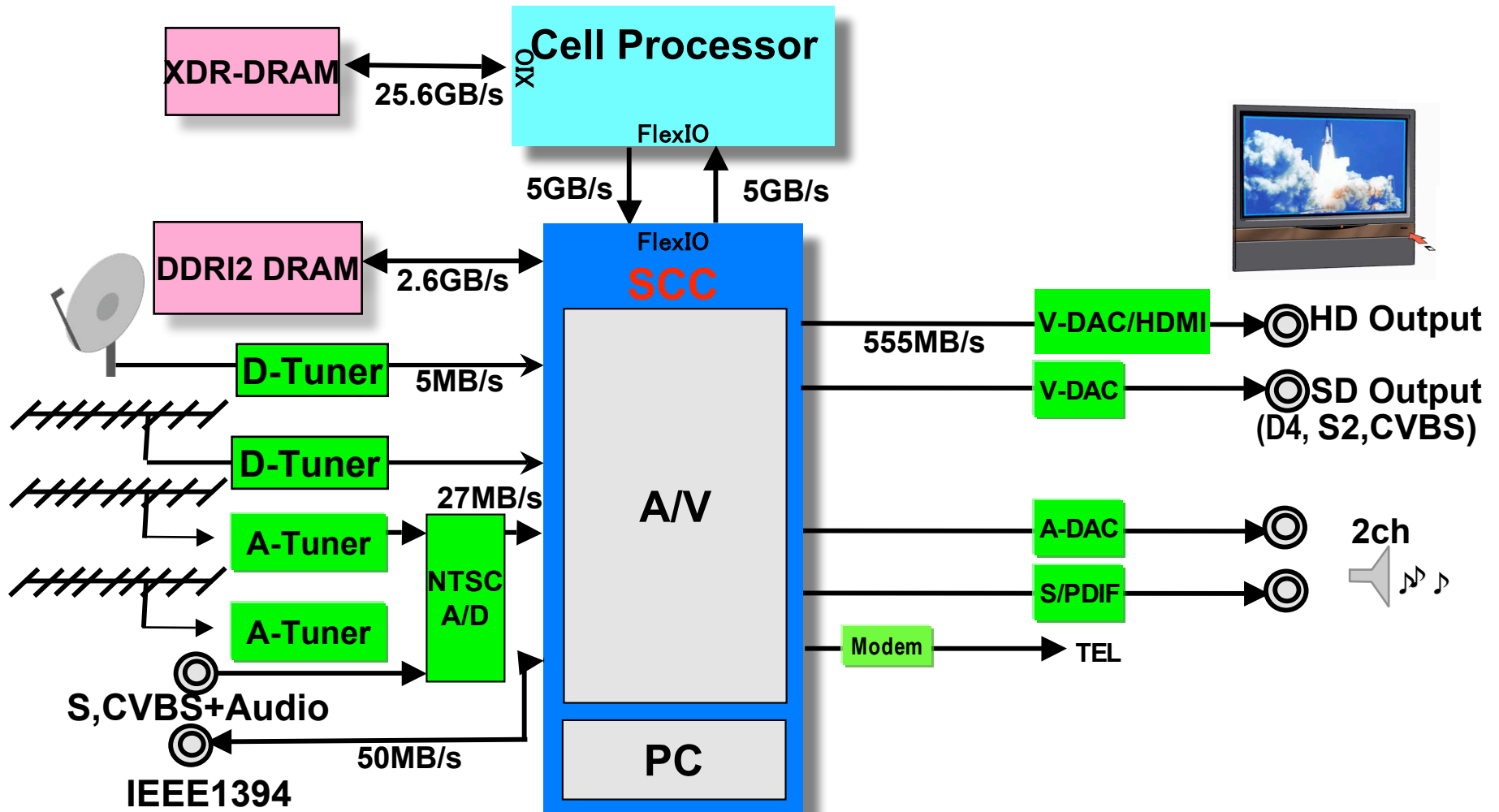
## ■ For versatile A/V system

- DDR2 DRAM I/F for Video RAM.
- Video output / Audio output.
- Video input / Audio input.
- Digital AV equipment connection I/F (IEEE1394).
- Digital tuner I/F (TS I/F).

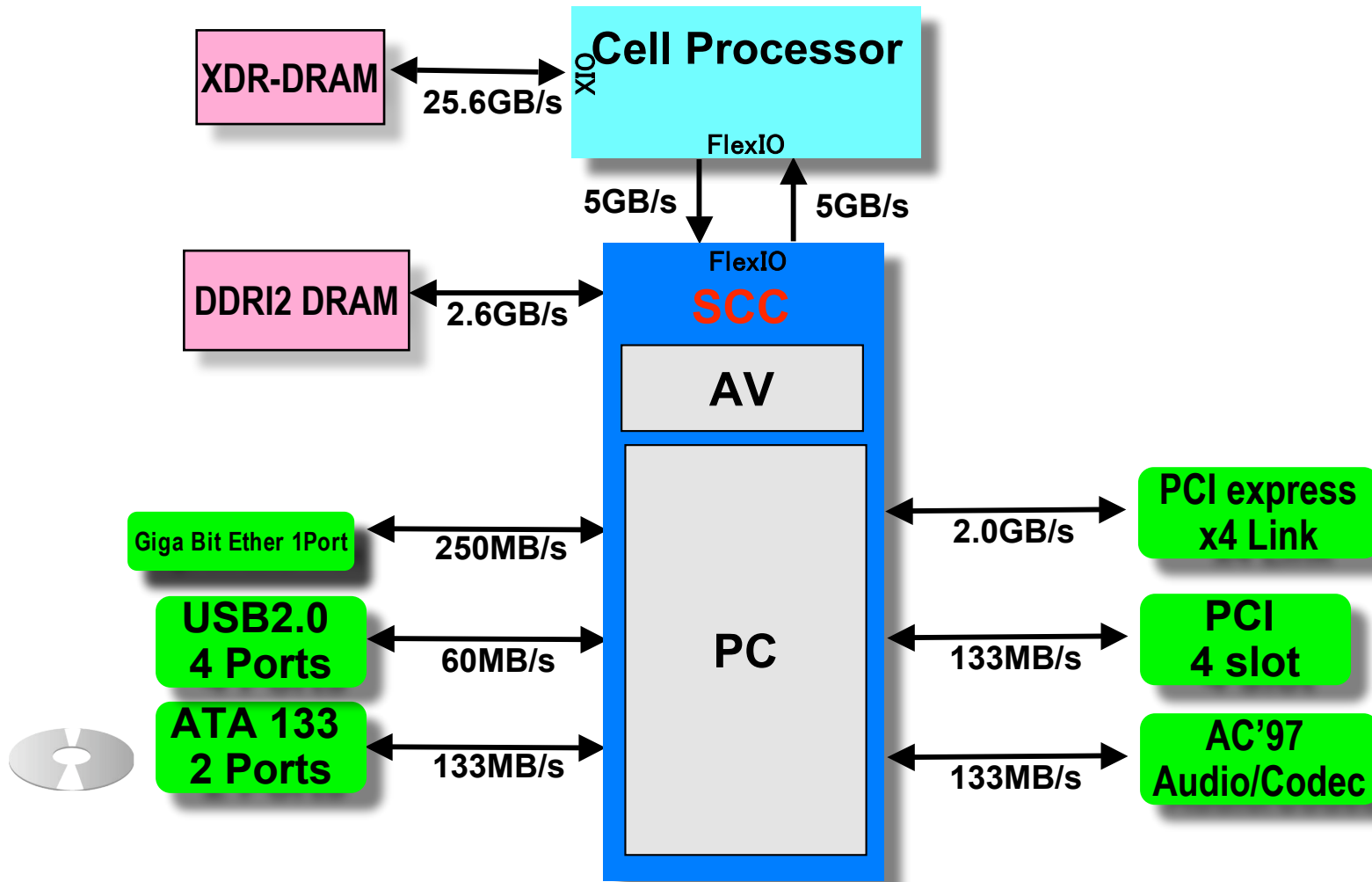
## ■ For computer system

- Standard PC I/F (PCI-Express, PCI, USB2.0).
- High-speed Network I/F (Giga Bit Ethernet).
- Storage device I/F (Parallel ATA).

# A/V functions in SCC



# Computer peripheral functions in SCC



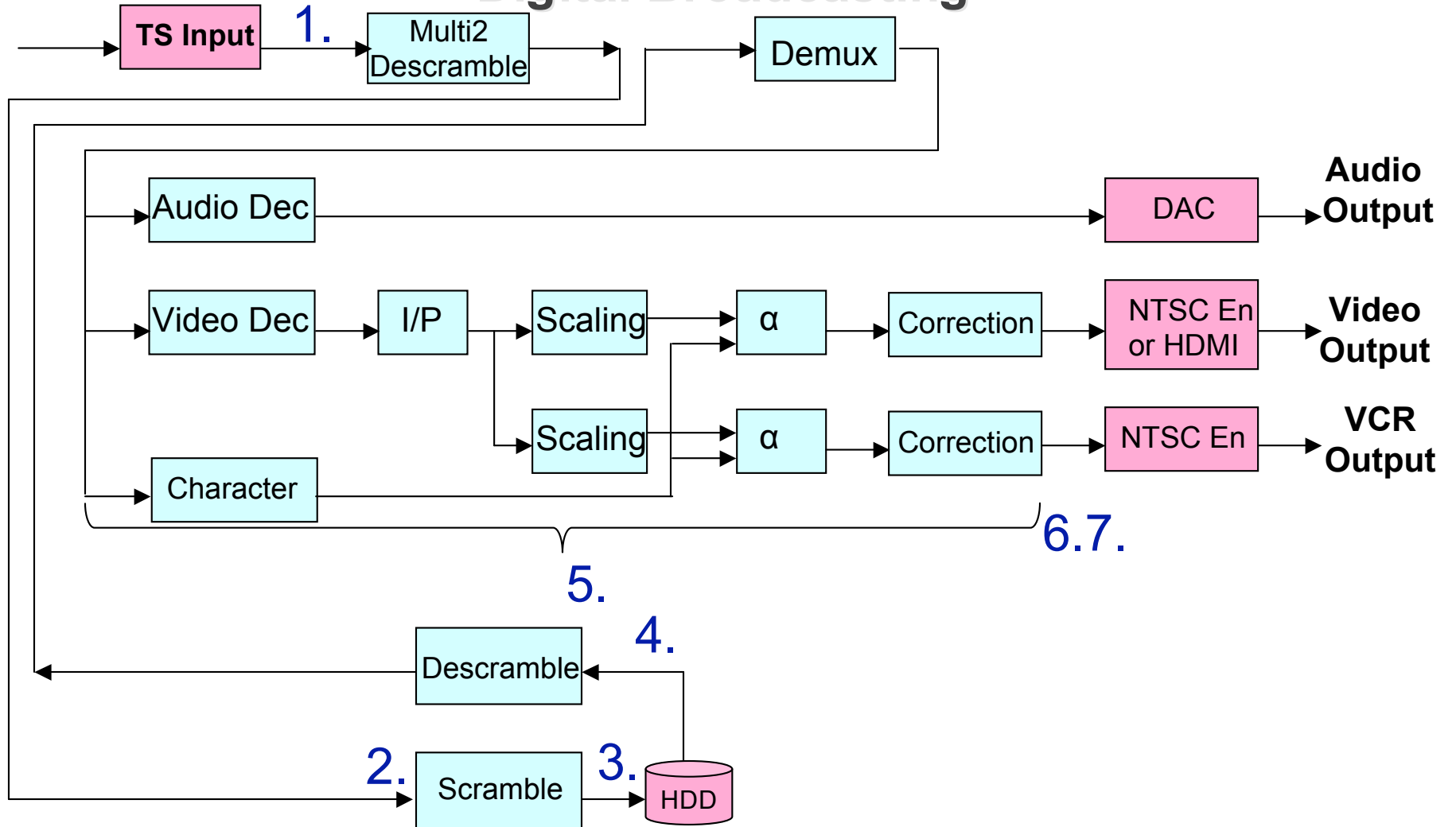
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# Audio/Visual Processing Steps

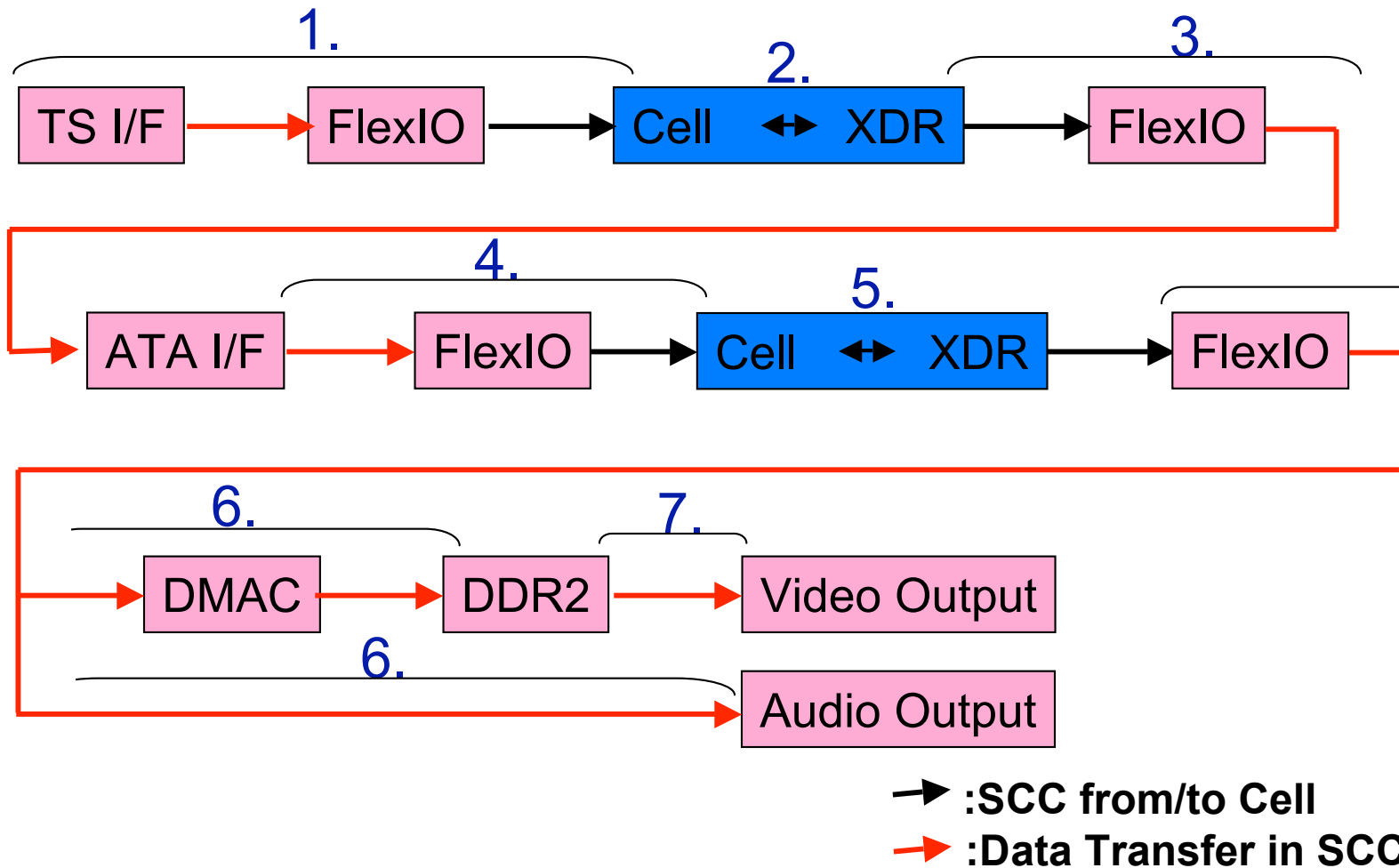
## < Digital Broadcasting >

From BS Digital Tuner

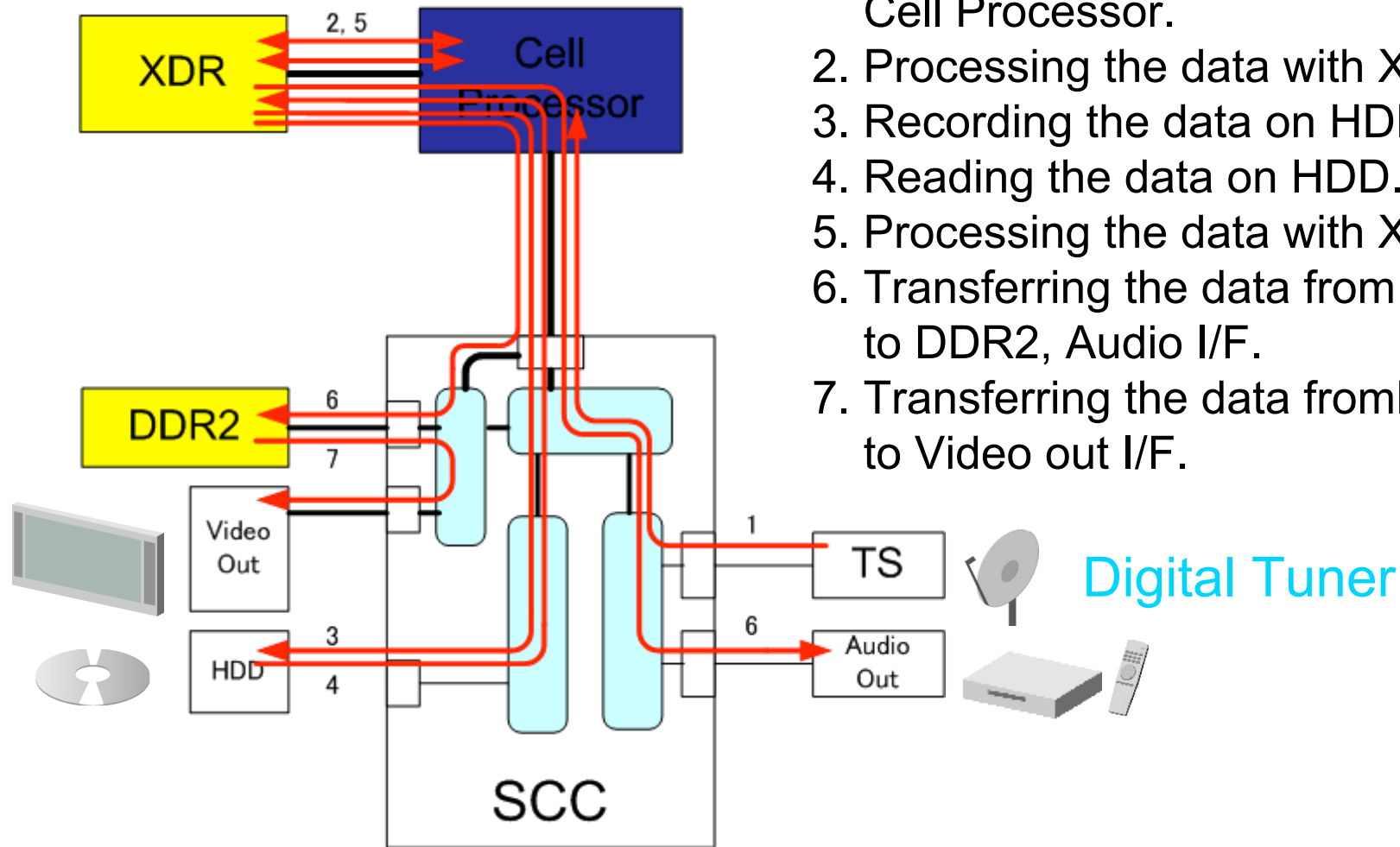


# Audio/Visual data flow

Taking digital broadcasting and Outputting A/V data with time shift function.



# Data Processing Flow



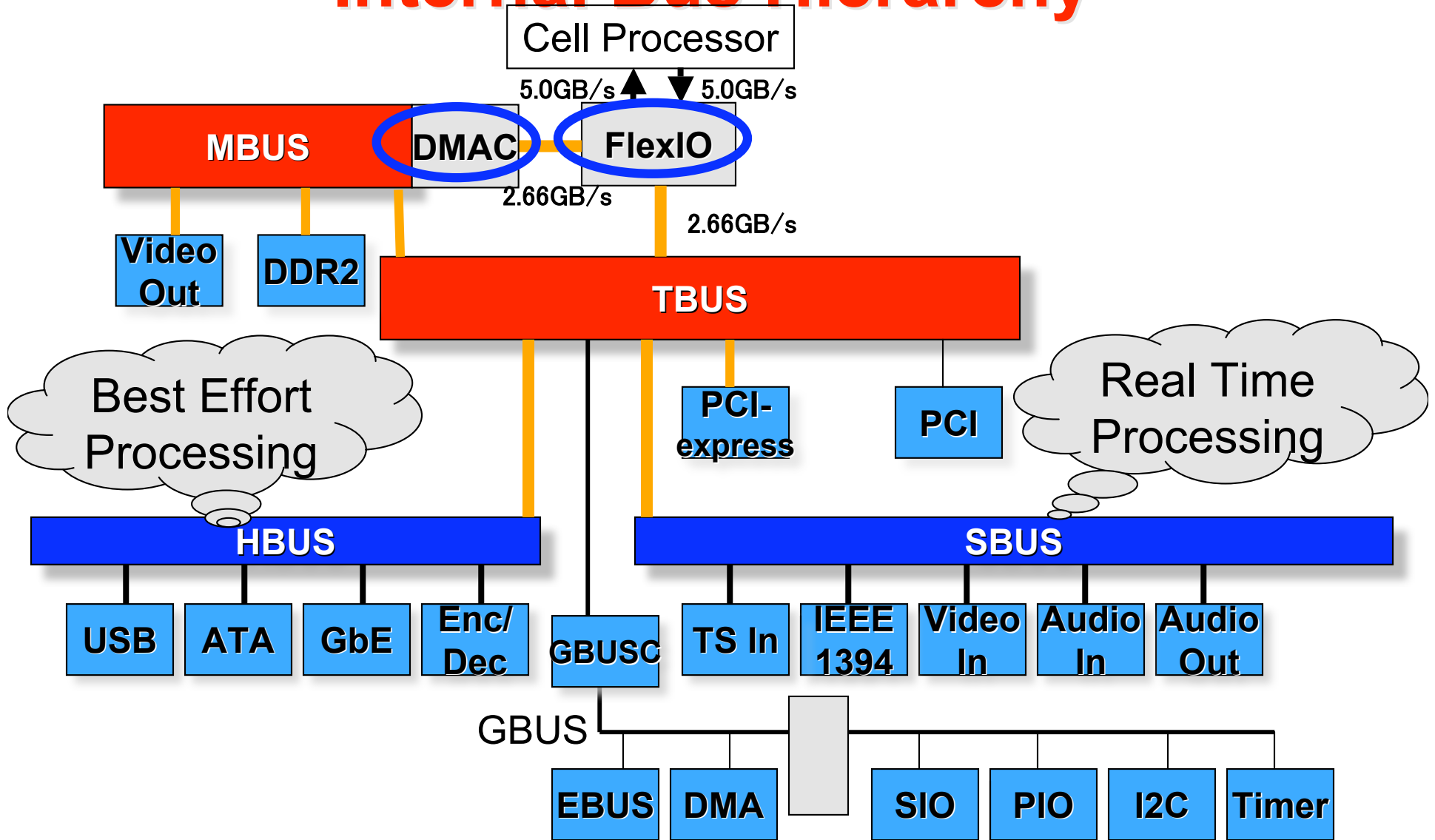
1. Transferring the data from TS I/F to Cell Processor.
2. Processing the data with XDR.
3. Recording the data on HDD.
4. Reading the data on HDD.
5. Processing the data with XDR.
6. Transferring the data from XDR to DDR2, Audio I/F.
7. Transferring the data from DDR2 to Video out I/F.

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# Internal Bus Hierarchy



# Key Architecture (1/2)

## ■ Internal Bus Architecture

### ➤ Quality of Service (QoS)

-Bandwidth allocation by bus arbitration mechanism.(with priority in every cycle. → TDM .)

### ➤ Hierarchical Architecture

-Dividing the bus according to the required features.

Real time bus and Best effort.

## ■ DDR2 memory interface

### ➤ Dedicated DMA controller

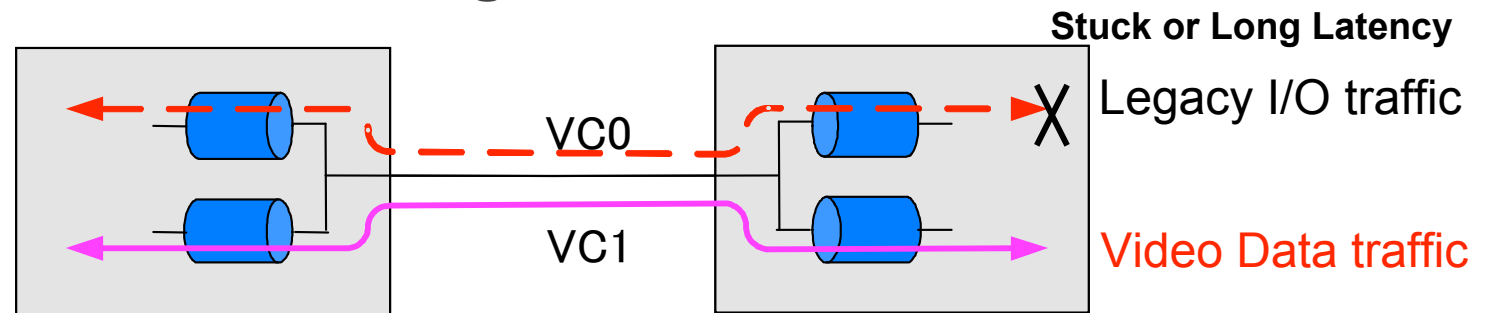
-For streaming data.

## Key Architecture (2/2)

### ■ Other Features

#### ➤ Virtual Channel Mechanism

To avoid blocking for data flow.



#### ➤ Multiple thread mechanism

Multi/Single threads are alternative.

#### ➤ Pipelined data processing

#### ➤ Data ordering mechanism

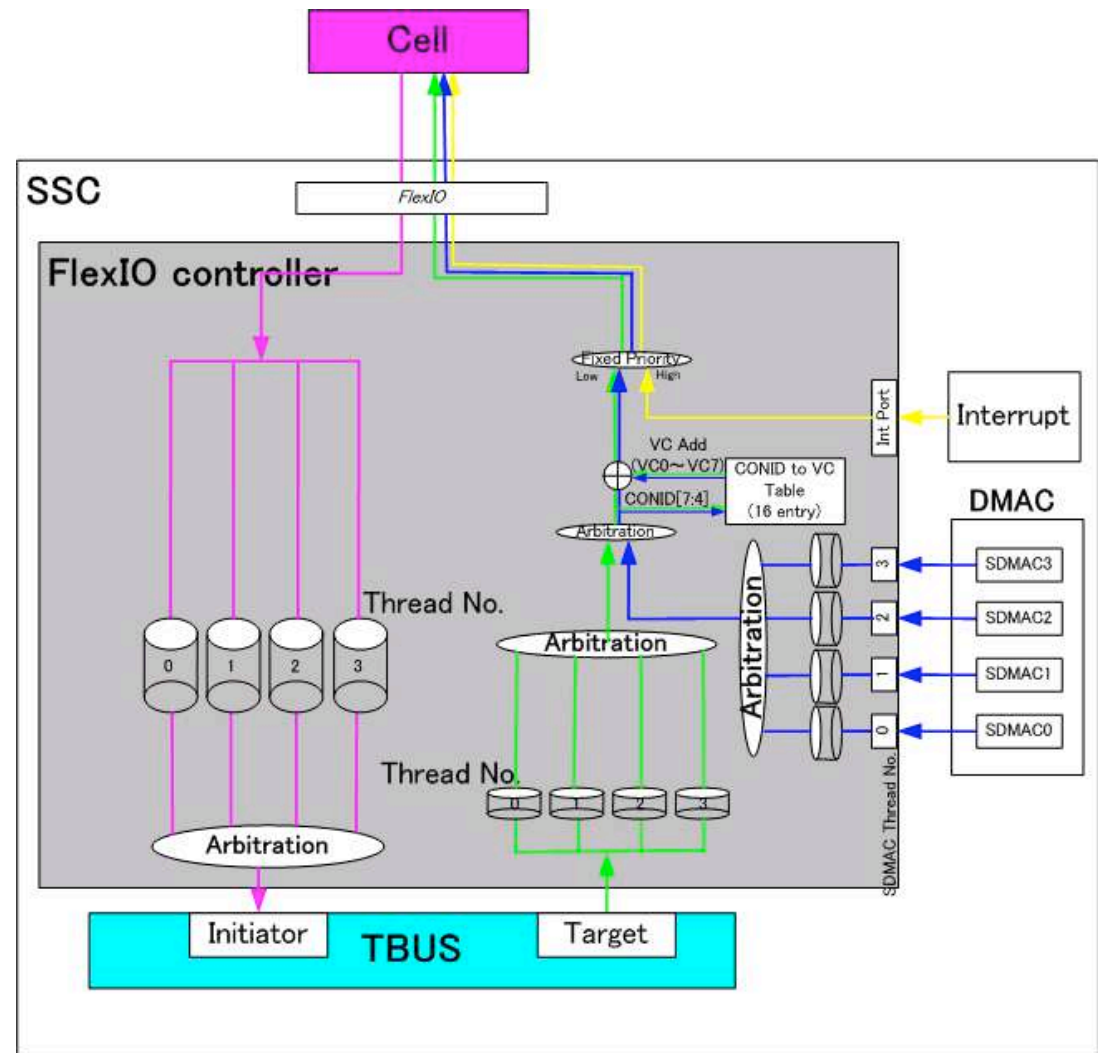
# FlexIO controller

- Virtual Channel/Thread correspond to Cell functionality

Master Path : 8

Slave Path : 4

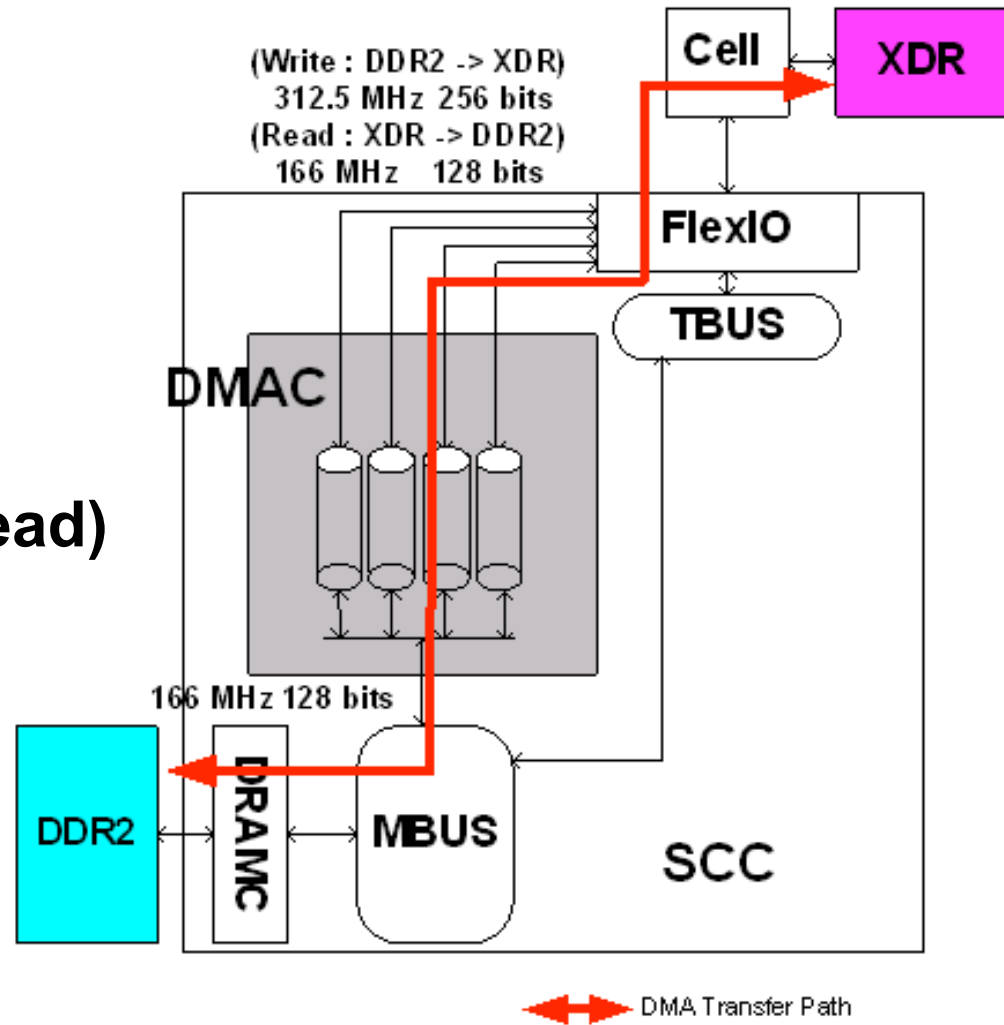
- Priority Control



# Dedicated DMA controller

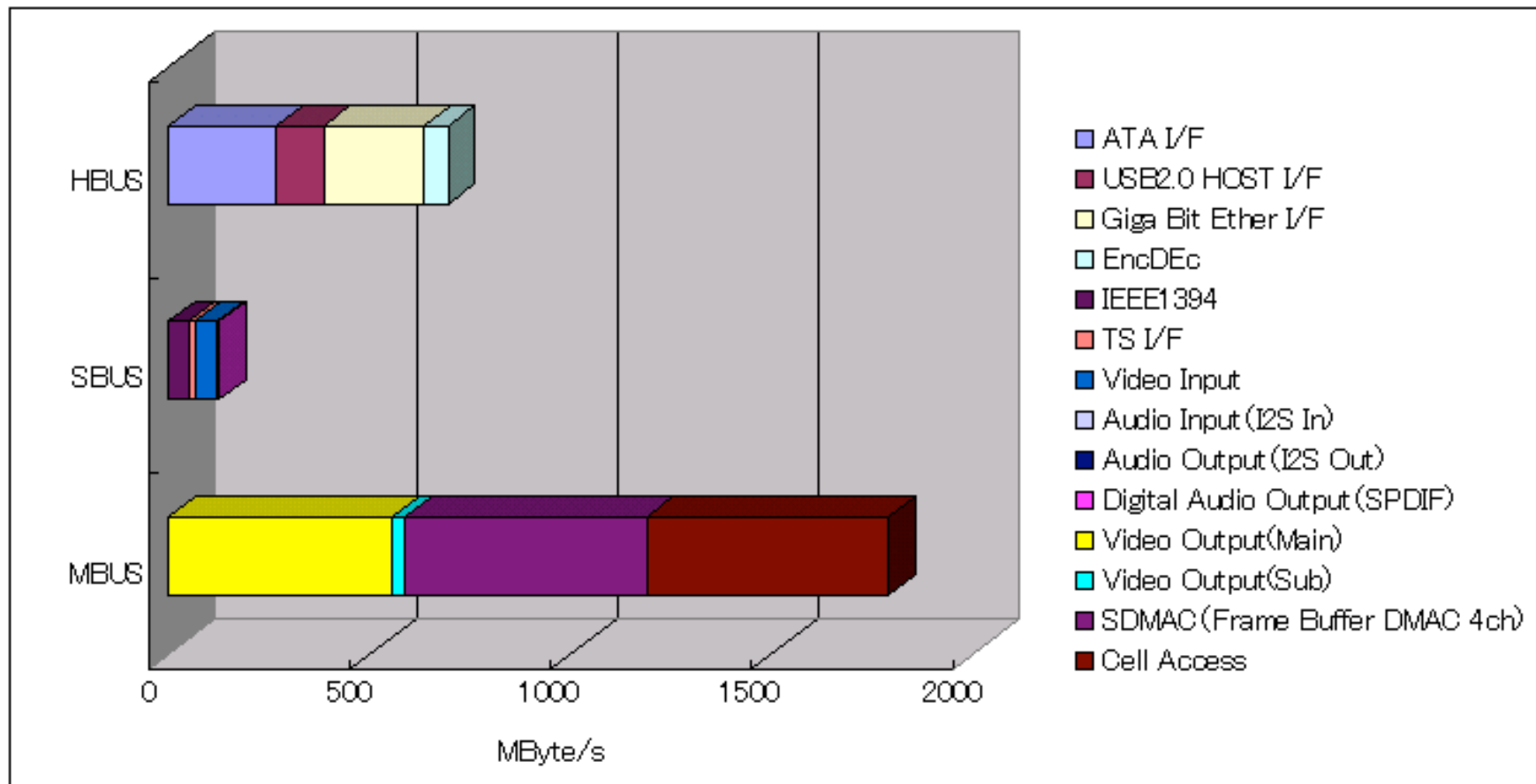
< For DDR2 memory >

- High bandwidth  
 XDR → DDR2  
 DDR2 → XDR
- 4 Virtual Channel(thread)
- Multi/Single threads



# Requirement vs. Bandwidth

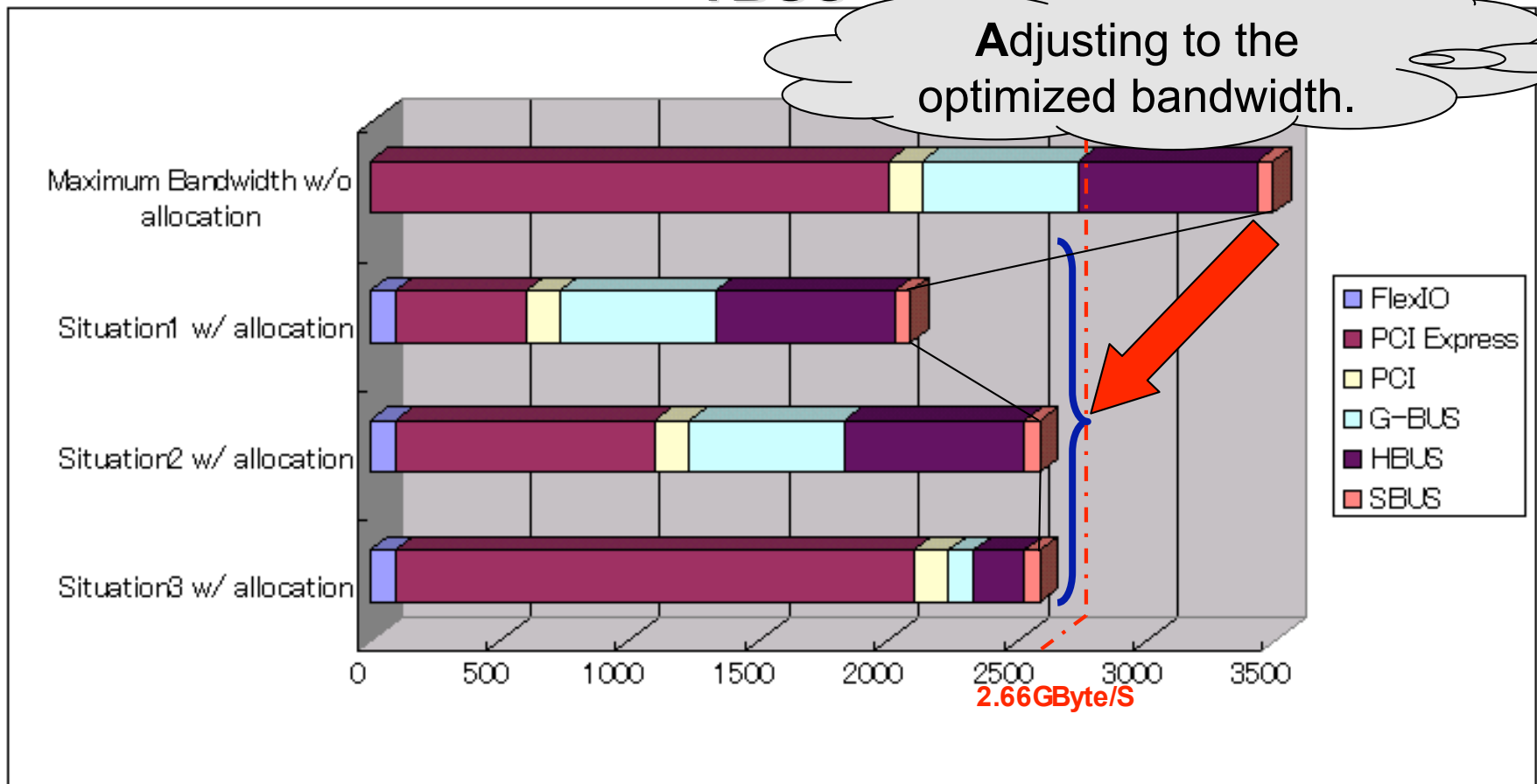
## < MBUS, SBUS, HBUS >



The each maximum bus bandwidth(2.66GByte/s) is sufficient for the every required module bandwidth.

# Bandwidth Allocation Results

< TBUS >



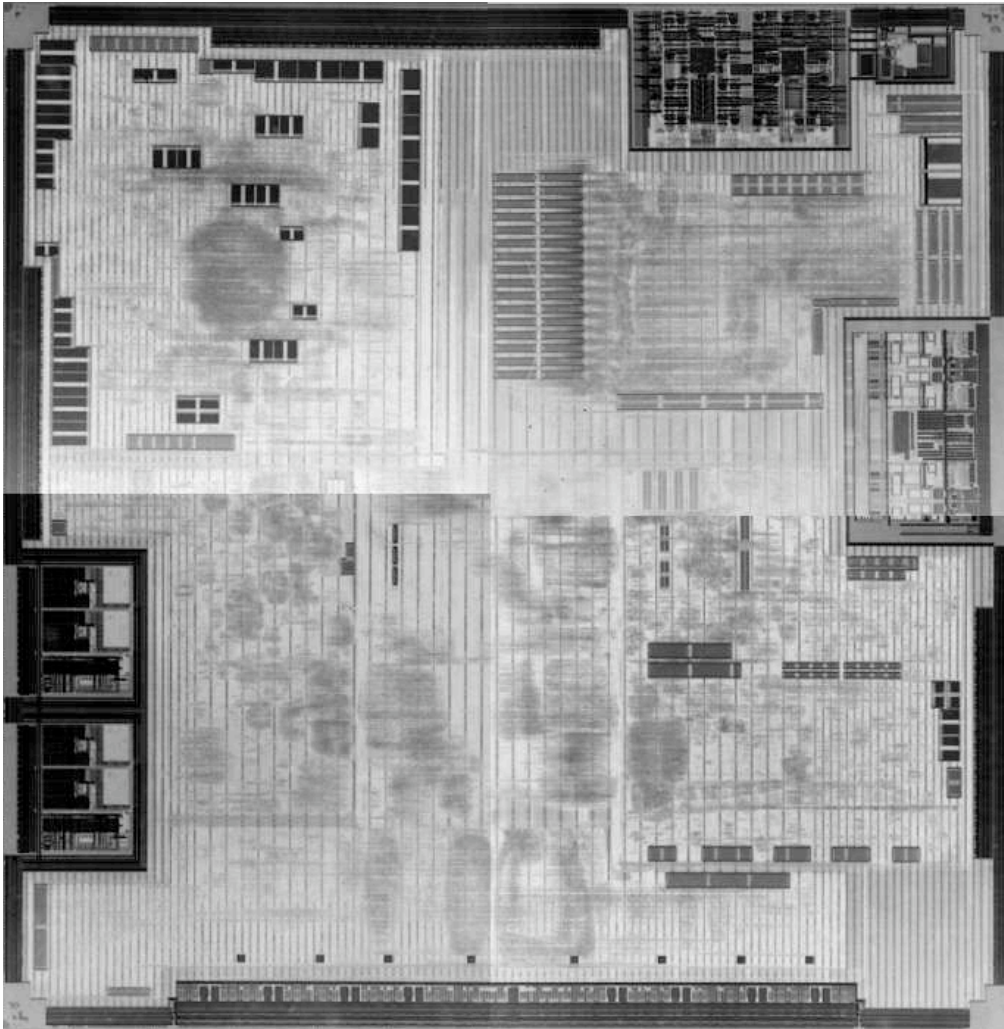
The bandwidth allocation mechanism can satisfy the BUS requirement from each module/bus bridge.

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# Chip Photo



- **Process**  
90nm CMOS Process  
7 Layer Cu
- **Frequency**  
-333MHz
- **Package**  
PBGA[FC], 1385pin,  
40mm $\square$ , 1mm pitch
- **Chip Size**  
12.71mm x 12.71mm
- **VDD**  
Core: 1.2V  
I/O: Multiple voltages for  
various peripherals

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## Conclusion

- **Super Companion Chip for “Cell” processor system has been successfully developed.**
- **Both rich audio visual features supporting HD and PC I/O features are integrated on the chip.**
- **Simultaneous 48 MPEG-2 SD stream decoding has been demonstrated by utilizing SCC’s high bandwidth bus with QoS capability.**