HOT CHIPS 17
August 14 to 16, 2005
Memorial Auditorium, Stanford University
A Symposium on High Performance Chips
Sponsored by the IEEE Technical Committee on Microprocessors and Microcomputers

Panel Discussion: The Next Killer Application

Moderator:	**Howard Sachs**	**Telairity**
Panelists:	**Ajay Luthra**	**Motorola**
	David Kirk	**Nvidia**
	Edward Frank	**Broadcom**
	Nick Tredennick	**Gilder Technology**
	Pradeep Dubey	**Intel**

Abstract:
Hot Chips has always focused on the latest semiconductor processes and computer architectures. As transistors continue to shrink, design costs increase and wafer sizes go from 200mm to 300mm, larger volumes of chips need to be sold in order to pay for the design, mask, EDA software, and manufacturing costs. This puts more pressure on the semiconductor business to search for the next killer application in the hopes of filling the factories. Some of the issues raised below will be discussed.

- What are some of the past successful killer applications?
- What were the key enabling factors?
- What are the financial requirements to be considered a killer application?
- Are FPGAs a killer application?
- What are the next killer applications?
- Has the emergence of foundries and COT service enabled more killer apps?
- Does the next killer app depend upon your perspective?
- Is HDTV one of the next killer apps?

Panelist Biographies:

Ajay Luthra received his B.E. (Hons) from BITS, Pilani, India in 1975, M.Tech. in Communications Engineering from IIT Delhi in 1977 and Ph.D. from Moore School of Electrical Engineering, University of Pennsylvania in 1981. From 1981 to 1984 he was a Senior Engineer at Interspec Inc., Philadelphia, Pennsylvania, where he was involved in applications of Digital Signal and Image Processing for Bio-medical applications. From 1984 to 1995 he was at Tektronix, Beaverton, Oregon, where from 1985 - 1990 he was manager of Digital Signal and Picture Processing Group and from 1990 - 1995 he was Director of Communications / Video Systems Research Lab. He is currently a Senior Director in Advanced Technology Group at Connected Home Solutions, Motorola (formerly General Instrument) in San Diego, California, where he is involved in advanced development work in the areas of Digital Video Compression & Processing, Streaming Video, Interactive TV, Cable Head-End system design and Advanced Set Top Box architectures.

He has been an active member of the MPEG committee for more than twelve years where he has chaired several technical sub-groups and pioneered the MPEG-2 extensions for studio applications. He is currently an associate rapporteur/co-chair of Joint Video Team (JVT) consisting of ISO/MPEG and ITU-T/VCEG experts working on developing next generation of video coding standard known as MPEG-4 Part 10 AVC / H.264. He is also U.S.A. Head of Delegates (HoD) to MPEG. He was an Associate Editor of IEEE Transactions on Circuits and Systems for Video Technology (2000-2002) and also a Guest Editor for its Special Issues on H.264/AVC Video Coding Standard, July 2003 and Streaming Video, March 2001.

He holds more than 20 patents, has published more than 25 papers and has been a guest speaker in numerous conferences.

David B. Kirk has been NVIDIA's Chief Scientist since January 1997. His contribution includes leading NVIDIA graphics technology development for today's most popular consumer entertainment platforms. In 2002, Dr. Kirk received the SIGGRAPH Computer Graphics Achievement Award for his role in bringing high-performance computer graphics systems to the mass market. From 1993 to 1996, Dr. Kirk was Chief Scientist, Head of Technology for Crystal Dynamics, a video game manufacturing company. From 1989 to 1991, Dr. Kirk was an engineer for the Apollo Systems Division of Hewlett-Packard Company. Dr. Kirk is the inventor of 50 patents and patent applications relating to graphics design and has published more than 50 articles on graphics technology. Dr. Kirk holds B.S. and M.S. degrees in Mechanical Engineering from the Massachusetts Institute of Technology, and M.S. and Ph.D. degrees in Computer Science from the California Institute of Technology.

Dr Edward H. Frank is corporate Vice President of Research and Development at Broadcom Corporation. He joined Broadcom in 1999 through its acquisition of Epigram Inc., where he was Executive Vice President and co-founder.

Prior to founding Epigram, Frank co-founded NeTpower, a workstation company. Before NeTpower, he was a Distinguished Engineer at Sun Microsystems, where he was co-architect of several generations of Sparcstations, and was one of the principals of the Green Project, which created the precursor to Java.
Frank holds a Ph.D. in Computer Science from Carnegie Mellon University, and M.S.E.E and B.S.E.E degrees from Stanford. He has over 20 issued patents.
Dr. Frank is a trustee of Carnegie Mellon University and a venture partner with Advanced Technology Ventures.

Howard Sachs is the President & CEO of Telairity Semiconductor, Inc. Prior to forming Telairity Semiconductor, Mr. Sachs has held a variety of senior management positions with Fujitsu Microelectronics, Intergraph Corporation, Fairchild Semiconductor, Cray Laboratories and National Semiconductor. He has worked primarily in computer hardware and software development, and has fifteen patents issued relating to microprocessor cache memories, VLIW architectures, and design methodologies. He was the architect for the Clipper and Telairity processors. He has a BSE from Los Angeles State College and a MSEE from the University of Southern California.

Dr. Nick Tredennick is Editor of the *Gilder Technology Report*. He is an advisor and investor in numerous pre-IPO startups and is a member of technical advisory boards for numerous companies including Ascenium, CriticalBlue, Impinj, QuickFlex, Terakeet, and the Venture X Group. He has been on the editorial advisory board for several technical publications including *IEEE Spectrum* and *Microprocessor Report*.

Nick was named a Fellow of the IEEE for contributions to microprocessor design. He was a Senior Design Engineer at Motorola, a Research Staff Member at IBM's Watson Research Center, and Chief Scientist at Altera. He has taught at the University of Texas at Austin and the University of California, Berkeley. He has been a founder of several Silicon Valley startups.

Pradeep Dubey is a senior principal engineer and manager of Innovative Platform Architecture (IPA) in the Microprocessor Technology Lab, part of the Corporate Technology Group at Intel. His research focus is computer architectures to efficiently handle new application paradigms for the future computing environment. Dubey previously worked at IBM's T.J. Watson Research Center, and Broadcom Corporation. He was one of the principal architects of the AltiVec* multimedia extension to Power PC* architecture. He also worked on the design, architecture, and performance issues of various microprocessors, including Intel® i386™, i486™, and Pentium® processors. He has published extensively, and served on various conference committees in the areas of computer architecture, multithreading, and multimedia processing. He holds 24 patents. Dubey received a B.S. in electronics and communication engineering from Birla Institute of Technology, India, an M.S.E.E. from the University of Massachusetts at Amherst, and a Ph.D. in electrical engineering from Purdue University. He is a Fellow of the IEEE.