Facing the Hot Chip Challenge (Again)

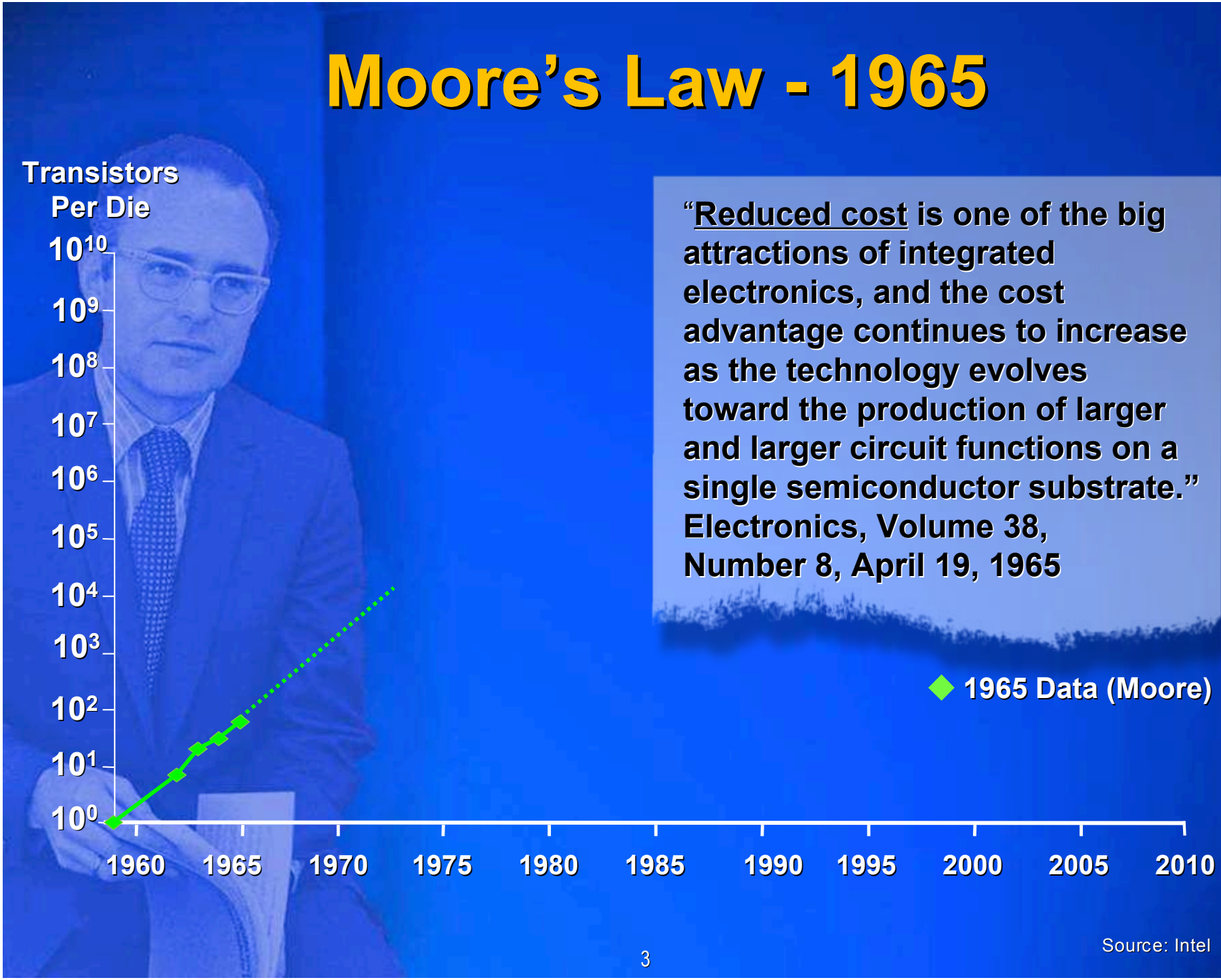
Bill Holt
General Manager
Technology and Manufacturing Group
Intel Corporation

Hot Chips 17
August, 2005

Key Messages

- The driving force behind Moore's Law
- Power has always been a consideration
- Process and design collaboration required to address power challenges
- Technology Advances provide a transistor budget to support innovation
- Efficient Design utilizes transistor budget to deliver product performance

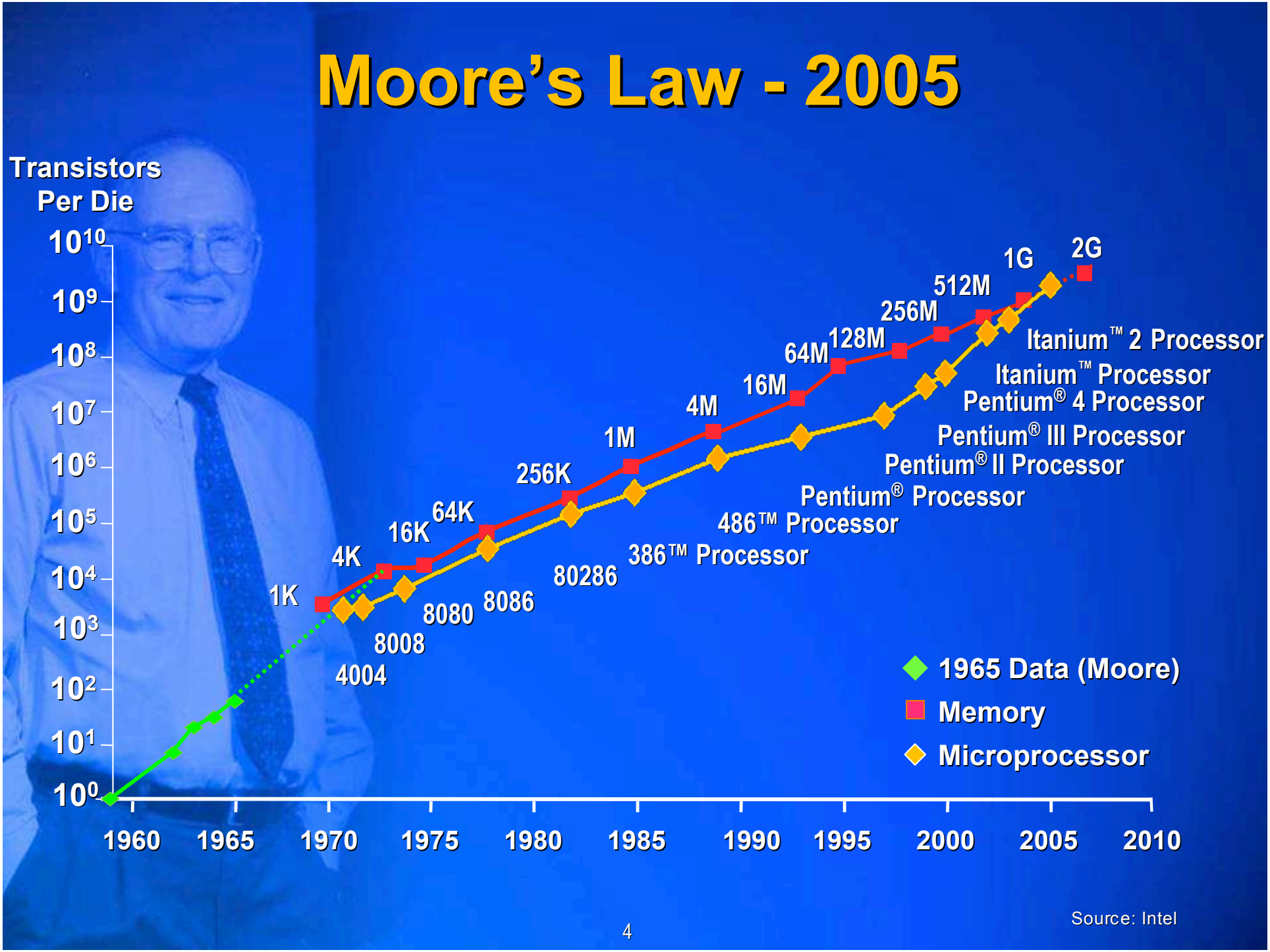
Moore's Law - 1965



"Reduced cost is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate."
Electronics, Volume 38,
Number 8, April 19, 1965

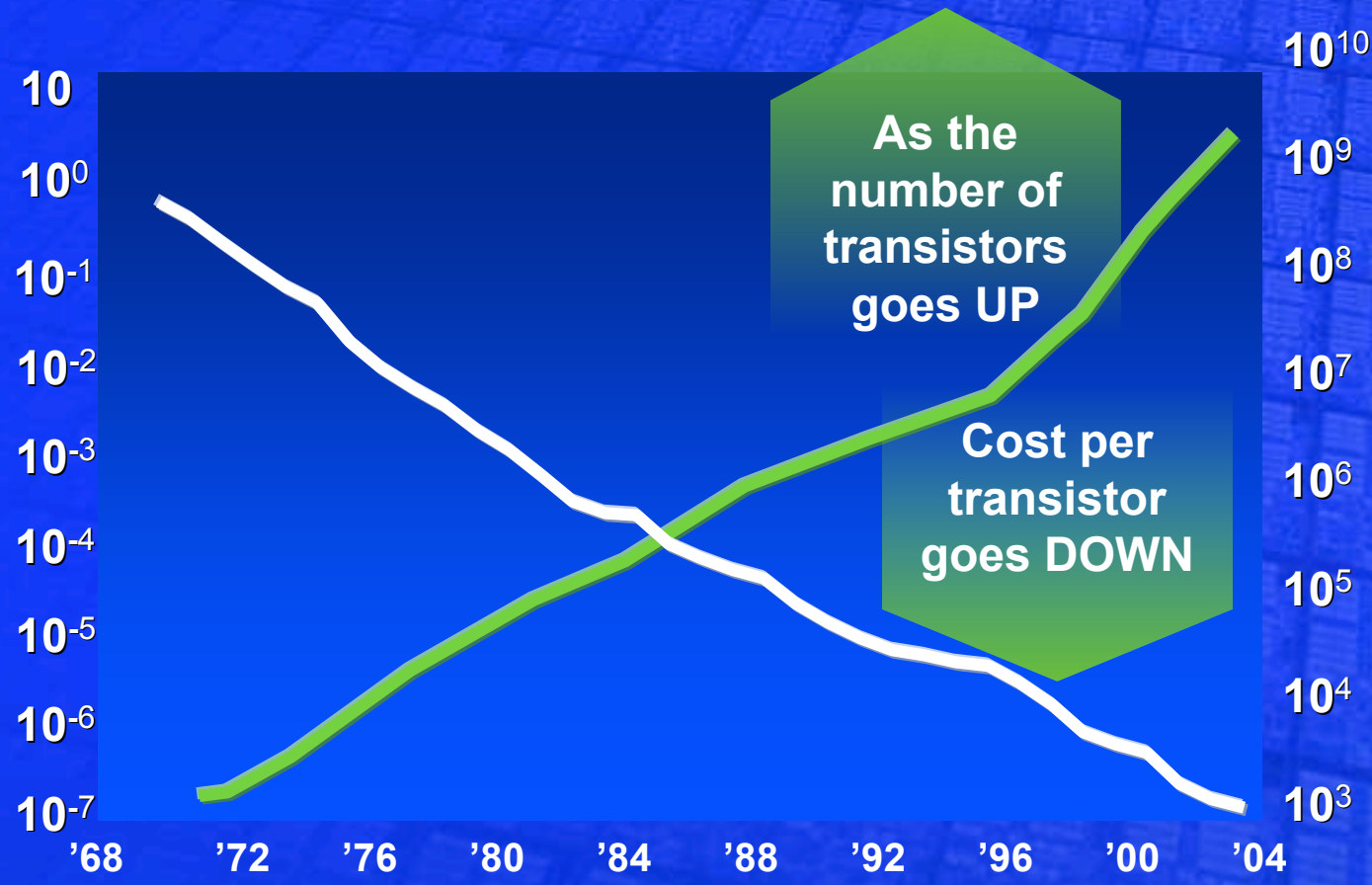
Source: Intel

Moore's Law - 2005



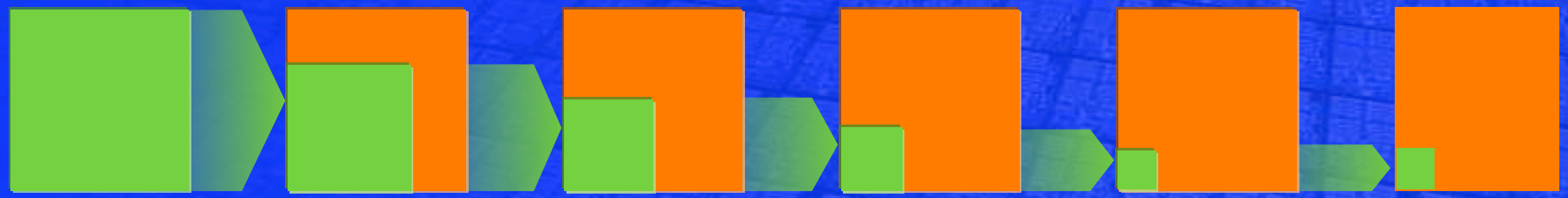
Source: Intel

The Economics of Moore's Law



Source: WSTS/Dataquest/Intel

Scaling: The Fundamental Cost Driver



350nm 200mm | 250nm 200mm | 180nm 200mm | 130nm 200mm | 90nm 300mm | 65nm 300mm *Dual Core*

Twice the circuitry in the same space (architectural innovation)

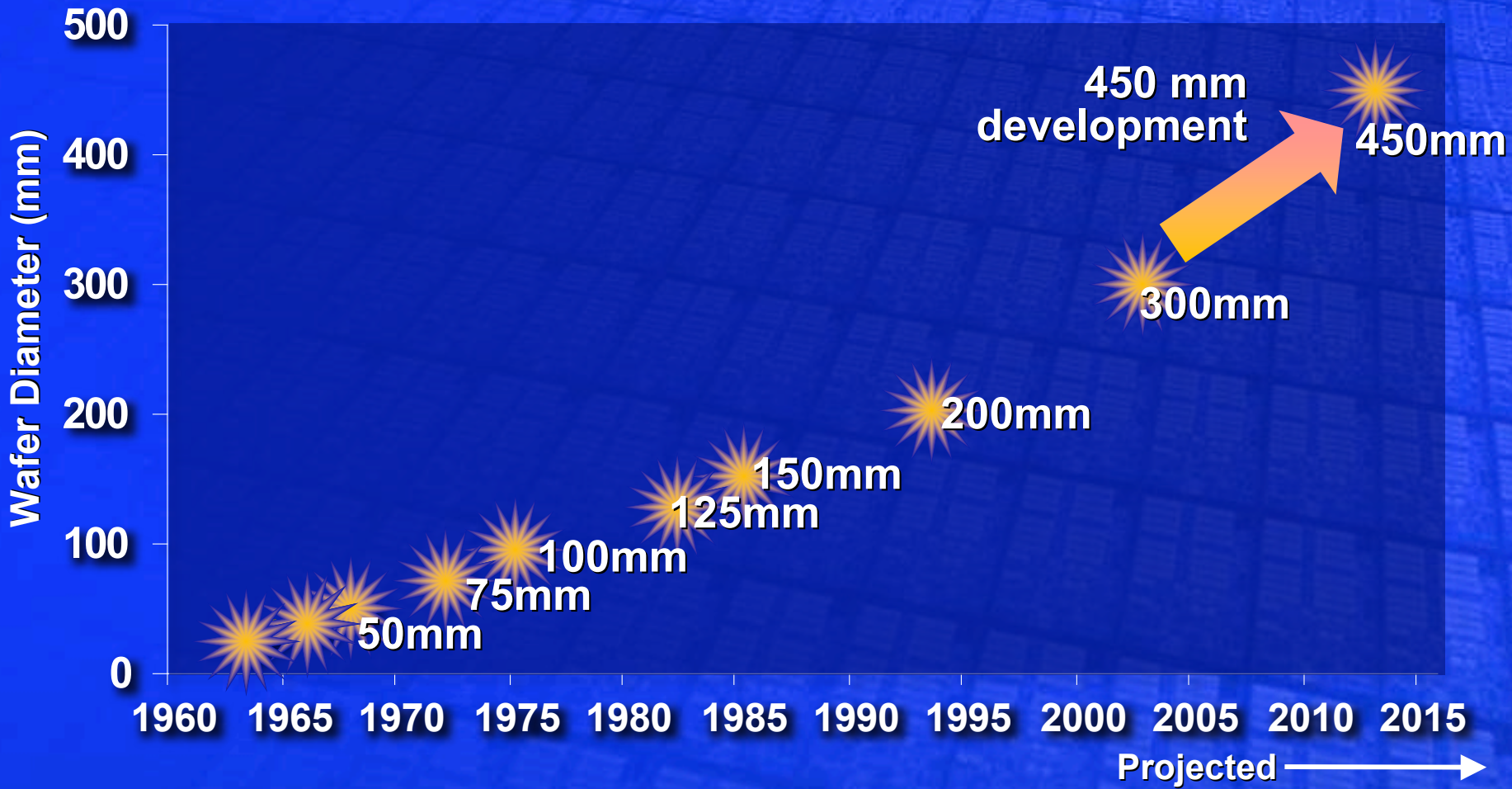
OR

The same circuitry in half the space (cost reduction)

=

Half the die size for the same capability than in the prior process

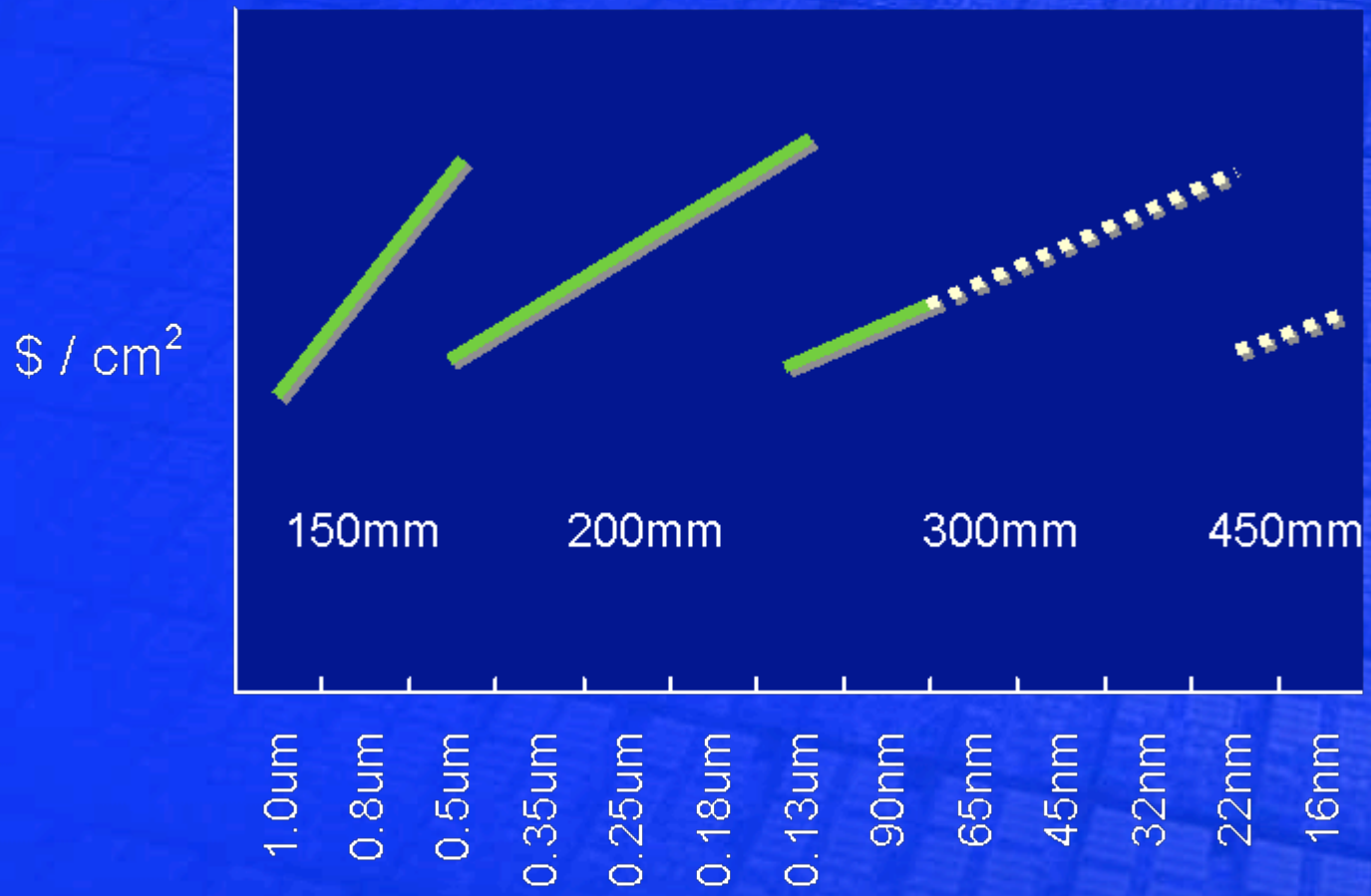
Wafer Size: Enables Cost Efficiency



Year That Industry Exceeds 3 Million wafers/year

Source: VLSIR

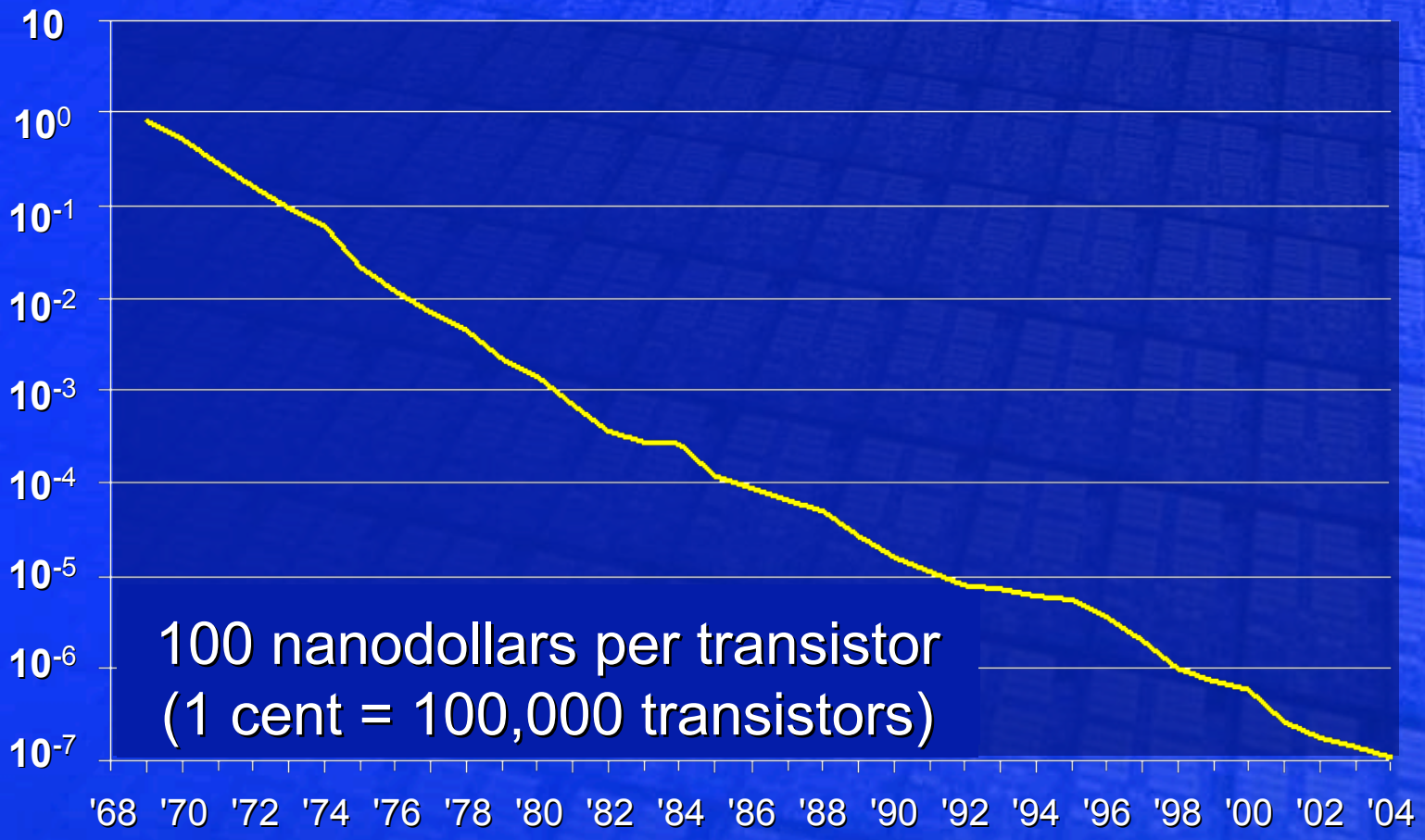
Processed Wafer Cost



Wafer size conversions offset trend of increasing wafer processing cost

Source: Intel

Moore's Law + Bigger Wafers = Lower Cost/function



Source: WSTS/Intel, 5/05

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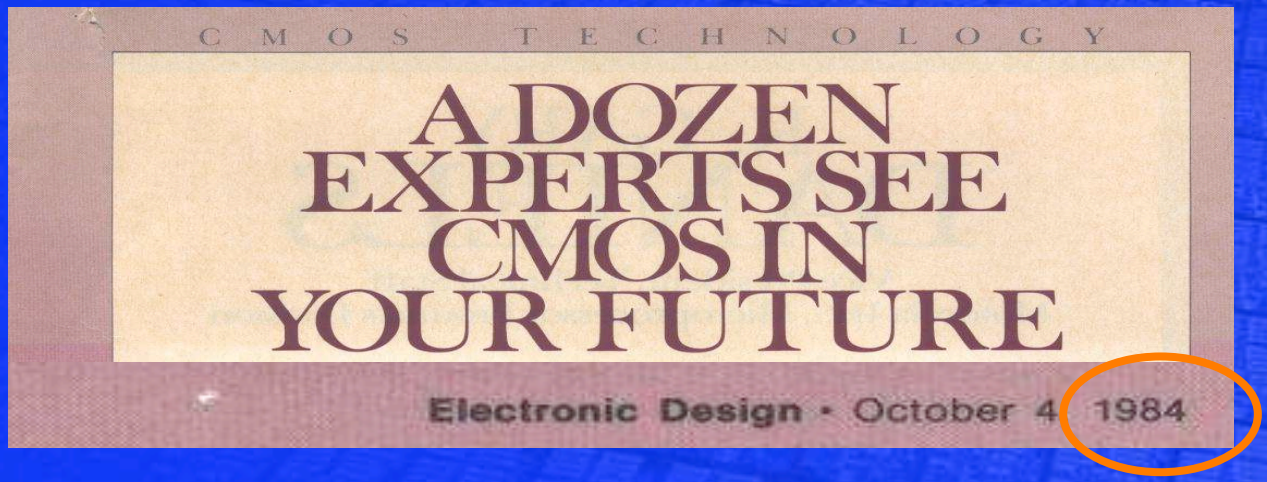
Power challenges are neither new nor fundamental

"Will it be possible to remove the heat generated by 10's of thousands of components?"

G. Moore, *Cramming more components onto integrated circuits*, Electronics, Volume 38, Number 8, April 19, **1965**

Moore's Law Preceded CMOS


CMOS TECHNOLOGY

A DOZEN EXPERTS SEE CMOS IN YOUR FUTURE

Electronic Design • October 4 1984

"The **power barriers** now facing alternative semiconductor processes indicate that only CMOS will allow chip makers to capitalize on the density that can be achieved with gate arrays and standard cells."

"Once, maybe twice a decade the electronics industry encounters a force that affects not only the way circuits are physically designed but also the way the industry thinks. **CMOS is just such a force**."

Source: Electronic Design, October 1984

Silicon Technology has Changed to Increase Power Efficiency

1960's: Bipolar

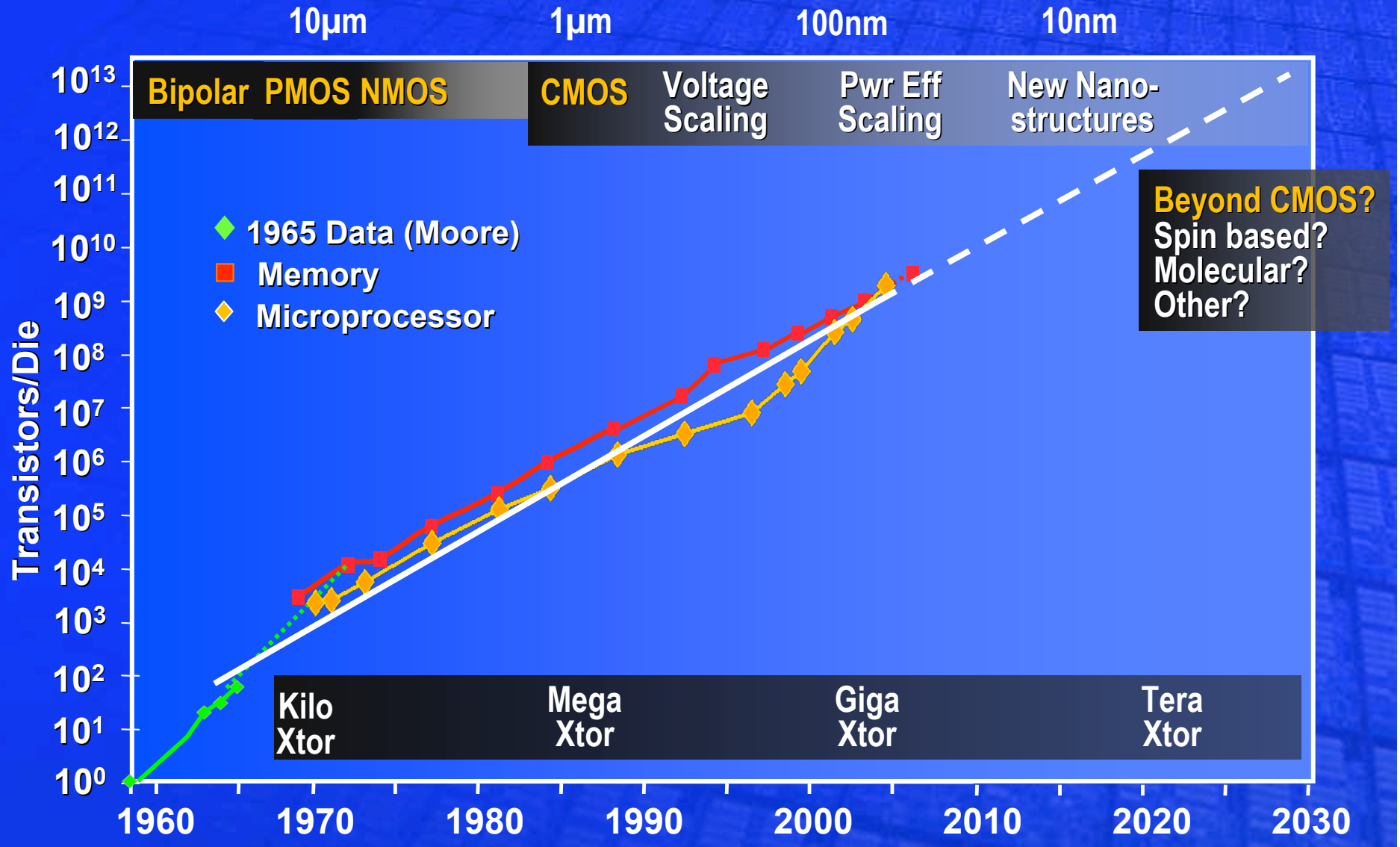
1970's: PMOS, NMOS

1980's: CMOS

1990's: Voltage scaling ($P = CV^2f$)

2000's: Power efficient scaling/design

Moore's Law Will Outlive CMOS



Through Innovation

Source: Intel

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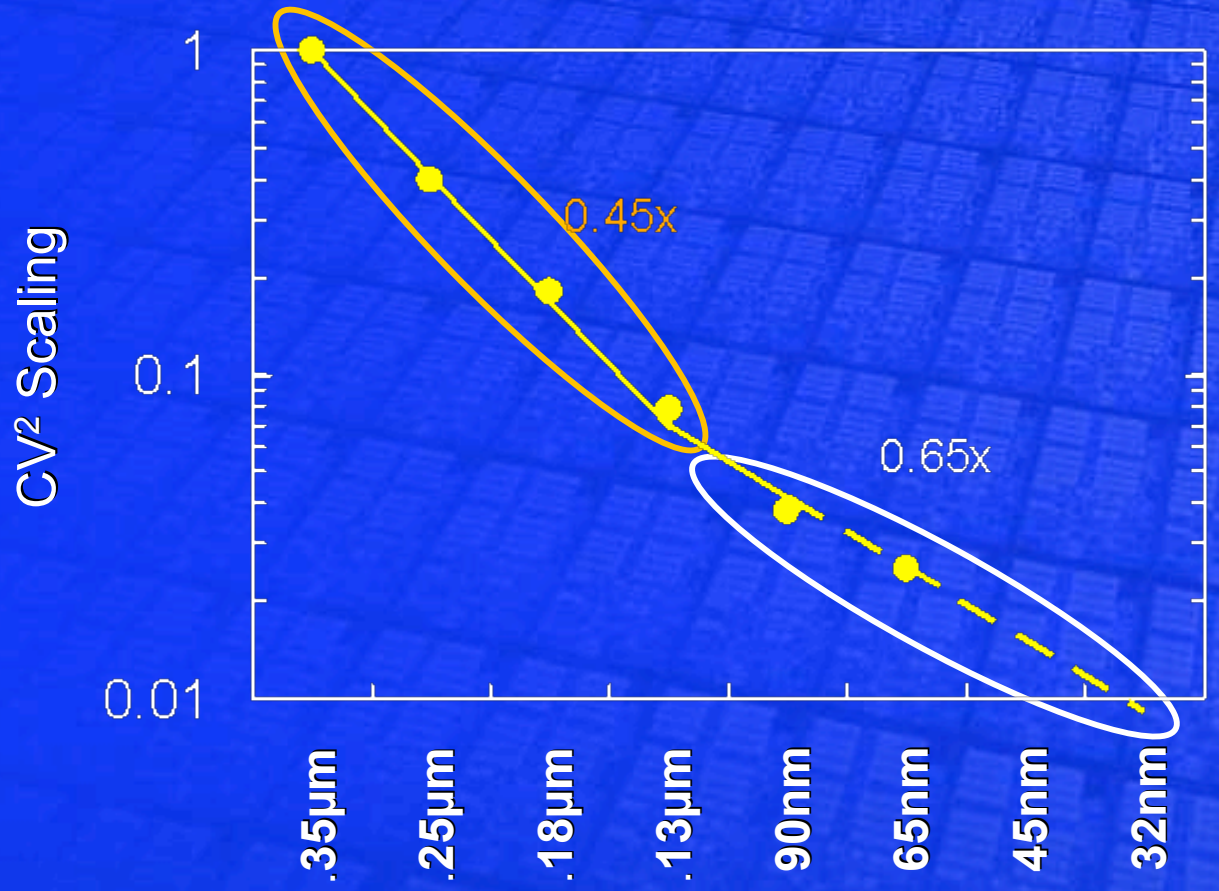
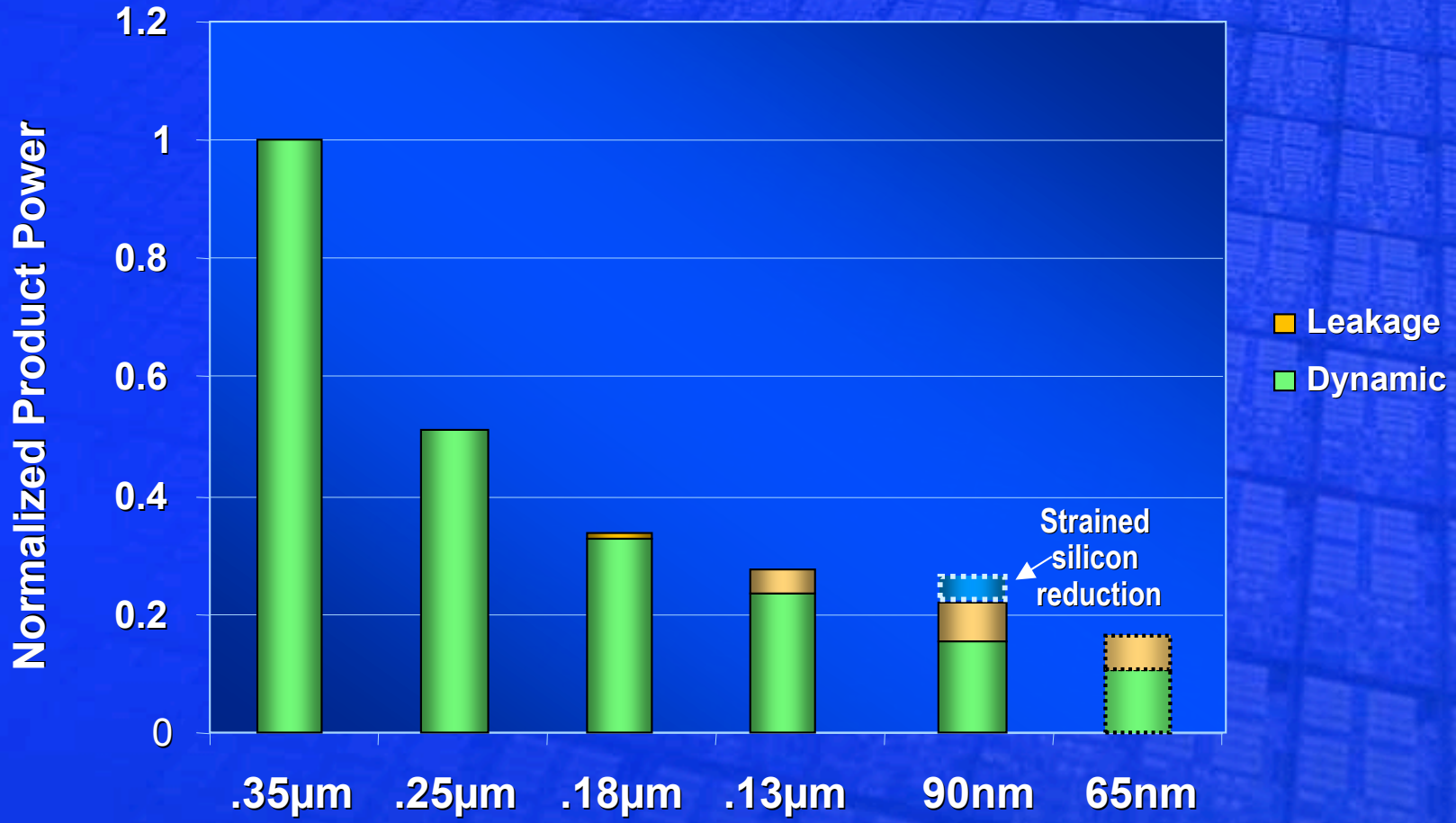
Process Advances Still Scale Power



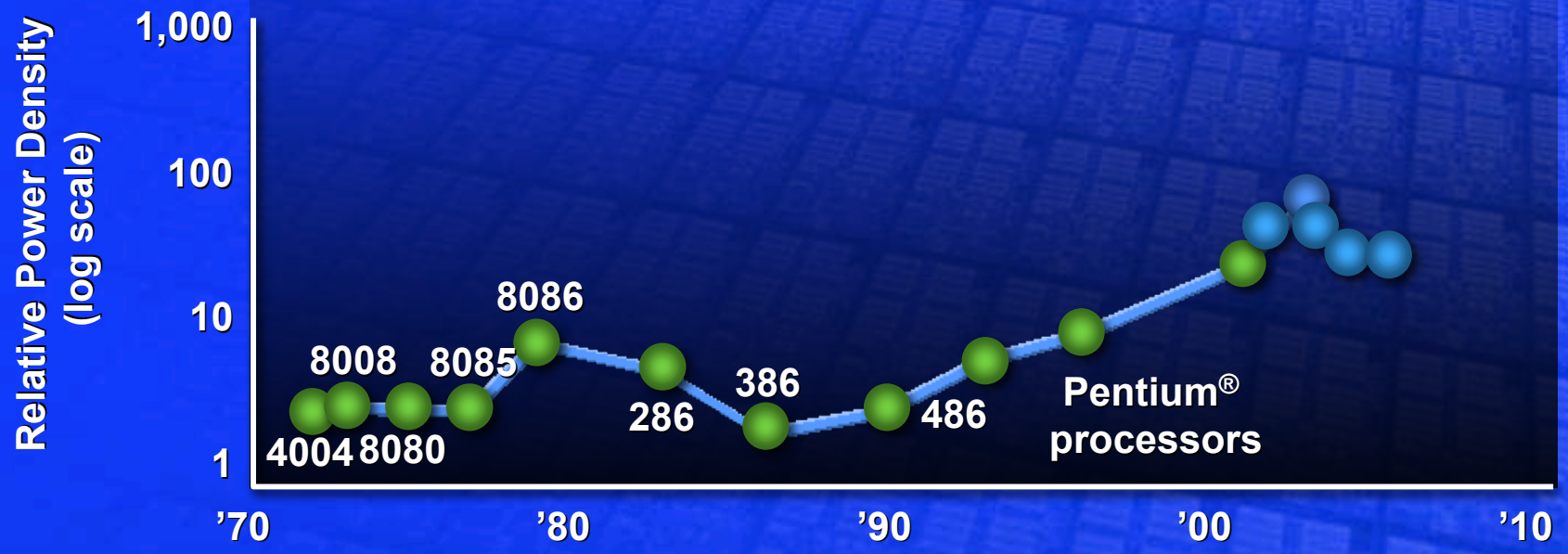
but the rate has slowed and collaboration is required

Leakage becomes Significant

Power scaling vs. process for the last 10 years
(includes frequency increasing with process speed)

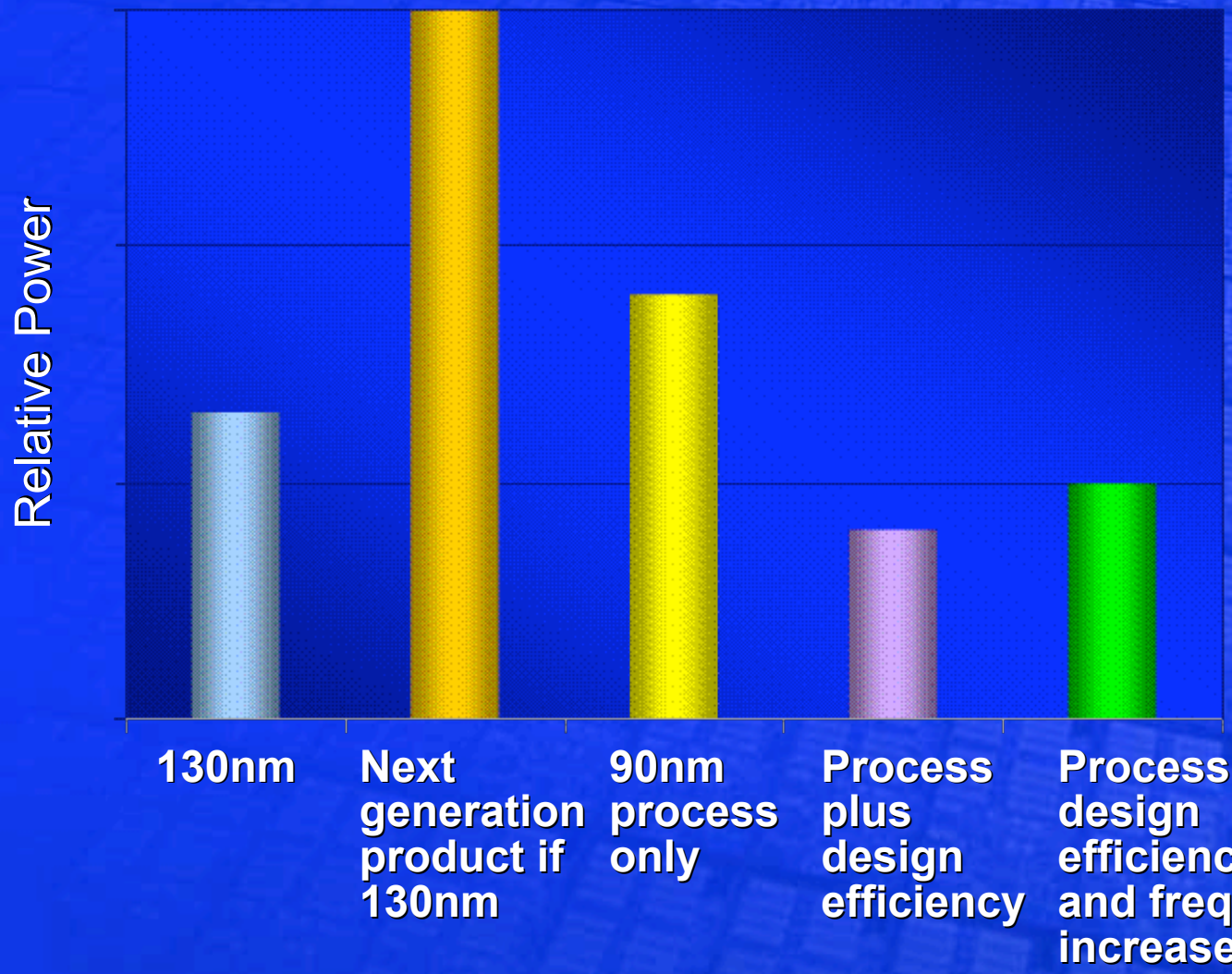


However, Power Density Has Leveled Off



Source: Intel

Effective Process and Design Collaboration Succeeds in Power Improvements



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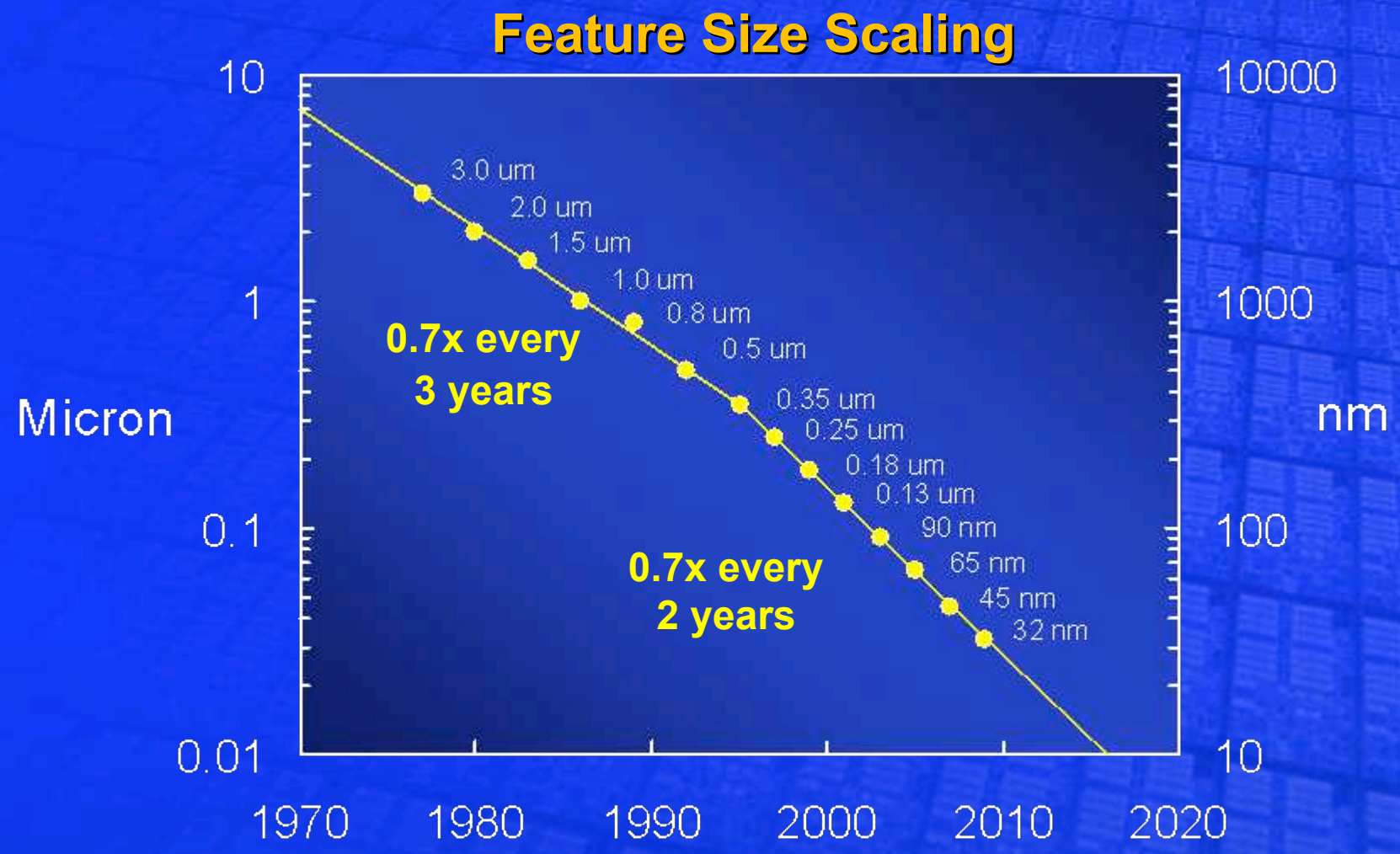
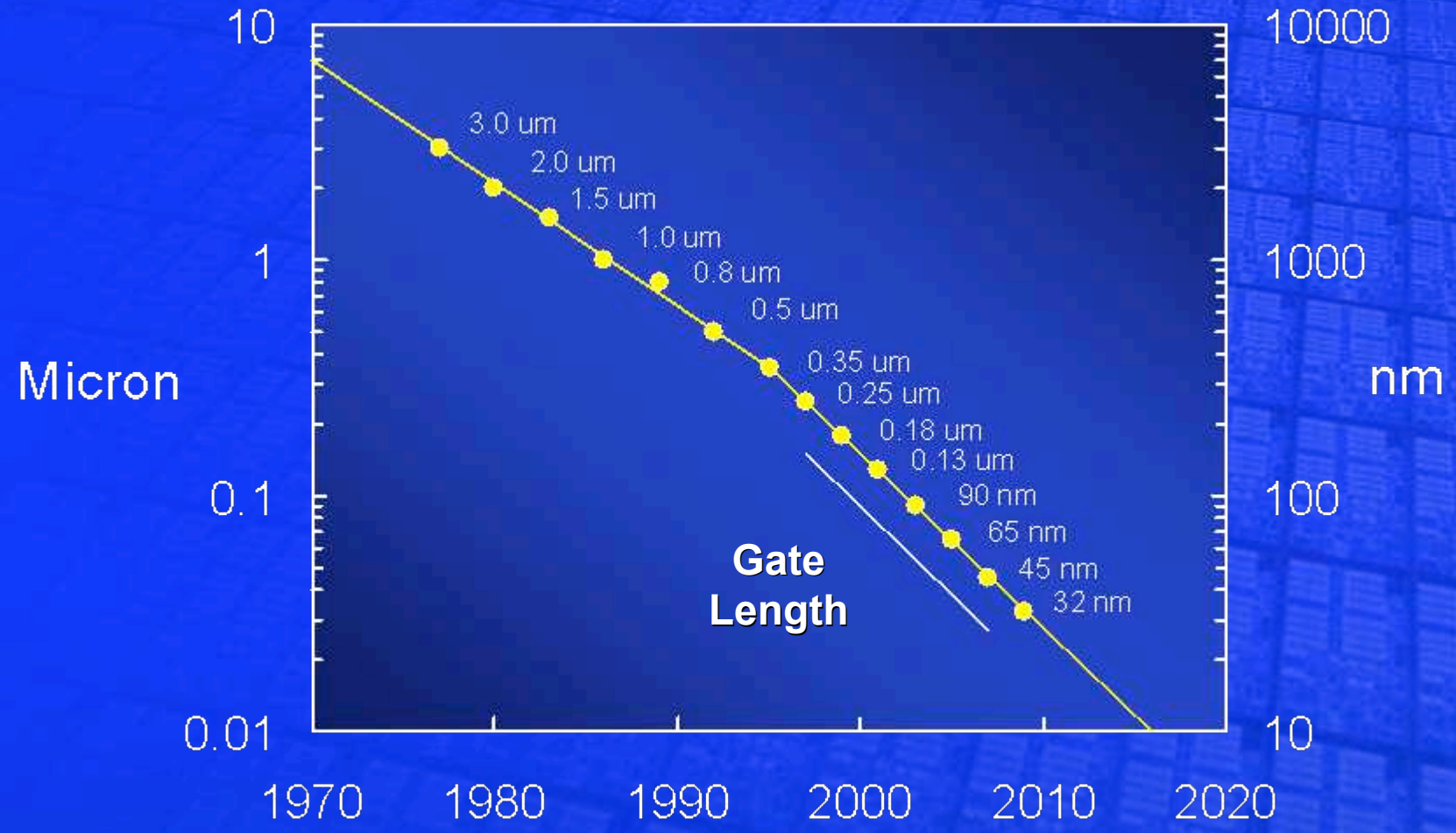
Silicon Technology Advances



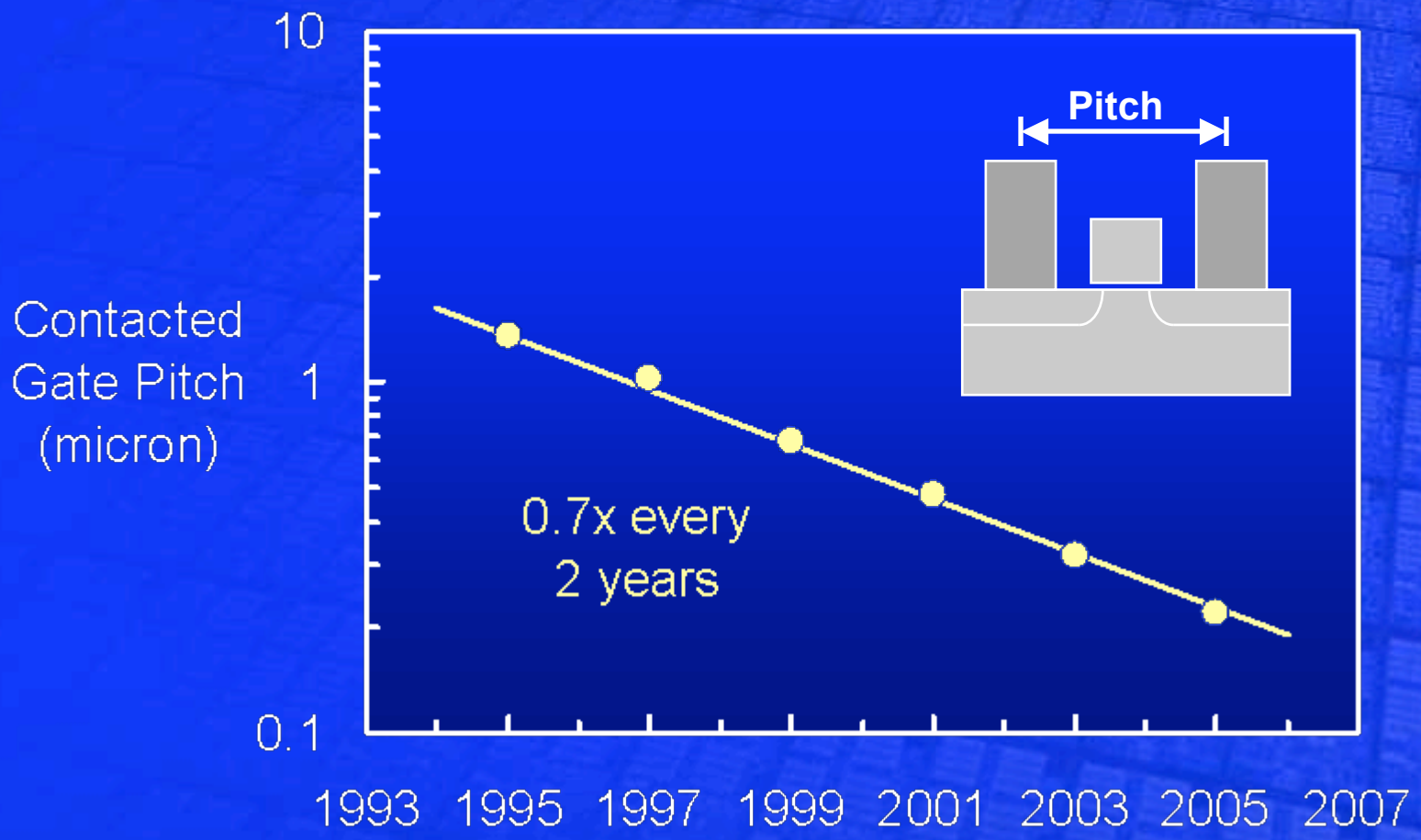
New technology generation every 2 years

Transistor Gate Length Scaling



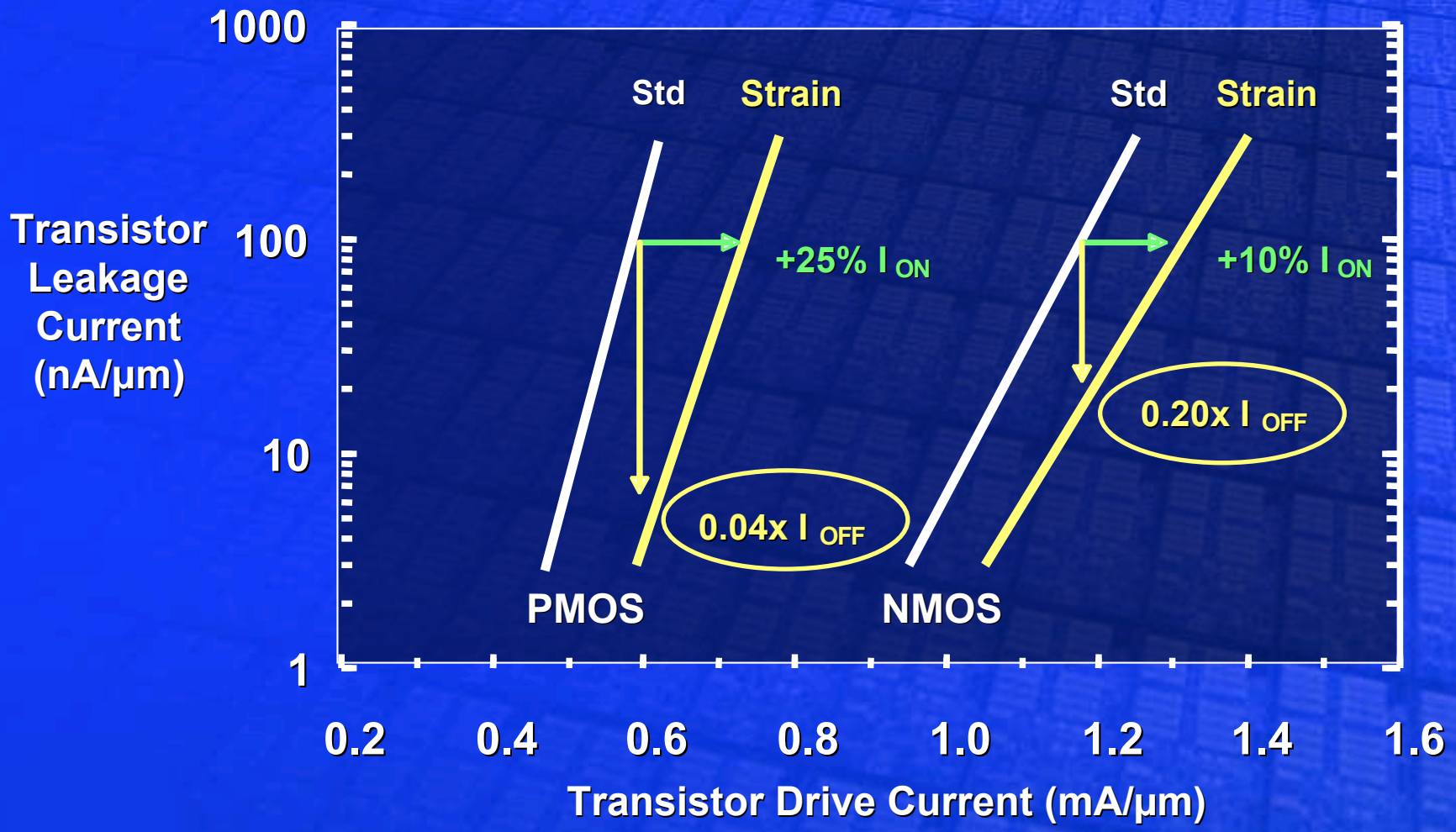
Transistor gate length ~60% of other minimum features

Key Density Indicator Continues to Scale



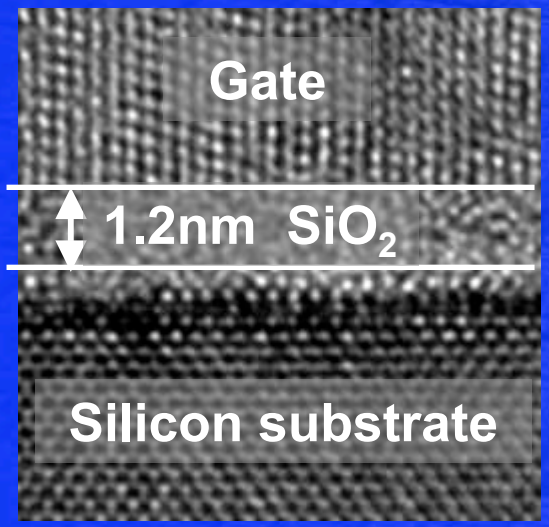
Gate pitch continues to scale 0.7x per generation, providing ~2x transistor density improvements

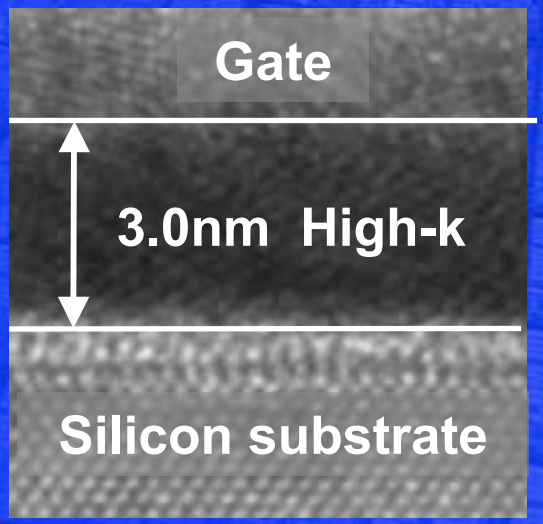
Strained Silicon Improves Transistor Performance and Leakage Today



Source: Intel

High-k Dielectric Can Reduce Gate Leakage Tomorrow





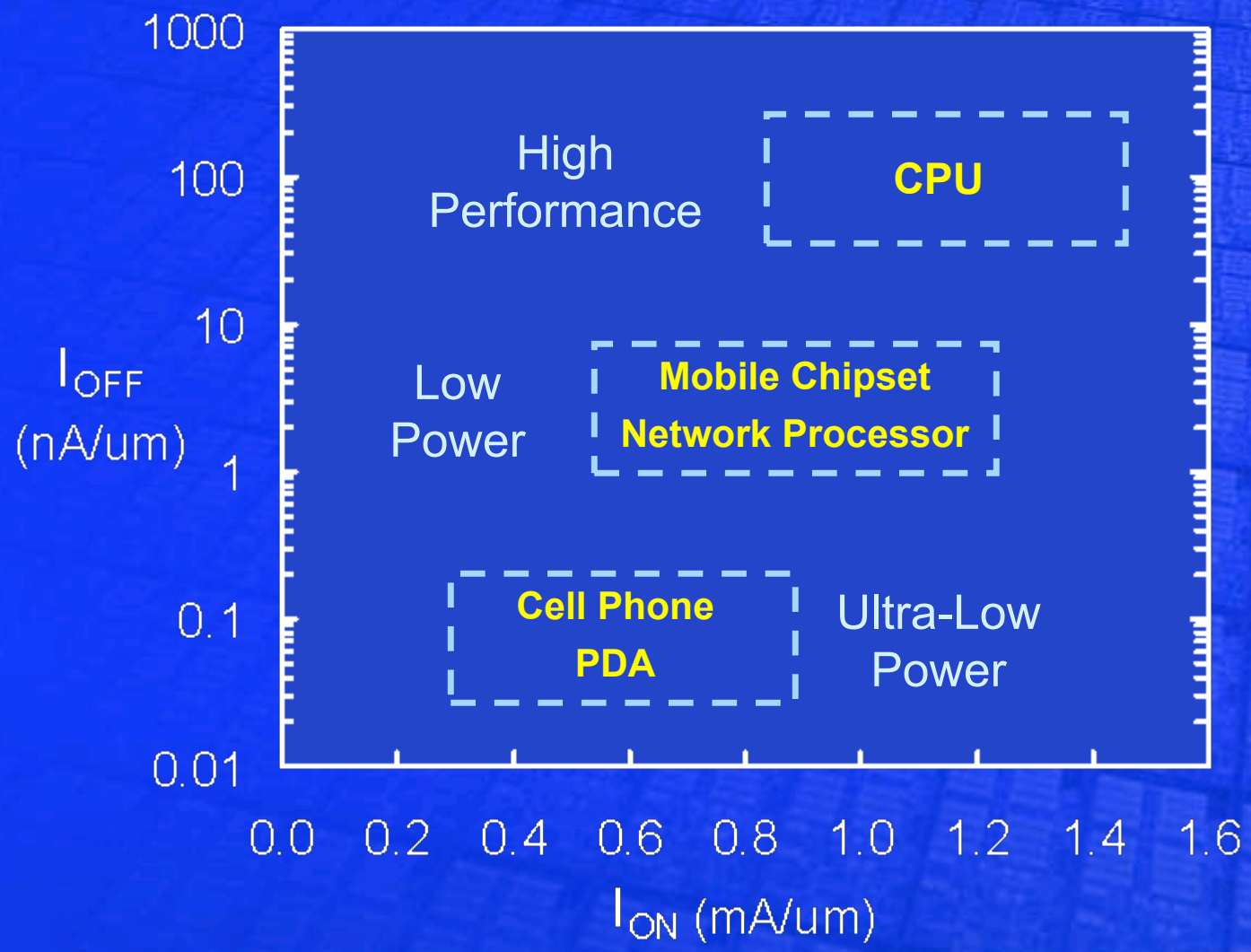
	High-k vs. SiO_2	Benefit
Gate capacitance	60% greater	Faster transistors
Gate dielectric leakage	> 100x reduction	Lower power

Process integration is the key challenge

Source: Intel

Transistors Require Optimization to the Application

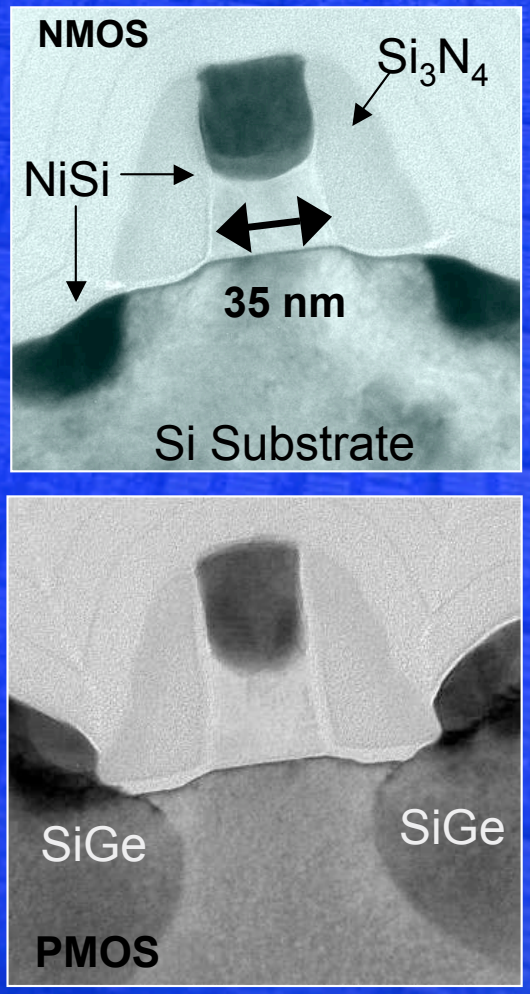
Performance vs. Leakage



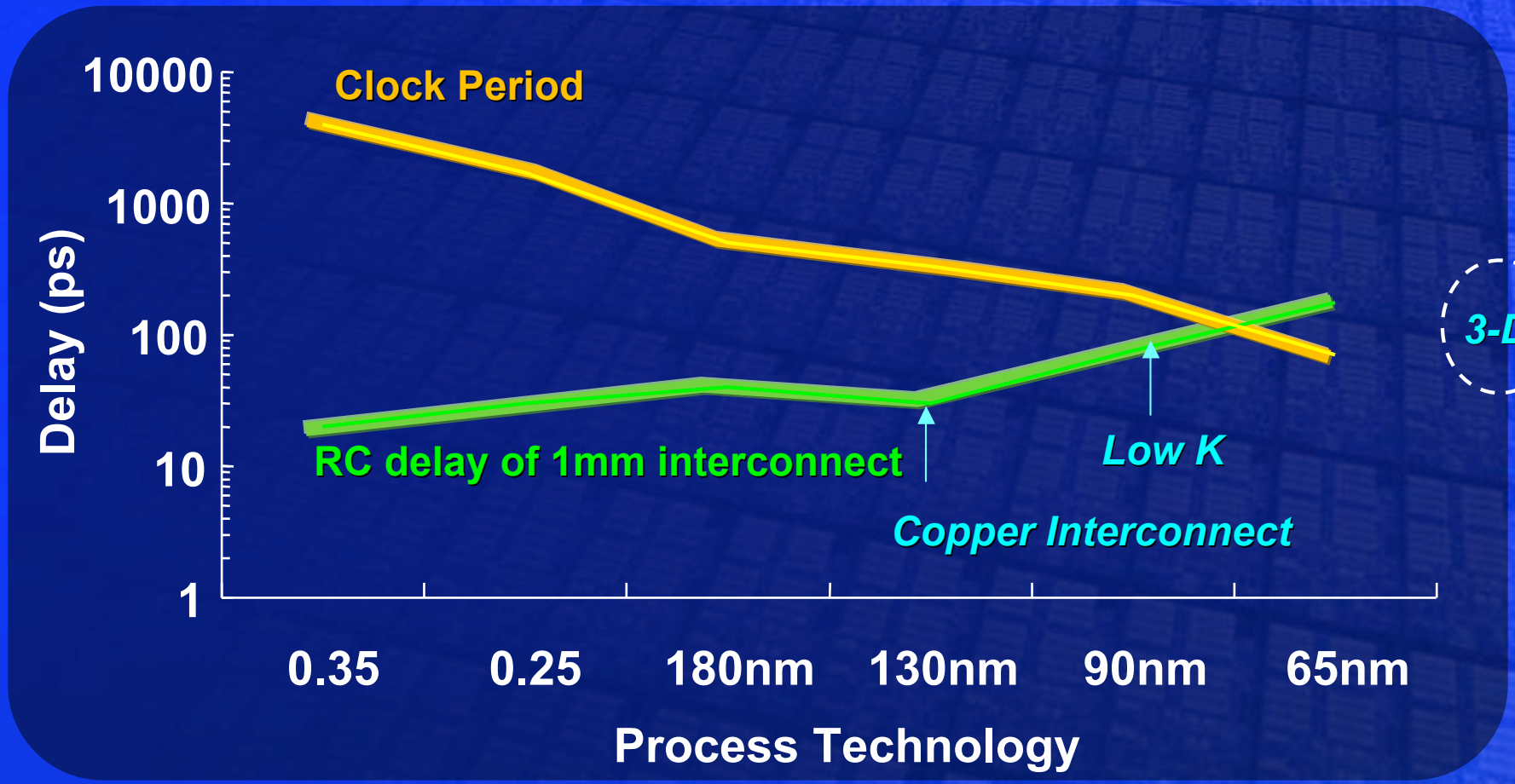
Optimized transistors can provide ~1000x lower leakage

65 nm Generation Transistors Today

- 35 nm gate length
- 1.2 nm gate oxide
- 220 nm gate pitch
- NiSi for low resistance
- 2ND generation strained silicon for enhanced performance/power



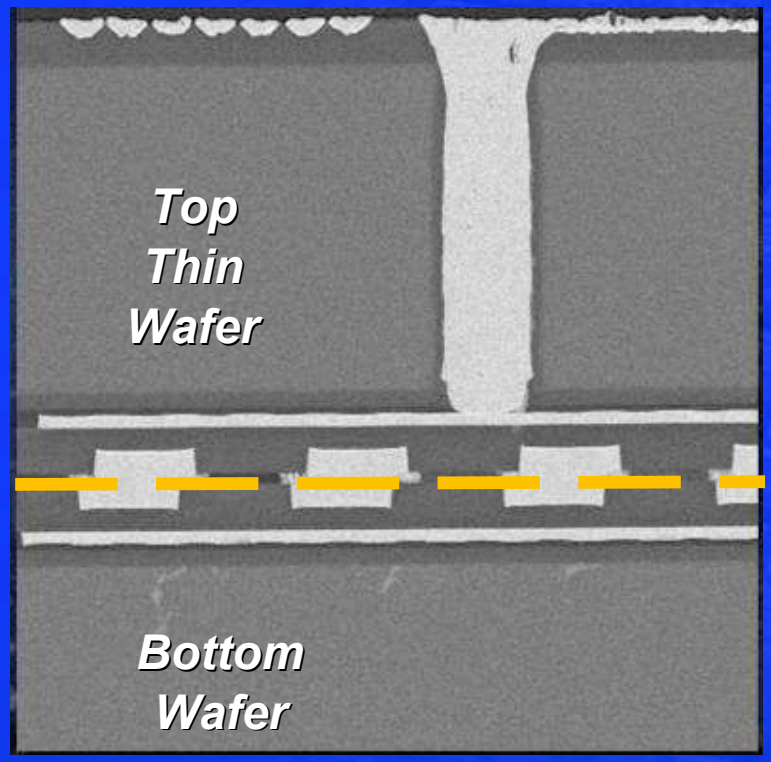
Innovations Required to Reduce Interconnect RC Challenges



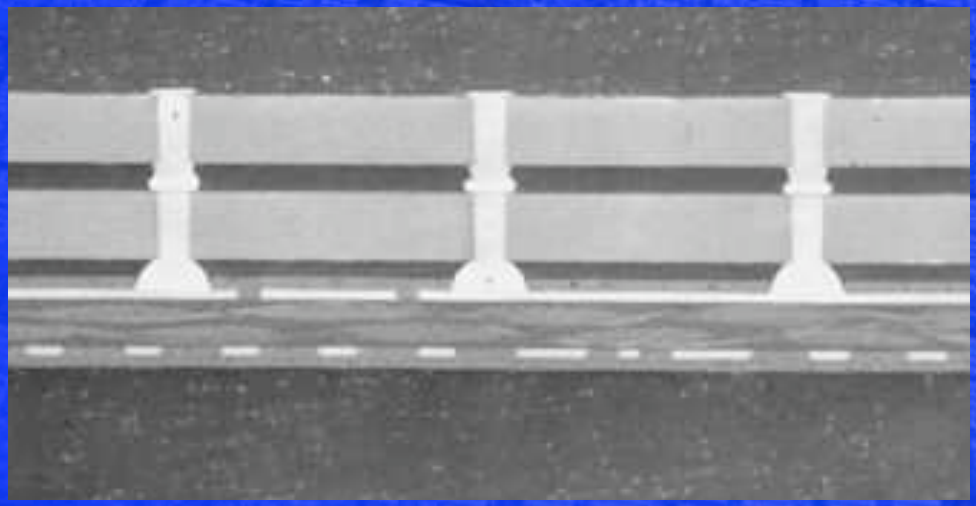
Source: IDF

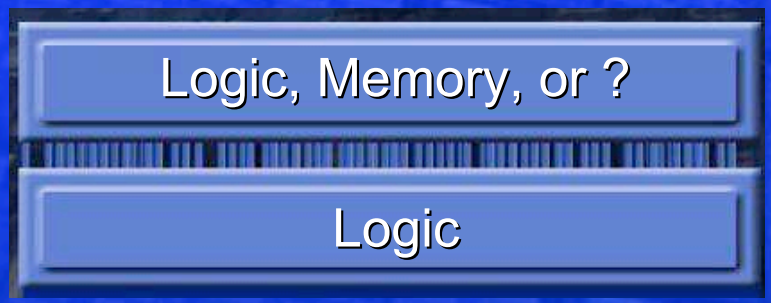
3D Silicon Stacking

Wafer



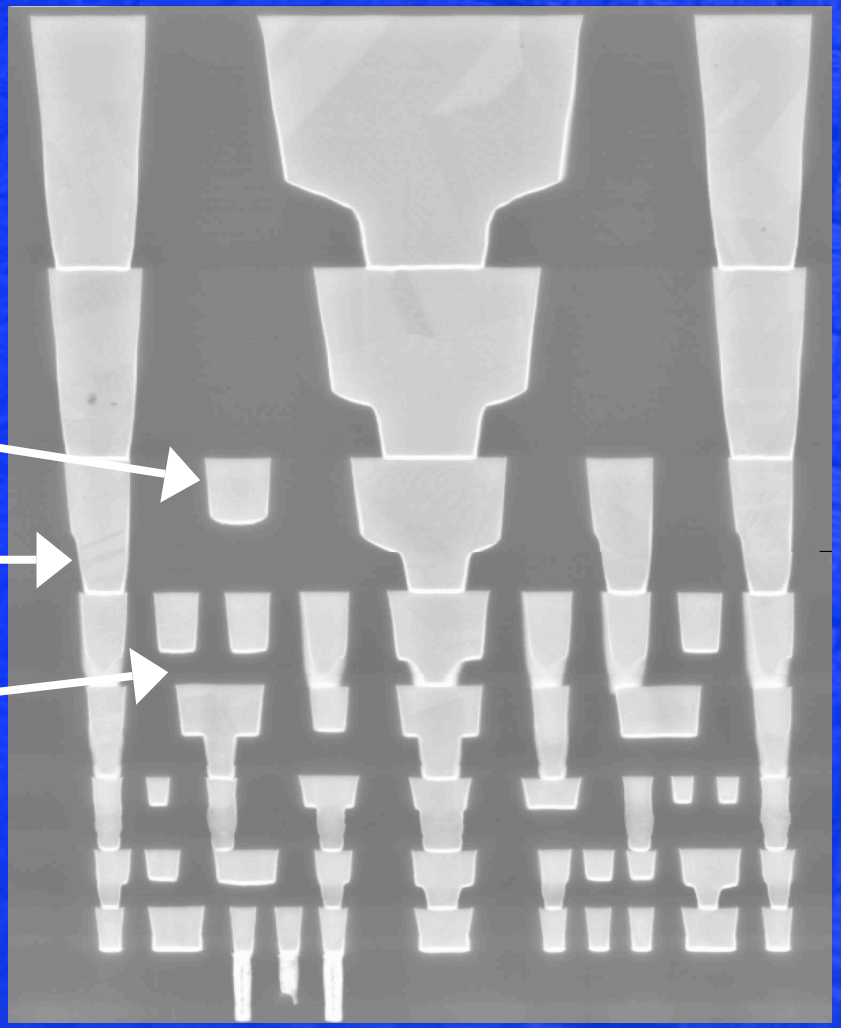
Die



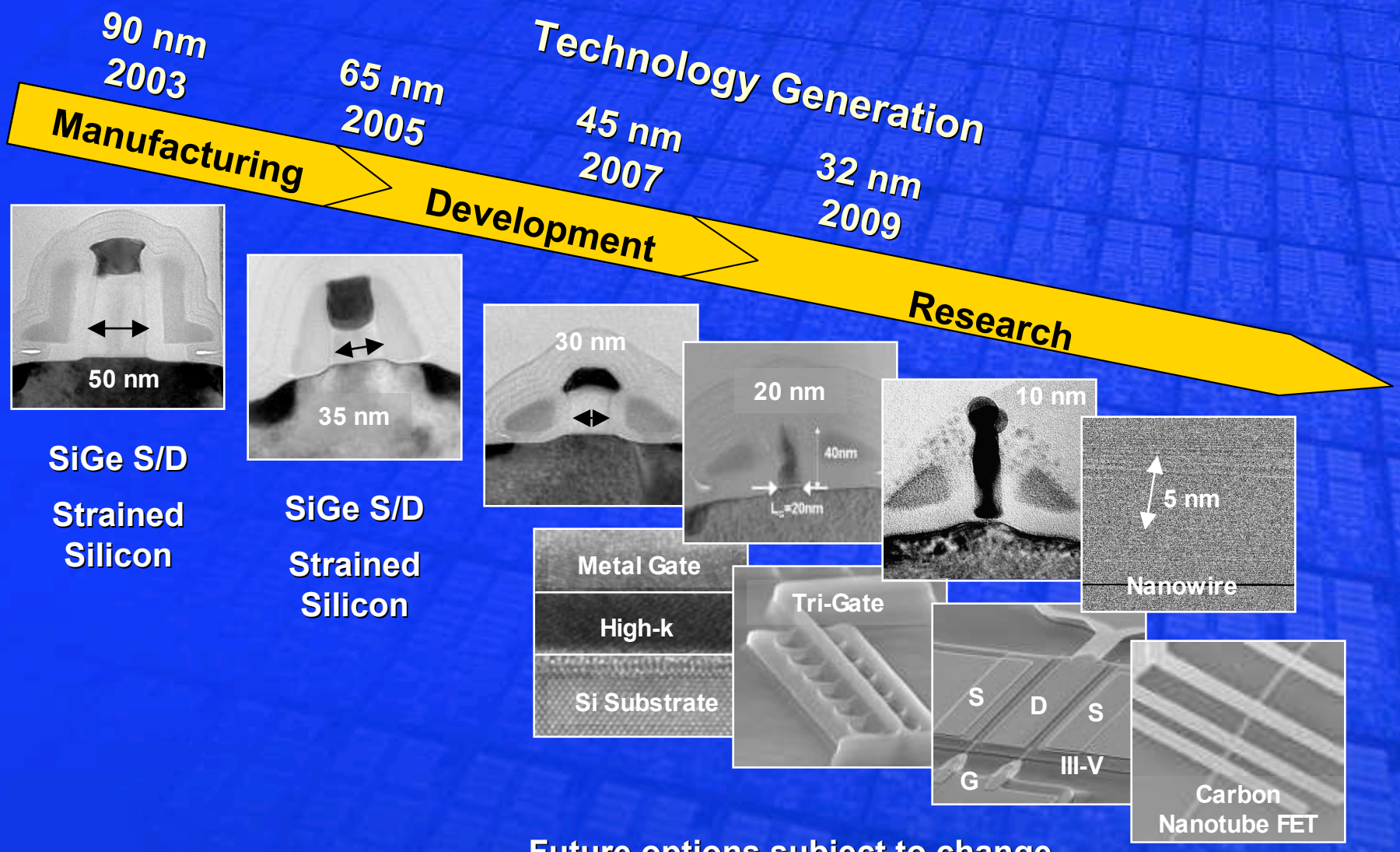


Source: Intel

65 nm Generation Interconnects



Innovation-Enabled Pipeline in Place



Future options subject to change

Source: Intel

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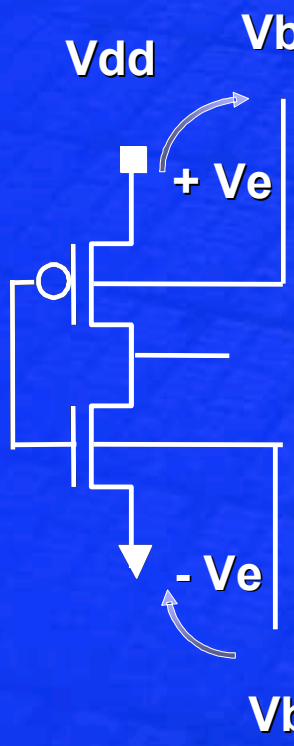
Power Reduction Techniques

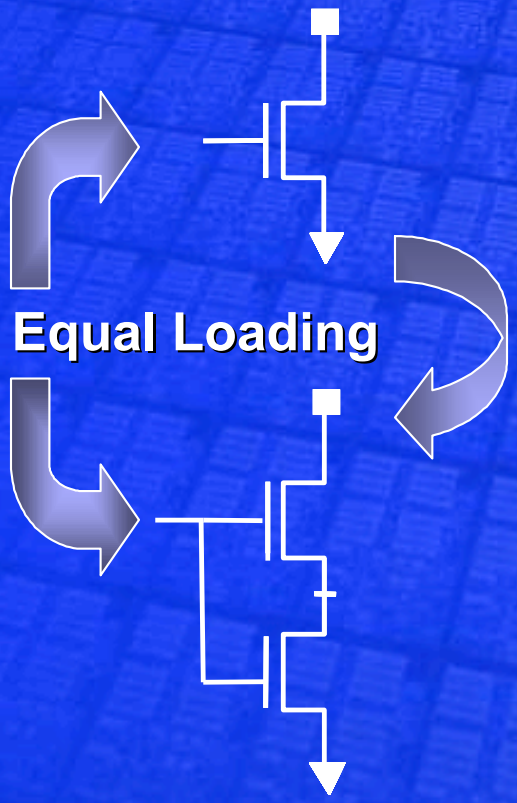
- Optimum Design
- Leakage Control
- Active Power Reduction
- Increase On-die Memory
- Multi-threading
- Dual Core and Multi-core
- Special Purpose Hardware
- Function Integration through SOC/SIP

Circuit Techniques Reduce Source Drain Leakage

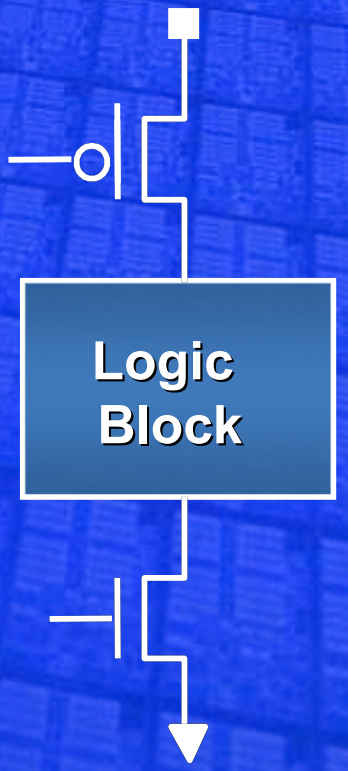
Body Bias



Stack Effect

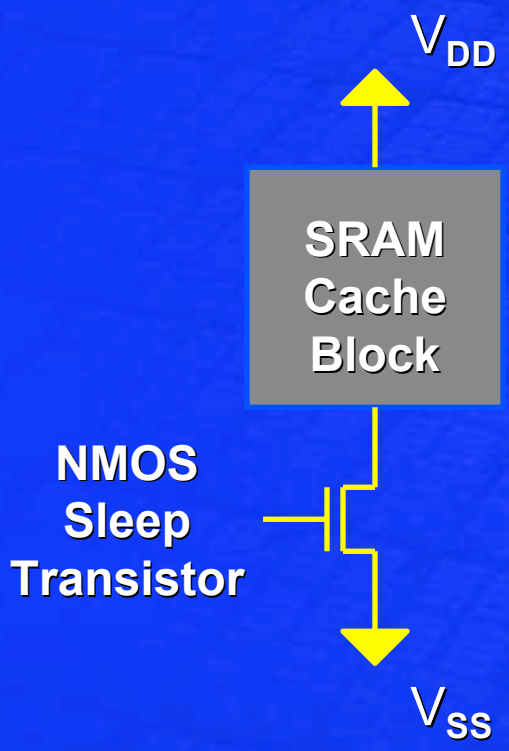


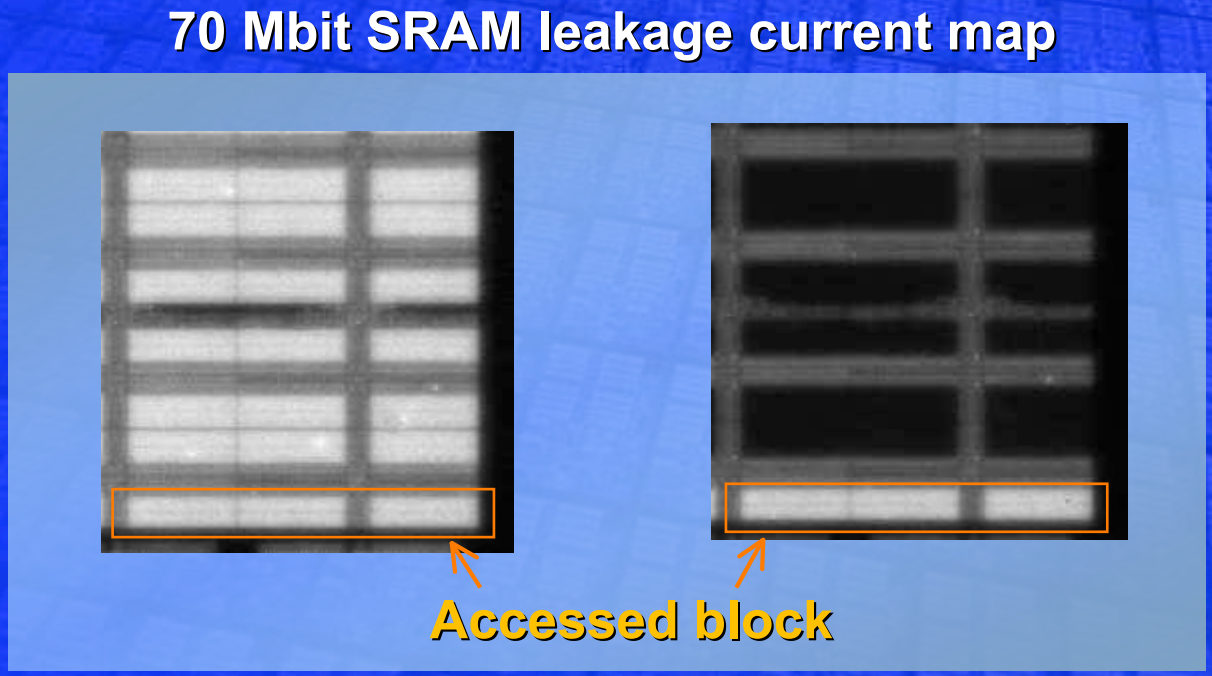
Sleep Transistor



Leakage Reduction	2 - 10X	5 - 10X	2 - 1000X

Sleep Transistor Reduces SRAM Leakage Power

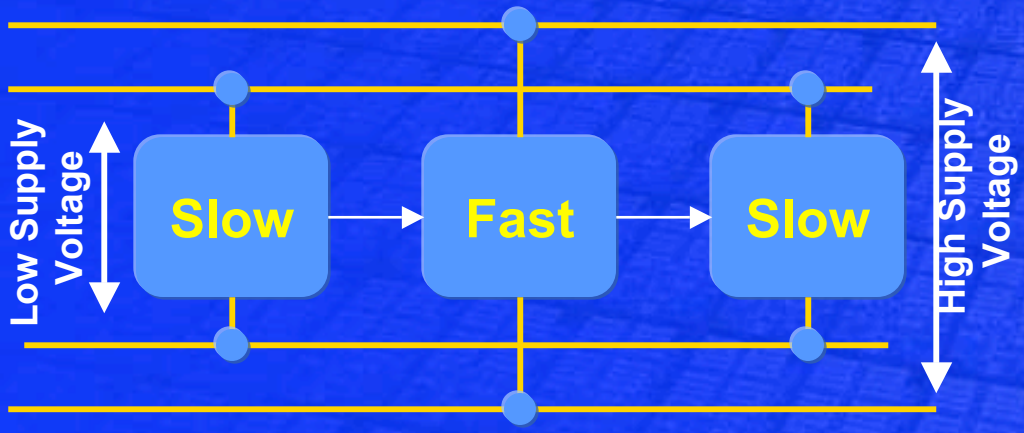




>3x SRAM leakage reduction on inactive blocks

Source: Intel

Active Power Reduction



Multiple Supply Voltages

Replicated Designs

Vdd

Logic Block

Freq = 1
Vdd = 1
Throughput = 1
Power = 1
Area = 1
Pwr Den = 1

Vdd/2

Logic Block

Logic Block

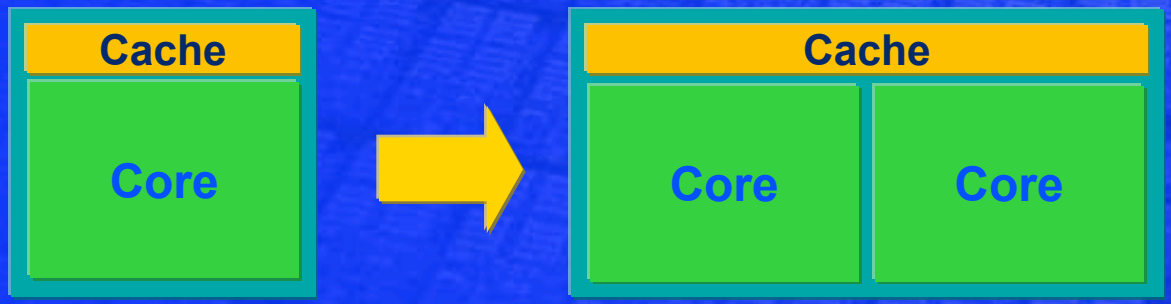
Freq = 0.5
Vdd = 0.5
Throughput = 1
Power = 0.25
Area = 2
Pwr Den = 0.125

Dual Core

Rule of thumb

Voltage	Frequency	Power	Performance
1%	1%	3%	0.66%

In the same process technology…

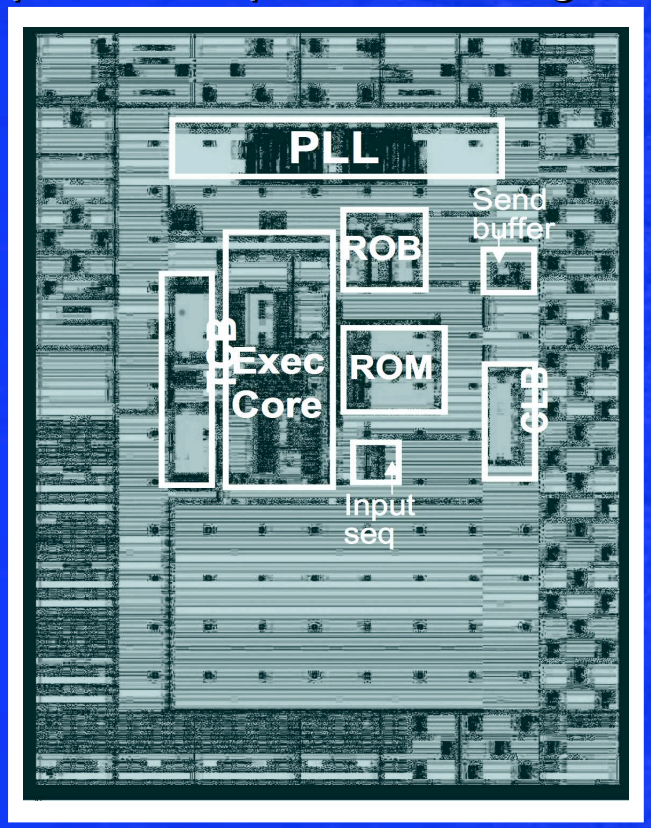


Voltage = 1
Freq = 1
Area = 1
Power = 1
Perf = 1

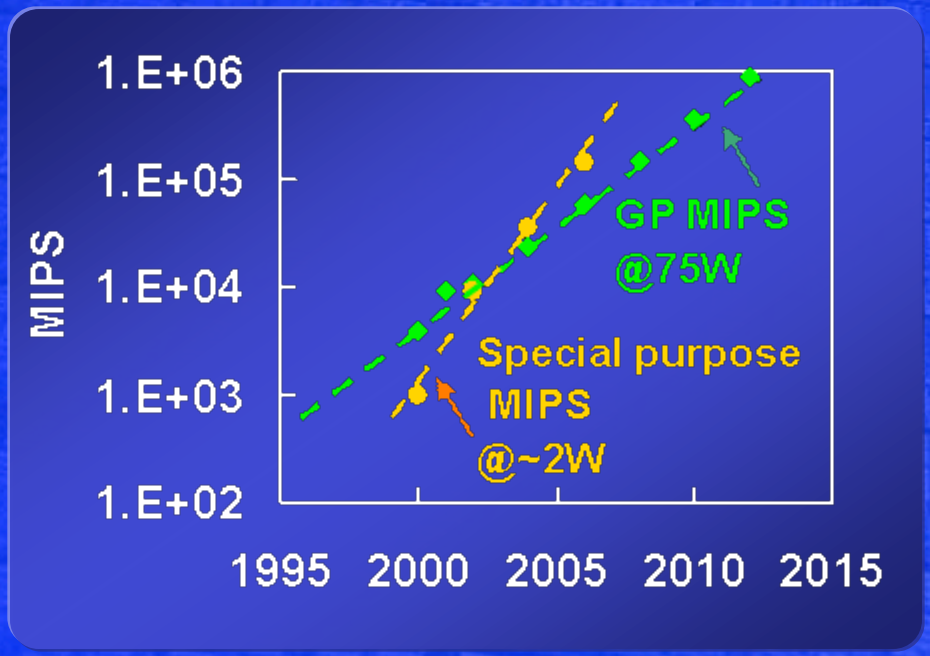
Voltage = -15%
Freq = -15%
Area = 2
Power = 1
Perf = ~1.8

Special Purpose Hardware

Special Purpose HW Engine



2.23 mm x 3.54 mm, 260K transistors



Opportunities:
MPEG Encode/Decode
Speech recognition
Graphics

Special purpose HW—Best Mips/Watt

Value of Integration

- Special-purpose hardware → more MIPS/mm²
- SIMD integer and FP instructions in several ISAs

	Die Area	Power	Performance
General Purpose	2X	2X	~1.4X
Multimedia Kernels	<10%	<10%	1.5 - 4X

Si Monolithic

Special HW

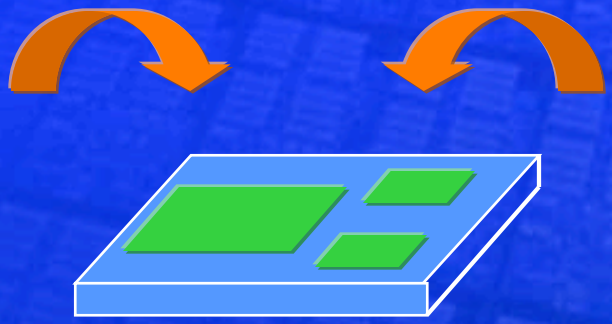
Wireline

CMOS RF

CPU

Memory

Polylithic



Heterogeneous
Si, SiGe, GaAs

Opto-Electronics

RF

Dense Memory

Joint Power Reduction Technology Roadmap

Process Technology	Dual Vt Copper	Dual Vt (Le) Strain engineering Low K ILD	FinFET (Tri-Gate) Metal Gate 3D
Circuits and Design	Sizing Clock gating	Sleep transistors Stack effect Multiple supply voltages Body Bias	
Micro-Architecture	Shallower pipelines Large caches Multi-threading	Multi-threaded Multi-core Increasing multi-processing Special purpose HW	

Future options subject to change

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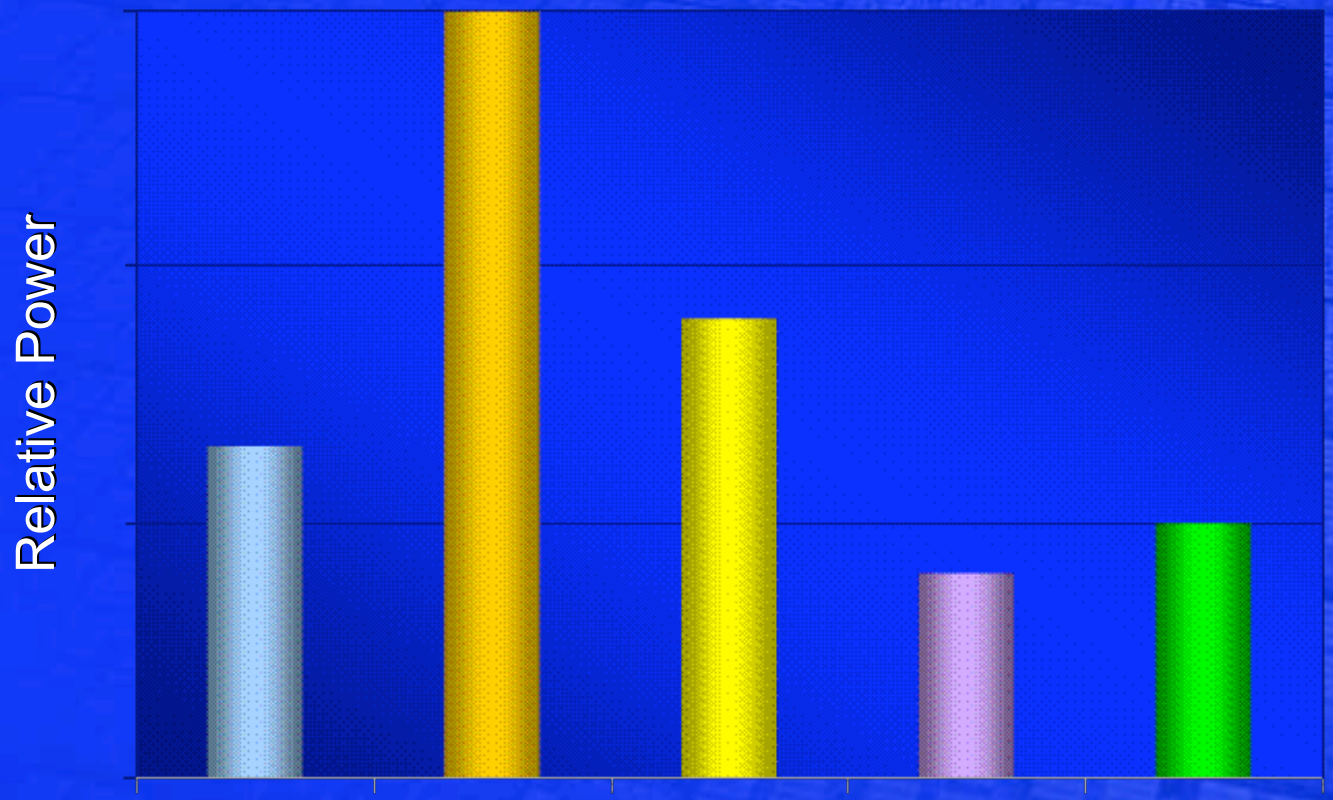
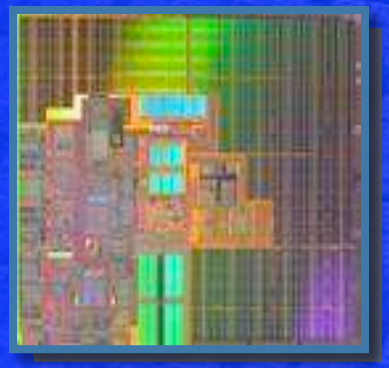
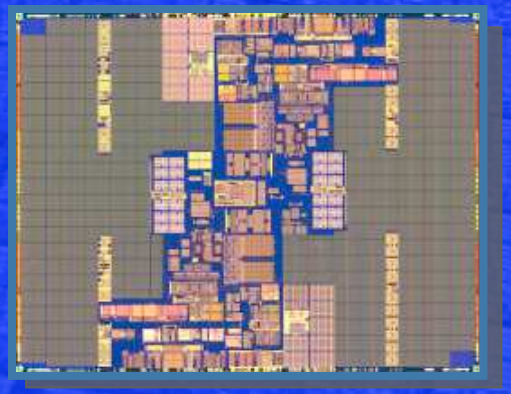


… and it works





	130 nm Madison	90 nm Montecito	
Cores/Threads	1/1	2/4	
Transistors	0.41	1.72	Billion
L3 Cache	6	24	MByte
Frequency	1.5	>1.7	GHz
Relative Performance	1	>1.5x	
Thermal Design Power	130	~100	Watt

Source: Intel

Conclusions

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Thank you