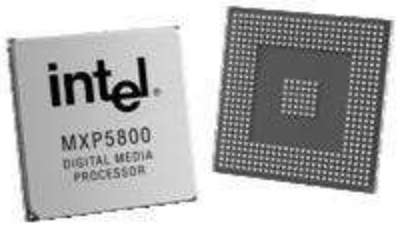
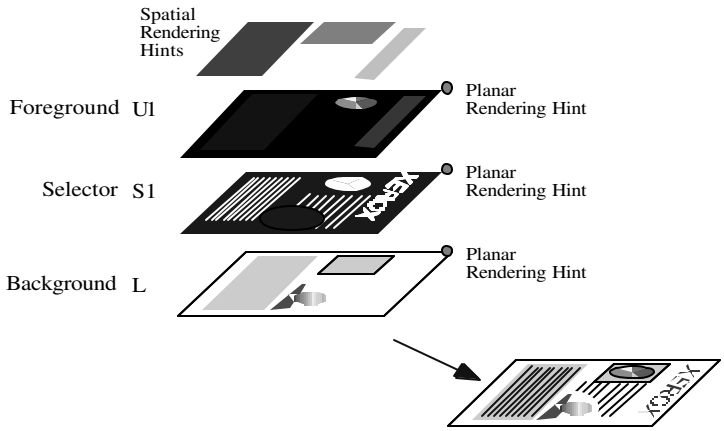
Architecture of the Intel® MXP5800 Digital Media Processor



Lou Lippincott, Chief Architect
Arup Gupta, Chief Technology Officer
Glenda Dorchak, VP and General Manager
Consumer Electronics Group

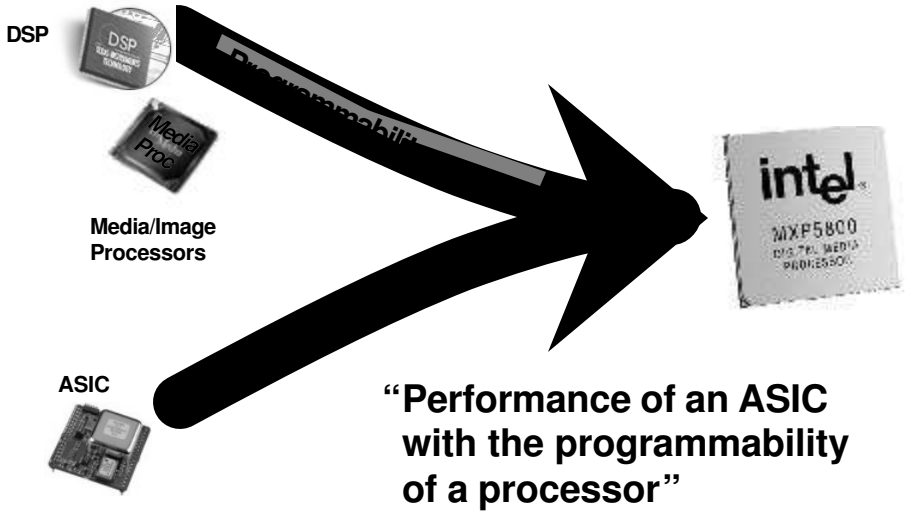
MXP5800 Application Space

- **Document Processing (Segmentation Algorithm)**



High-efficiency is achieved from limiting the application space

MXP5800/5400
Architectural Objectives



"Performance of an ASIC with the programmability of a processor"

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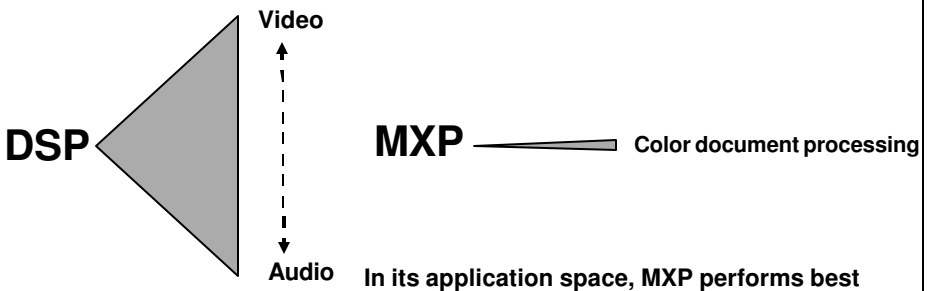
Architectural Tradeoffs

- **Flexibility - for performance**
  - **Limited re-configurability in small PEs**
- **Large application space - for efficiency**
  - **Example: MXP5800 does not do Video Processing (well)**



In its application space, MXP performs best

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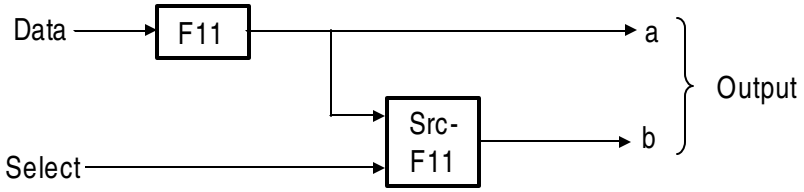
MXP5800 Architecture Efficiency

- **Architecture Benchmarking Example**
  - **Compare MXP-5800 HWAs to 128-bit SIMD engine**
    - **Single Tap Filter and Variable Tap Filter units**
      - **121 (11x11) input samples of Data processed for each "a" output**
      - **121 (11x11) "a" outputs used for each "b" output**
        - **14,641 F11 operations**
      - **Filter tap on "b" output can change on a pixel-by-pixel basis**
      - **Select allows ¼ tap increments**
      - **normalized and interpolated "b" outputs**



128-bit SIMD = 14,500 clocks **MXP5800 = 10 clocks**

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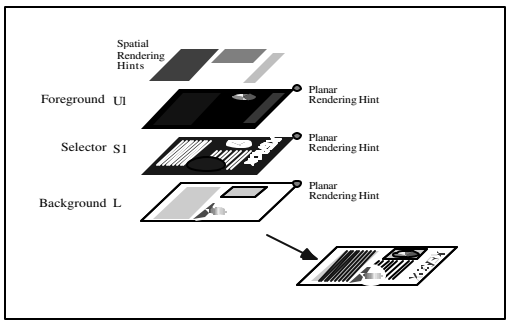
MXP5800 Performance

- **Segmentation algorithm example**
  - **Segmentation algorithm separates documents into image planes**
    - **Allows different compression techniques for each plane (image type)**
    - **Gives very high compression ratios**
    - **Very complex, data-intensive algorithm**



- **Runs on one MXP5800**
  - **Performs @ 12ppm**
  - **Less than 3W typical**
  - **Easily scaled to multiple chips**
- **Replaces ~8 competitive parts**
  - **(More general-purpose arch)**
  - **(Supported by C compilers)**

High-efficiency is achieved from specialization

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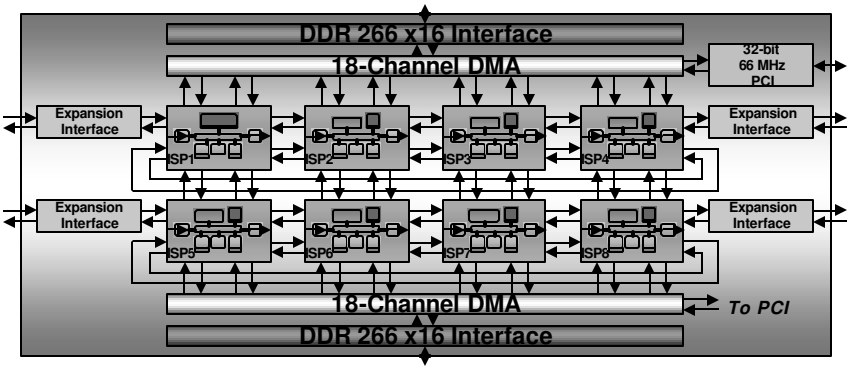
MXP5800 Architecture Overview

- MXP5800 is a high performance image/media processor
  - 8 MIMD processing engines connected by a streaming mesh
  - Each MIMD engine has five 16-bit ALUs with dual MAC units
    - Total of 40 ALUs & 16 MACs
  - 36 channels of DMA supporting dual banks of DDR
  - PCI and Expansion Interfaces for data movement
  - Hardware assist for filtering and compression



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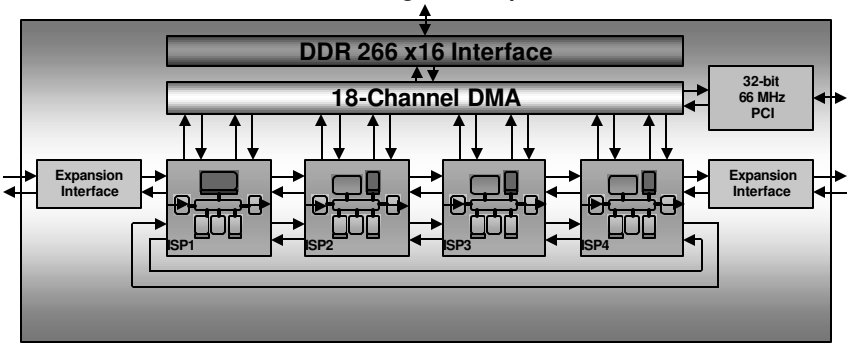
MXP5400 Architecture Overview

- MXP5400 is a high performance image/media processor
  - 4 MIMD processing engines connected by a streaming mesh
  - Each MIMD engine has five 16-bit ALUs with dual MAC units
  - Total of 20 ALUs & 8 MACs
  - 18 channels of DMA supporting dual banks of DDR
  - PCI and Expansion Interfaces for data movement.
  - Hardware assist for filtering and compression



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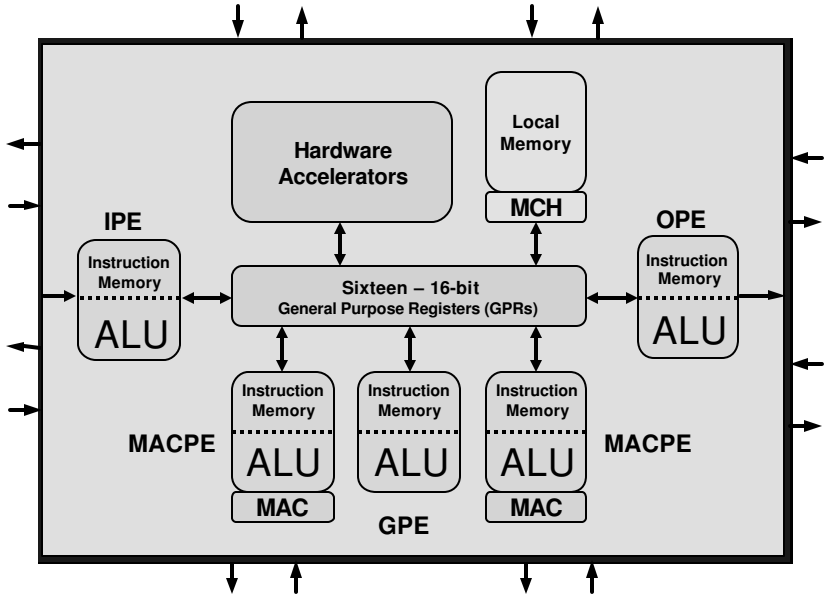
Detailed ISP Overview



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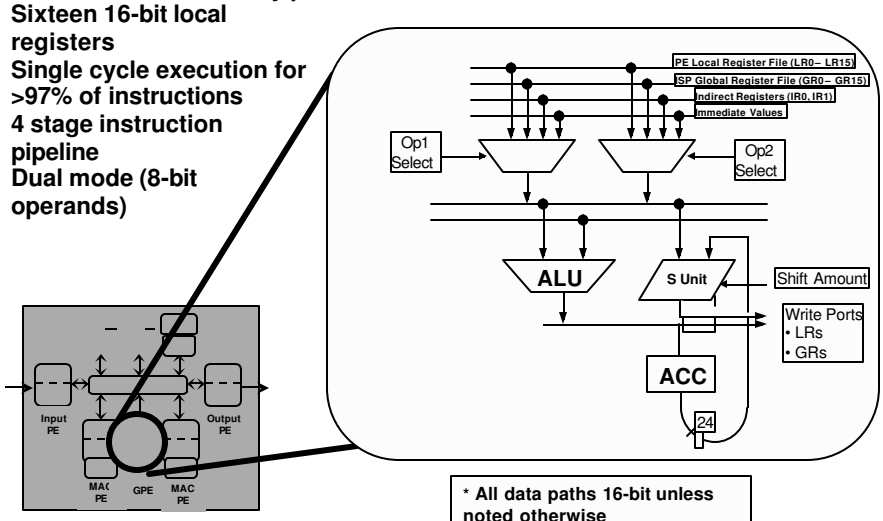
GPE Architecture

- All PEs run the same baseline instruction set
- 128 instruction memory per PE
- Sixteen 16-bit local registers
- Single cycle execution for >97% of instructions
- 4 stage instruction pipeline
- Dual mode (8-bit operands)



* All data paths 16-bit unless noted otherwise

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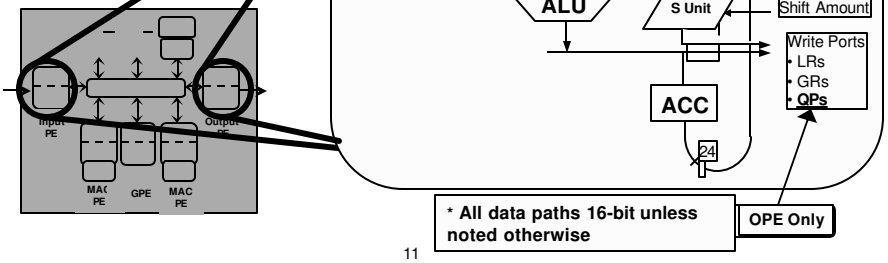
IPE/OPE Architecture

- Same core architecture as GPE but with direct interfaces to the Quad Ports
- IPE provides read access to Quad Ports
- OPE provides write access to Quad Ports
- Quad Port references made through instruction source/destination value



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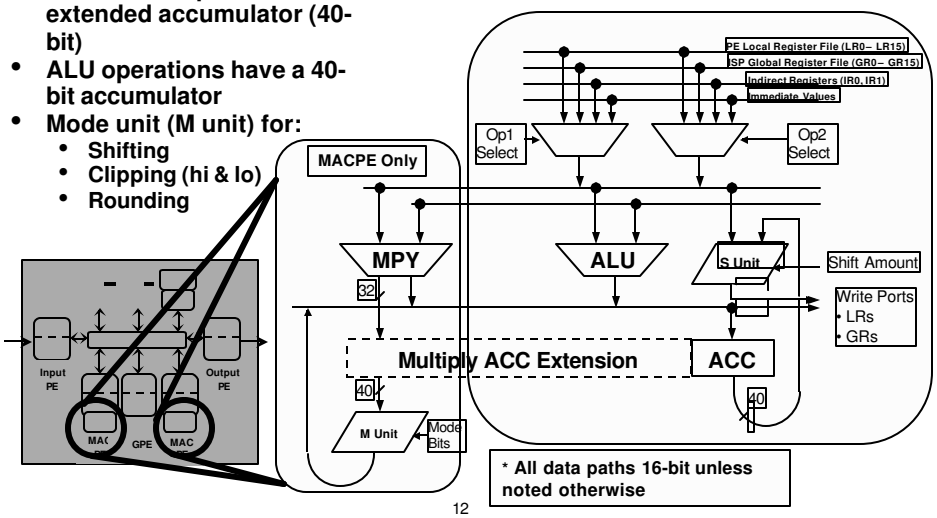
MACPE Architecture

- MACPE has same core architecture as GPE but with a 16x16 multiplier and an extended accumulator (40-bit)
- ALU operations have a 40-bit accumulator
- Mode unit (M unit) for:
  - Shifting
  - Clipping (hi & lo)
  - Rounding



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PE Instruction Set Summary

All PE Baseline Instructions

ALU ops:
absolute, add, clear, logical ops, min/max, mux, mode, nop, pack/unpack, read/write instruction memory, store acc, shift, subtract, test bit

Data movement:
load

Control ops:
call/rtn, interrupt, compare, jump, loop, repeat, stop

MACPE 16 x 16 Multiplier

Multiplier:
basic multiply, multiply/accumulate (MAC), output modes

GPE bit rotation

Bit rotation:
Extract one bit and load in another register at specified bit location.

IPE/OPE Quad Port access

Quad Port access:
access provided by quad port operands

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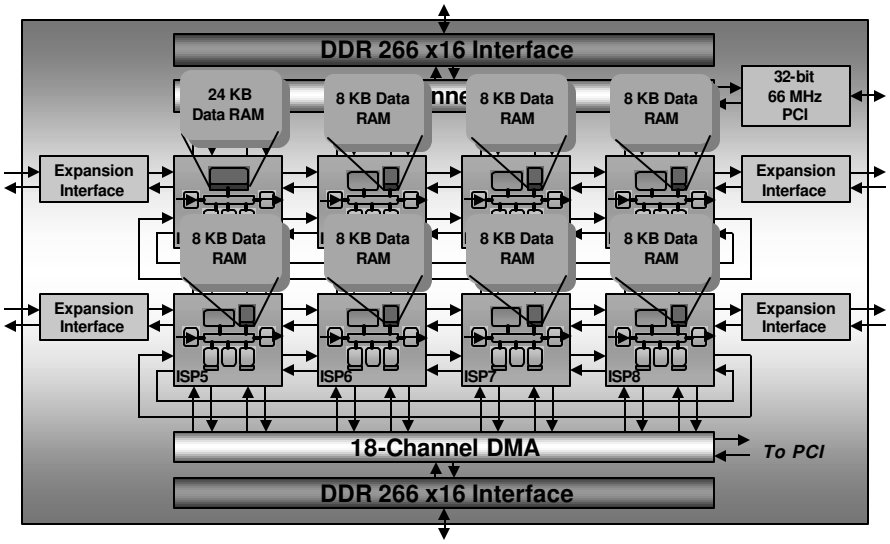
On-Chip Local Memory



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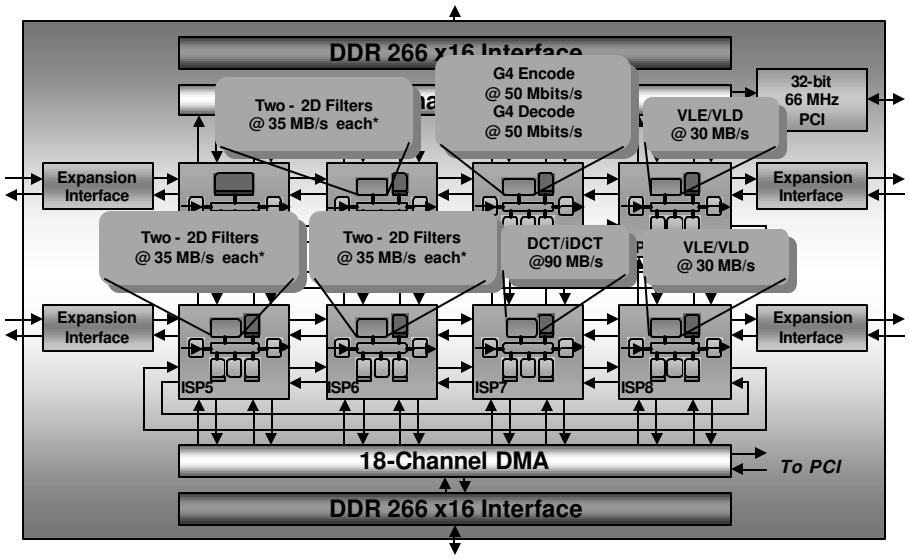
Hardware Accelerators



*These are average performance numbers.
Performance varies depending on the input data.

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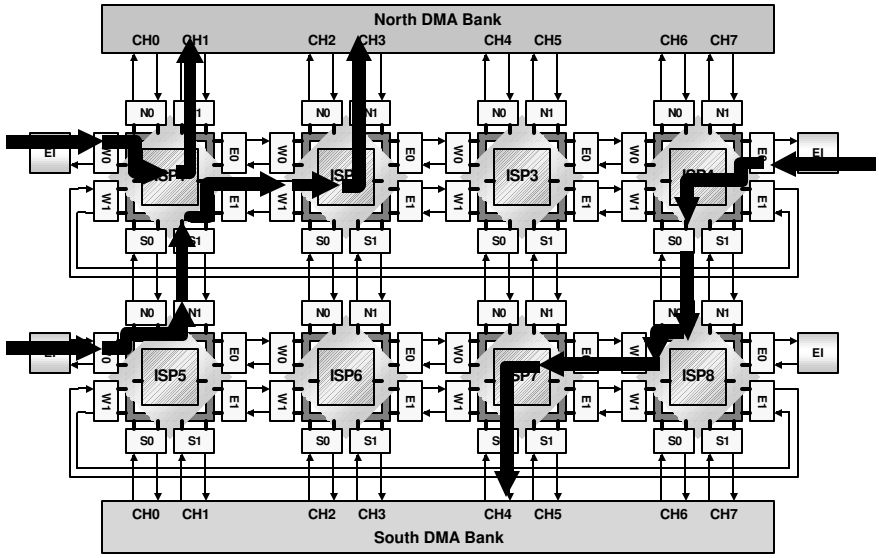
EI and Quad Port Routing Example



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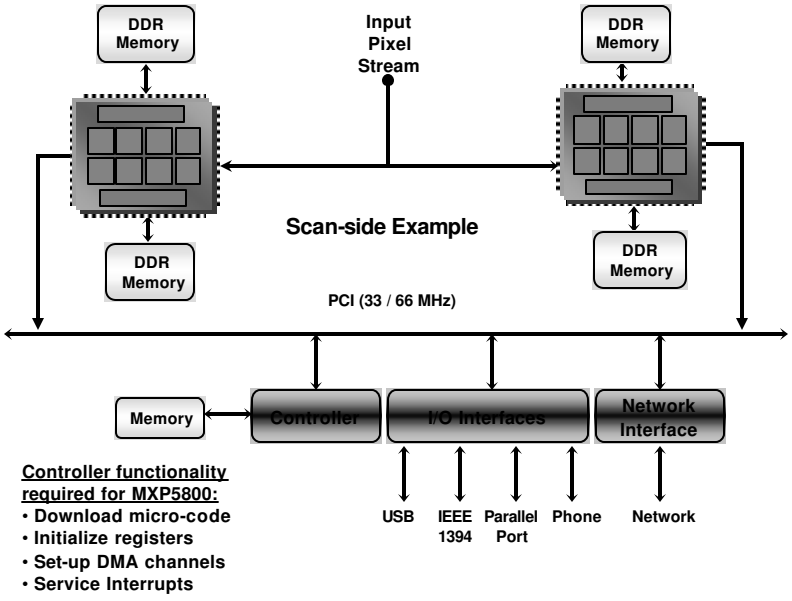
MXP5800 is a Scalable Architecture



Controller functionality required for MXP5800:

- Download micro-code
- Initialize registers
- Set-up DMA channels
- Service Interrupts

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MXP5800 Architectural Summary

- 40 independent parallel resources
  - Optimized for the processing of image / media data
- Hardware acceleration
  - VTF, STF, G4, VLE, IDCT/DCT
- High performance streaming mesh network
  - Dynamic links allow maximum system performance
- Scaleable architecture
  - From 1 ISP to multiple chips

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Questions?

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