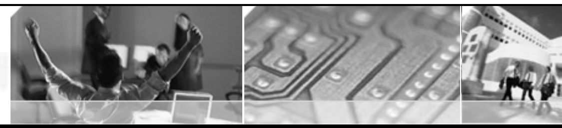
one radio multiple networks



Single Chip CMOS Direction Conversion Transceivers for WWAN and WLAN

Tajinder (Taj) Manku
tmanku@sirific.com

 CONFIDENTIAL www.sirific.com

Introduction

I. Market Requirements

II. Receiver Architectures

III. Sirific's Virtual LO™

IV. Transmitter Architectures

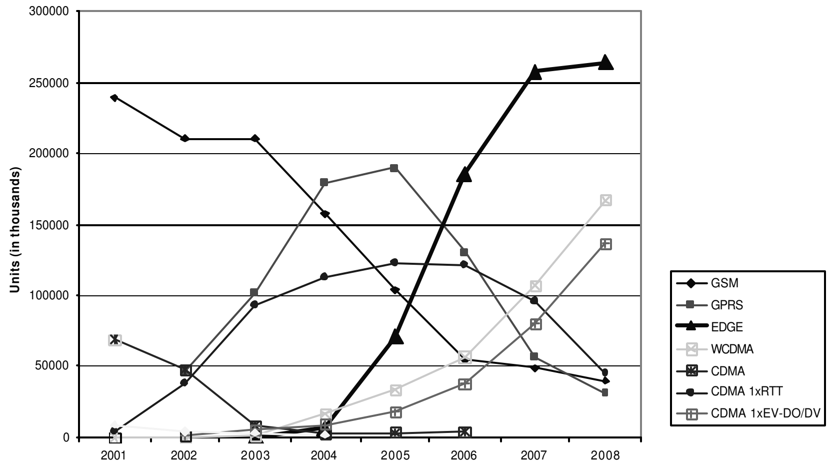
V. Sirific's Transceiver Platform and Implementation

VI. Conclusion

© Copyright Sirific Wireless Corporation 2002 CONFIDENTIAL www.sirific.com

Cellular Market Forecasts

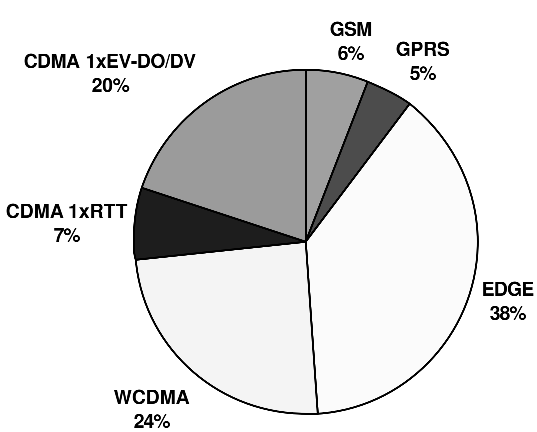
Wireless Market Forecasts by Standard



Source: Deutsche Bank (Jan 2004)

Cellular Market Forecasts

2008 Wireless Market Forecast by Standard

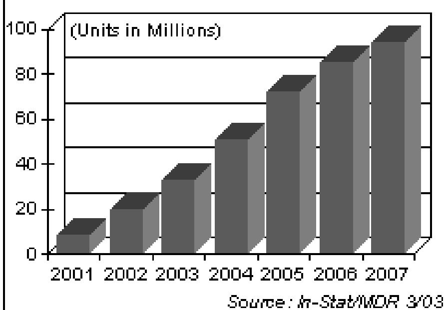


- **EDGE + WCDMA market will account for 62% of the overall worldwide wireless market**
- **GSM, GPRS, EDGE and WCDMA combined will dominate the cellular market share**

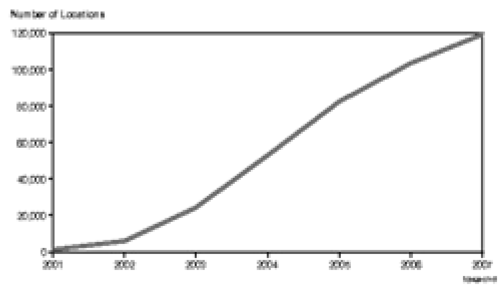
© Copyright Sirific Wireless Corporation 2002 CONFIDENTIAL www.sirific.com

WLAN Market Forecasts

Worldwide WLAN Chipset Units

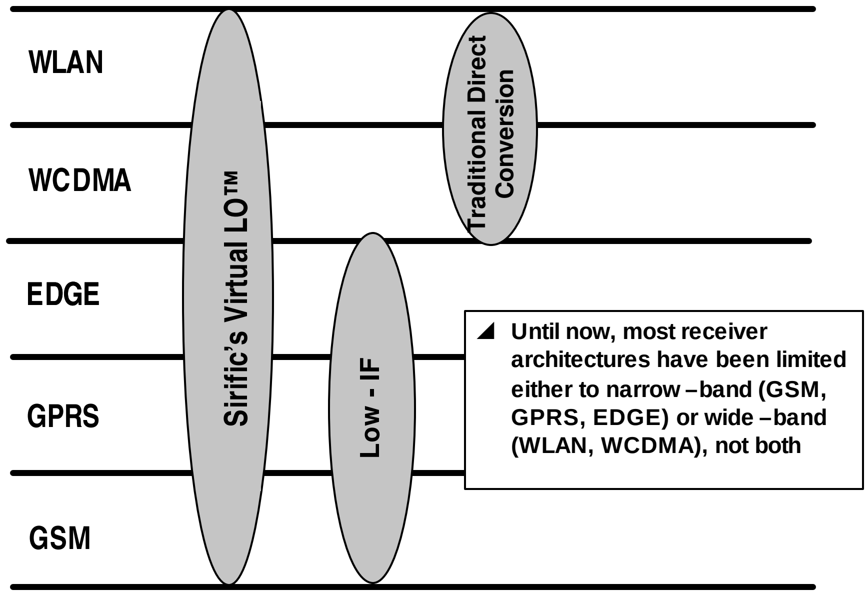


WLAN Hotspot Locations



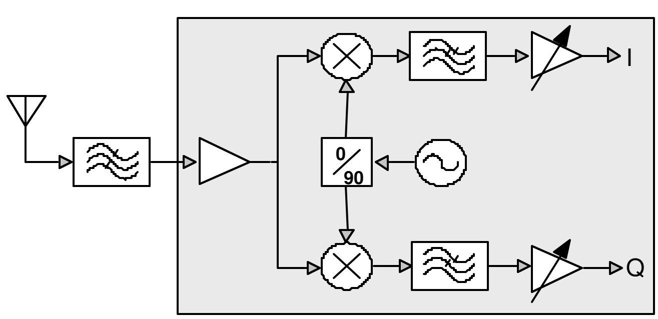
- **Predominant increase in WLAN Hotspot locations as well as WLAN chipset units in the next few years**
- **Expected that 50% of units by 2006 will be multi-standard (802.11a/b/g)**
- **Cellular and WLAN market trends are driving for multi –standard, multi –band devices**

Receiver Architectures Implemented in CMOS



Receiver Architecture – Direct Conversion / Zero-IF

- **Advantages**
  - Highly integrated
  - Platform for all bands and standards
- **Disadvantages**
  - DC offsets
  - 1/f Noise issues in CMOS



DC Offset Issues in Direct Conversion Radios

- **DC offsets are common problem for direct conversion architectures and result from 5 physical effects:**
  - RF leakage
  - LO-RF leakage
  - IIP2 (second order distortion) → Very bad for CMOS because of bad switching characteristics
  - Thermal DC offset
  - 1/f noise →Limiting factor for Direct Conversion CMOS

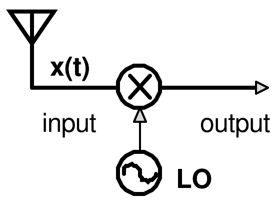
DC Offset Issues in Direct Conversion Radios

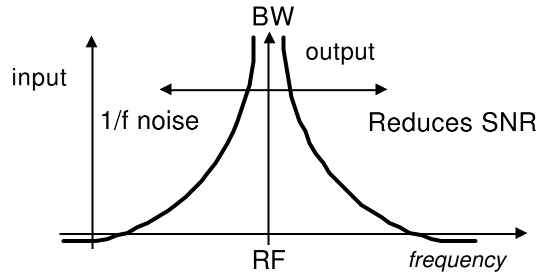
- **In order for IIP2 to be a "stable" measurement value, the following condition should hold:**

  (input referred second order harmonic) > (LO leakage level reference to the input)

LO leakage = -99dBm	**IM2 = -60 dBm**	**IIP2 "stable"**
LO leakage = -66dBm	**IM2 = -120 dBm**	**IIP2 "unstable"**

1/f Noise in CMOS Circuits for Direct Conversion

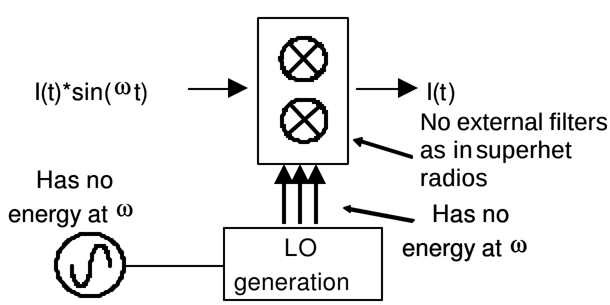




- **More important in CMOS**
- **Limiting factor for GSM/GPRS/EDGE direct conversion CMOS**
- **No "potential" fixes in CMOS**
  - 1/f noise is more significant in CMOS technology
  - 1/f noise arises at baseband due to the switching of transistors in the mixers
    (Darabi & Abidi, IEEE SSC, vol. 35, p 15, 2000)

LO Generation

- **LO generation is the generation of signal(s) to down convert the RF signal without corrupting the data**
- **Some contributors of DC offset can be combated with LO generation**



I. Market Requirements

II. Receiver Architectures

III. Sirific's Virtual LOTM

IV. Transmitter Architectures

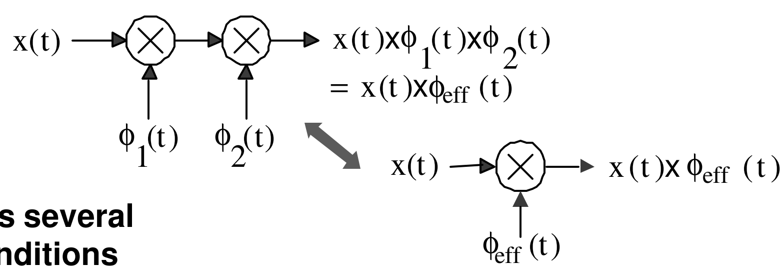
V. Sirific's Transceiver Platform and Implementation

VI. Conclusion

Virtual LO™ - Sirific's Solution for LO Generation

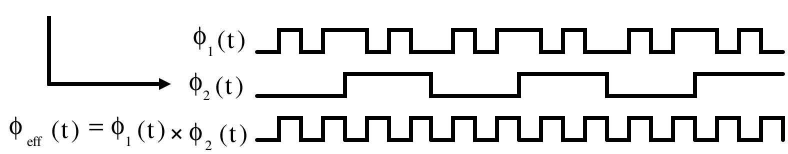
- **Sirific's Virtual LO™ frequency planning technique eliminates the DC offset**

a)



Has several conditions

b)



I. Market Requirements

II. Receiver Architectures

III. Sirific's Virtual LO™

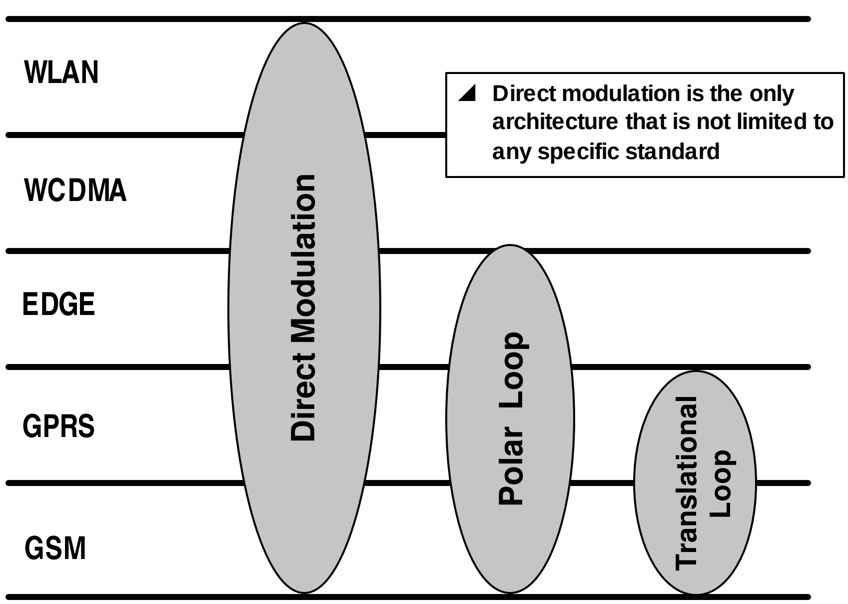
IV. Transmitter Architectures

V. Sirific's Transceiver Platform and Implementation

VI. Conclusion

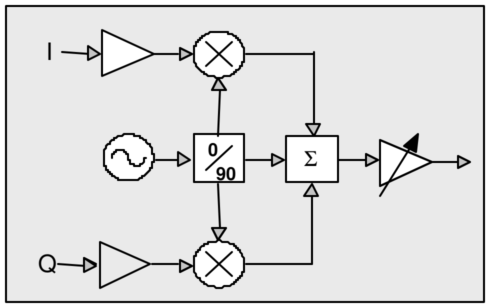
CONFIDENTIAL

Summary of Transmitter Architectures



Transmitter Architectures – Direct Modulation

- **Advantages**
  - Simple architecture
  - Wide –band
  - Single LO
- **Disadvantages**
  - Limited gain control
  - Difficult to meet noise, linearity, carrier feedthrough, and quadrature accuracy (especially in GSM)



 CONFIDENTIAL

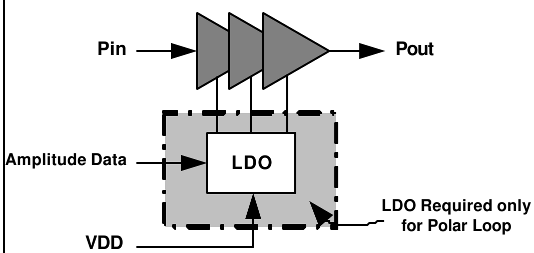
Direct Modulation vs. Polar Loop

Direct Modulation	Polar Loop
+ supports other more complex modulations (i.e. WCDMA) + no calibration or complex loops - Higher noise output (may require TX filtering/switches – filters are about <$0.20 in volume) - Requires Linear PA - Carrier feed-thru/sideband requires consideration ? Lower PA efficiency (higher power)	+ Lower noise (no TX filtering) + Add on to past GSM solutions (i.e. translational loop) - supports only some modulations - Requires calibration or complex loops that require power - May require isolators (significant size and >$1.00 in volume) - May require PA controller chip ? Higher PA efficiency (lower power)

 CONFIDENTIAL

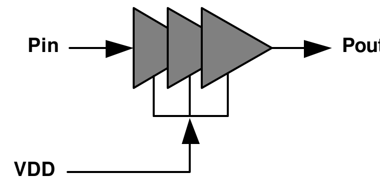
Polar Loop vs. Direct Modulation System PAE for EDGE

- **System PAE for a Polar Loop PA is limited by the LDO which is used for amplitude modulation**



System PAE < 20% including LDO) at Pout = +28dBm for Polar Loop

- **No LDO is required for Direct Modulation, and so system PAE depends only on the linear PA**



System PAE ~ 25% at Pout = +28dBm for Direct Modulation

 CONFIDENTIAL www.sirific.com

I. Market Requirements

II. Receiver Architectures

III. Sirific's Virtual LO™

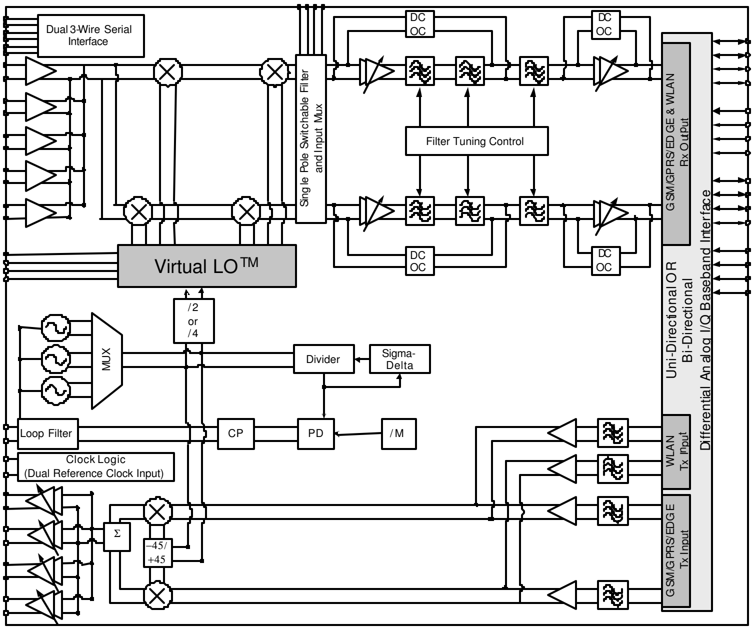
IV. Transmitter Architectures

V. Sirific's Transceiver Platform and Implementation

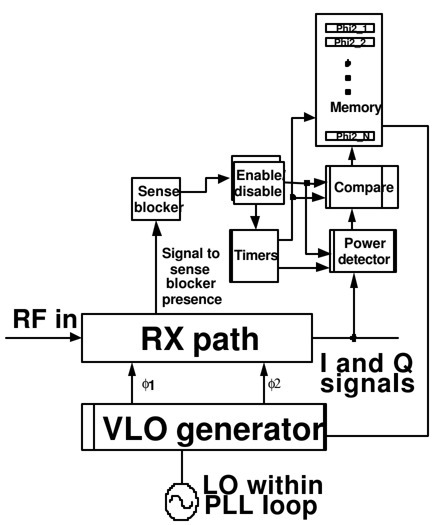
VI. Conclusion

 CONFIDENTIAL www.sirific.com

Transceiver Platform–GPRS/EDGE+802.11b/g



Virtual LO™ & Dynamic Spurious Control (DSC)

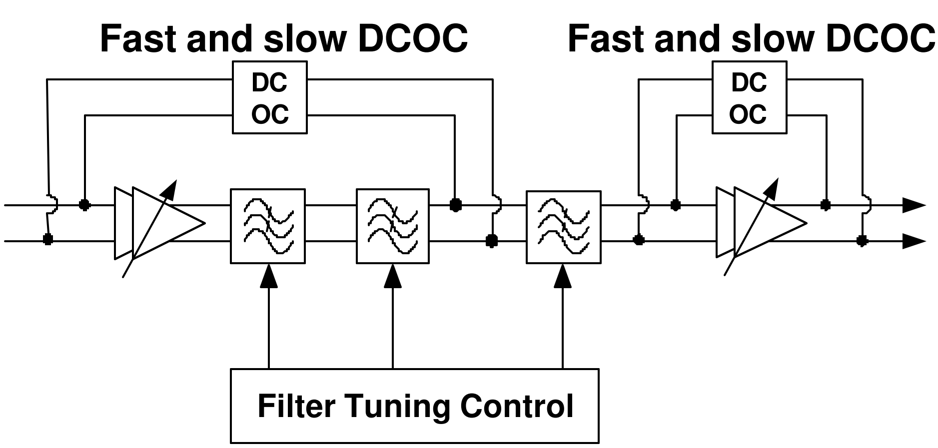


- **Dynamic Spurious Control (DSC) is used to boost radio performance in the presence of a large out-of-band blocker within a packet (i.e. for GSM)**
- **The interferer is sensed within the high frequency path and I/Q path.**
- **With these two pieces of data $\phi 2$ is modified which automatically modifies $\phi 1$.**

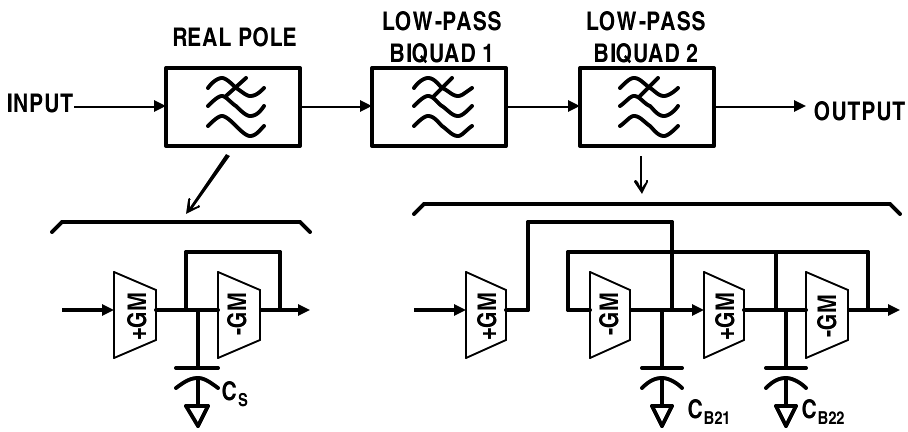
Rx total chain measurements

Receiver	850/900	1800/1900	WLAN
Noise Figure	2.8dB	3.0dB	3.5dB
LO Re-radiation	-133dBm	-103dBm	-108dBm
IQ Phase Error	< 1°	< 1°	< 1°
IQ Amplitude Error	< 0.5dB	< 0.5dB	< 0.5dB
Maximum Gain Range	95dB	95dB	80dB
IIP2 (min)	45dBm	54dBm	66dBm
∆NF with -26dBm Blocker @ 3MHz	4dB	4dB	-
LNA Power	18mW	18mW	18mW
Mixer Power	41mW	41mW	41mW

Gm-C Baseband Filter, VGA and DCOC



Gm-C Capacitor Assignments



© Copyright Sirific Wireless Corporation 2002 CONFIDENTIAL www.sirific.com

Gm-C Baseband Filter, VGA and DCOC

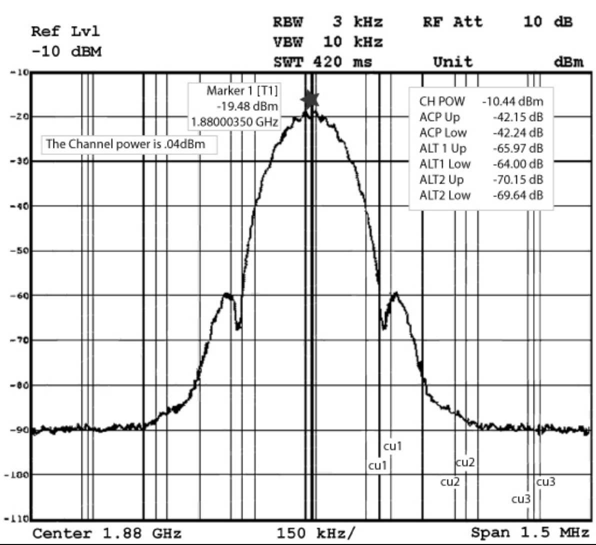
Baseband Filter	850/900	1800/1900	WLAN
3dB Bandwidth	204kHz	204kHz	7.3MHz
Rejection	64dB @ 600kHz	64dB @ 600kHz	62dB @ 25MHz
Baseband Filter Power (Max Gain)	20mW	20mW	54mW

© Copyright Sirific Wireless Corporation 2002 CONFIDENTIAL www.sirific.com

Tx Chain Measurements

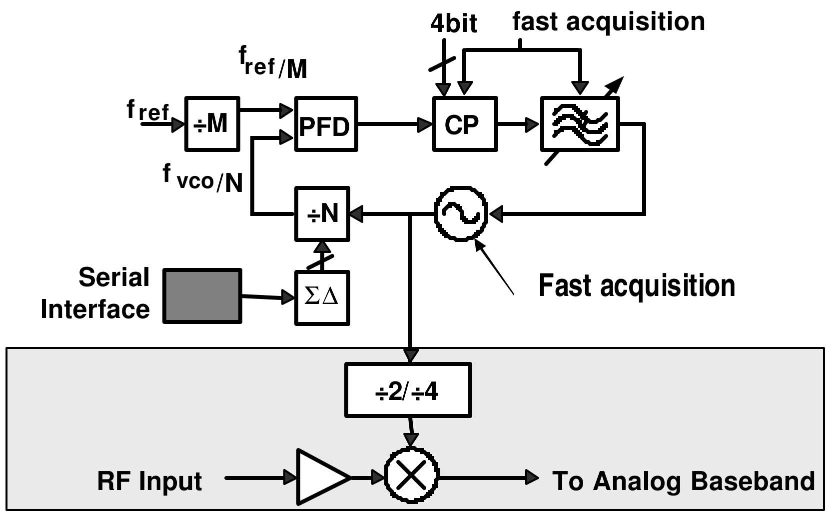
Transmitter	850/900	1800/1900	WLAN
Carrier Suppression	>40dB	>40dB	>40dB
Sideband Suppression	38dB	38dB	>35dB
PN@20MHz@max P	-154dBc/Hz	-149dBc/Hz	-
Gain Range	41dB	41dB	40dB
Max output power	8dBm	8dBm	4dBm
Mixer Power	34mW	34mW	65mW
PPA Power	77mW	77mW	65mW

EDGE Output spectrum from Tx



- EDGE modulation
- Pout = 0dBm
- Passes EDGE mask

RF Synthesizer



 CONFIDENTIAL www.sirific.com

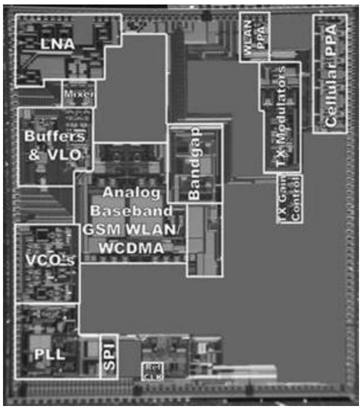
Synthesizer Measured Performance

Synthesizer	GSM	WLAN
VCO Frequency Range	3.4GHz to 3.9GHz	4.5GHz to 5.0GHz
Resolution	200kHz	200kHz or 1MHz
Settling Time (to 100ppm)	185µs	-
Phase Noise (at mixer port)	-90dBc/Hz @ 10kHz -140dBc/Hz @3MHz	-85dBc/Hz @ 100kHz -131dBc/Hz @ 3MHz
CP, Dividers, Loop Filter Power	36mW	36mW
VCO Power	11mW	11mW

 CONFIDENTIAL www.sirific.com

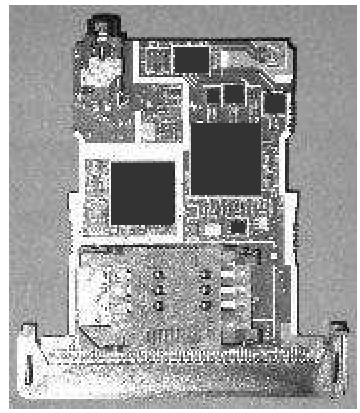
Die Photo & RF Reference Design

- Production chip is < 20mm2



WCDMA and 802.11a Reserved Area

- RF Reference Design



 CONFIDENTIAL www.sirific.com

I. Market Requirements

II. Receiver Architectures

III. Sirific's Virtual LO™

IV. Transmitter Architectures

V. Sirific's Transceiver Platform and Implementation

VI. Conclusion

 CONFIDENTIAL www.sirific.com

Summary

- **Multi – band, Multi-standard applications are a market requirement**
  - Network operators and handset OEM/ODMs require low -cost high performance multi-mode solutions
- **The consumer demand for wireless data services is driving the EDGE, WCDMA and WLAN markets**
- **CMOS solutions provide high integration and low cost**
  - Applying CMOS to narrow -band cellular standards presents many design challenges
- **Direct Conversion is the receiver architecture of choice for multi-standard applications**
  - Eliminating DC Offset is critical
- **Direct Modulation is the transmitter architecture of choice for multi-standard applications**
  - Reducing Carrier Feedthrough and improving Quadrature Accuracy
- **Sirific's Virtual LO™ and Dynamic Spurious Control are methods used to design a multi – band, multi – band direct conversion CMOS transceiver**