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Performance Comparison of State-of-the-Art Volatile and Non-Volatile Memory Devices

Abstract

Between vendor vested interests, presentation hype and datasheet specsmanship, it is often difficult to determine which memory devices are truly the most appropriate for an application in question. This is true for both volatile (DRAM, SRAM and pseudo-SRAM) and non-volatile (NOR and NAND FLASH) memory devices. This 3 hour tutorial will objectively examine the memories available today and in the reasonably near future, including SRAMs such as QDR II, DDR II and QDR III; DRAMs such as DDR2, GDDR3, FCRAM, RLDRAM and XDR, low-power volatile memory devices such as LPDRAM and PSRAM, and low-power non-volatile memory devices such as NOR and NAND FLASH. A brief description will be made concerning external operation of the major devices and where necessary some description of internal operation. The devices will be compared by performance (usable bandwidth under various operating scenarios, energy usage under these scenarios and signal count). Example operating scenarios include random operations, streaming requests with defined read/write ratios and resource predictability, streaming requests with defined read/write ratios but no predictable resource availability, etc. Performance comparisons are made using a cycle-accurate memory comparison software tool written by the author and empirically verified. Cost factors will be considered, including silicon area and test cost of competing architectures. A brief attempt will be made to assess market size and dynamics of the major devices where possible. Conclusions will be drawn for each major operating scenario concerning performance/cost ratios. Wherever possible, practical application examples will be illustrated to make the operating scenarios relevant to the system design tasks faced today and in the reasonably near future.

Biography

As Senior Director of Architecture Development in Micron's NetCom group, Thomas Pawlowski is responsible for Micron memory product definition for networking and communications applications. During his tenure at Micron, Tom has created or co-created the following devices: Reduced Latency DRAM-II, Pipelined Burst Synchronous SRAM, Zero Bus Turnaround SRAM, Double Data Rate SRAM and Quad Data Rate SRAM. Tom holds over 80 U.S. and international patents, with more pending.

Prior to joining Micron in 1992, Tom's spent eight years at Allied Signal Aerospace. He holds a bachelor of applied science degree in electrical engineering from the University of Waterloo, Ontario, Canada.