Janus – A Gigaflop RISC + VLIW SoC Tile

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Agenda (1/2)

- **mAgic™ DSP VLIW Core**
  - Complex Domain, 40-bit Floating Point VLIW DSP Core, 15 ops/cycle
  - Automatic VLIW Scheduling
  - Dynamic Program Decompression
  - Low clock, high ILP core: 1.0 Gigaflops @ 100 MHz, 180 nm CMOS
  - SoC interface
- **Janus ™ = ARM7 + mAgic VLIW DSP Core**
  - Audio Beam-forming, Physical Modeling
  - Architecture, Floor-plan, Technological results (180 nm CMOS)

Agenda (2/2)

- **Dimensional Analysis for Deep Sub-Micron (DSM) VLIW tile design methodology for high performance at moderate clock speed**
  - **ILP*frequency vs. Wire Delay balance on present and future designs**
  - **Memory area vs. Operator Area on present and future designs**
  - **Validation of the dimensional analysis using mAgic detailed Gate Counts and Technological Implementation feedbacks.**
  - **Tiles for Short Wires:**
    - **RISC+VLIW Tile for SoC on future DSM designs**
    - **Hypothesis for a 90 nm multiple tile design**

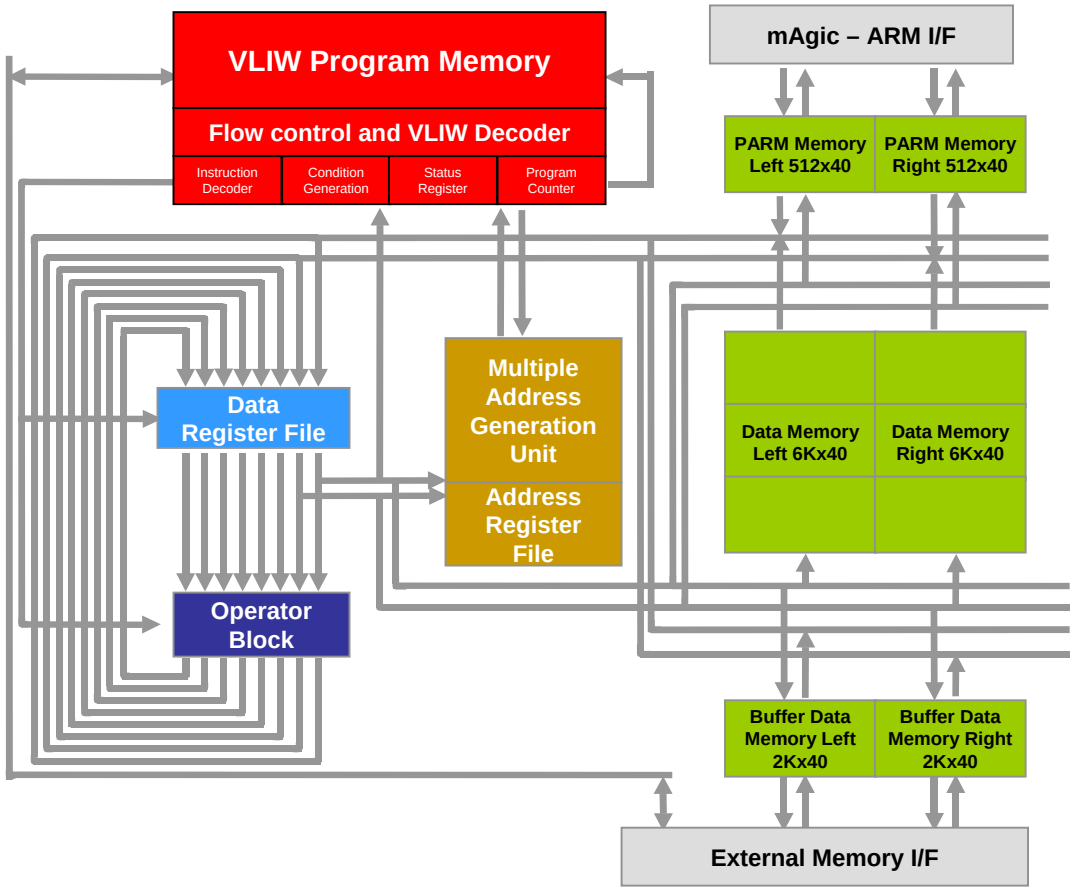
mAgic™ DSP Core

- 1.0 Gigaflops @ 100 MHz, 15 ops/cycle
- Complex Domain, 40-bit Floating Point VLIW DSP Core
- Seamless VLIW: from linear assembler to VLIW scheduling
- DyProDe: Dynamic Program Decompression: 4 PM bit/op
- Low clock, high ILP core: easier SoC Design Closure, less internal pipelines (no need for custom operators), higher efficiency on applications
- Memory mapped slave on the controller's system bus
- Expected dissipation: less than 500mW (typical)

2.4X the performance or 41% the clock at 40 bit vs. classical 32-bit stand-alone floating point DSP

mAgic™ VLIW DSP core Architecture

- On chip 8 k*128 VLIW Program Memory (equivalent to 24k using our patented DyProDe Code compression scheme)
- 2*256 entry multi-port Register File
- On core 8 k*80 Data Memory
- 10 arithmetic operation per cycle, native complex arithmetic, single cycle butterfly
- Multiple Address Generation Unit

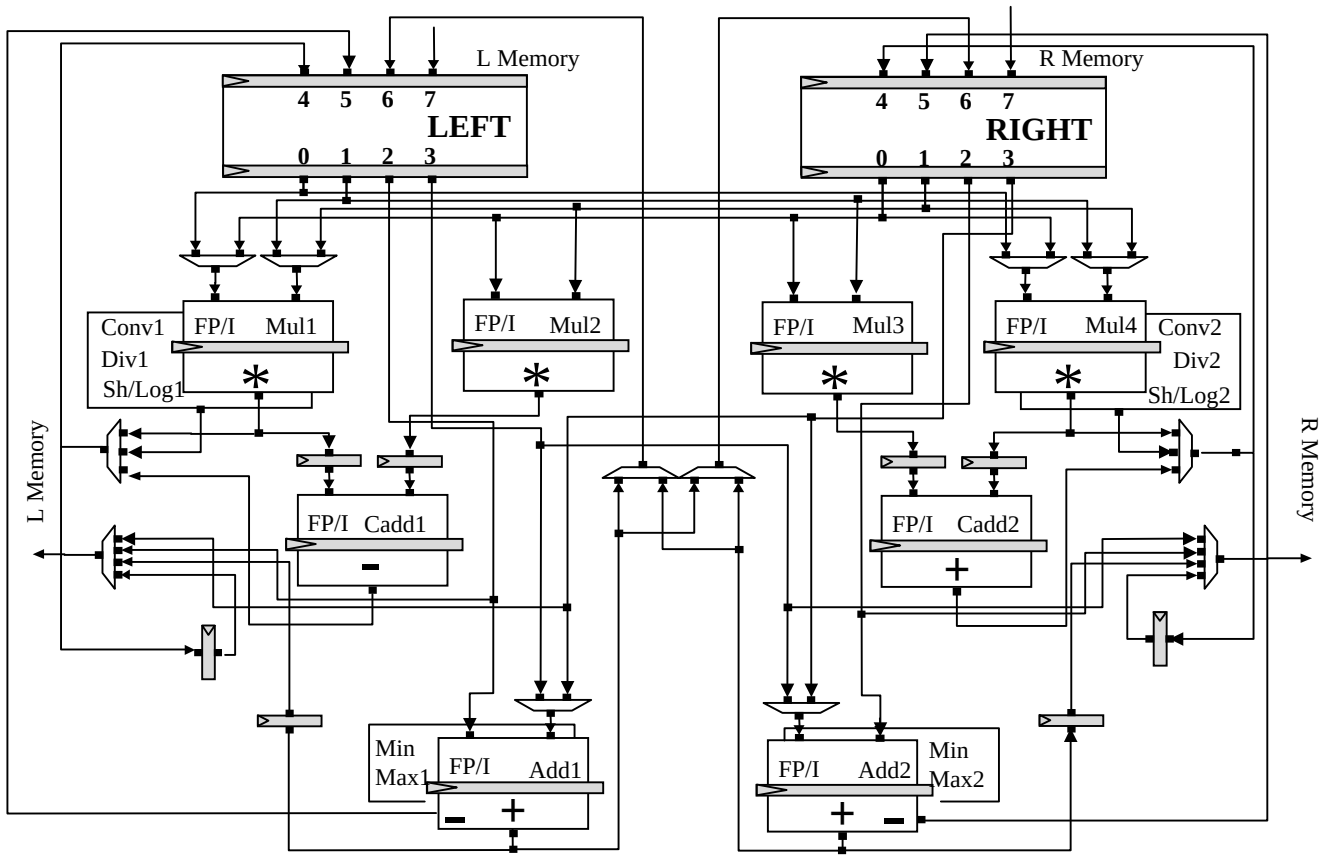


Native Complex Domain Arithmetic

- Significant DSP applications regard wave-processing in audio, radio or ultrasound domains➔complex domain
- The area required for each floating point arithmetic operator is <1/2 mm2 on 180 nm and ~0.1 mm2 on 90 nm CMOS.
- mAgic VLIW DSP benchmarks (Native Complex Domain Support, added operators, added memory bandwidth):
  - 1024 points FFT:
    - 5962 cycles on mAgic VLIW DSP vs 14400 on C67
  - 64 output from a 64 taps complex FIR filter:
    - 4663 cycles on mAgic VLIW DSP vs. 8225 on C67
  - Single cycle butterfly (40 bit floating point)
  - Single cycle complex mulacc (40 bit floating point)

mAgic™ Operator block

- Operator Block: 10 Float/Int Op per Cycle
- Complex Arithmetic support
- Vector 2 Arithmetic
- Butterfly Arithmetic
- Large (512) Multiport (8+8) Register File



Automatic VLIW Scheduling

The designer writes in a serial fashion, and the assembler schedules optimized code that takes advantage of the DSPs Instruction Level Parallelism, accounting for data dependencies and latencies

A SEQUENTIAL CODE LIKE:

A=B+C

D=E*F

G=A+D

L=M+N

Q=Memory[I]

P=Q*R

IS SCHEDULED AS:

A=B+C; D=E*F;Q=Memory[I]

L=M+N;

G=A+D; P=Q*R

Multiple Address Generation Unit

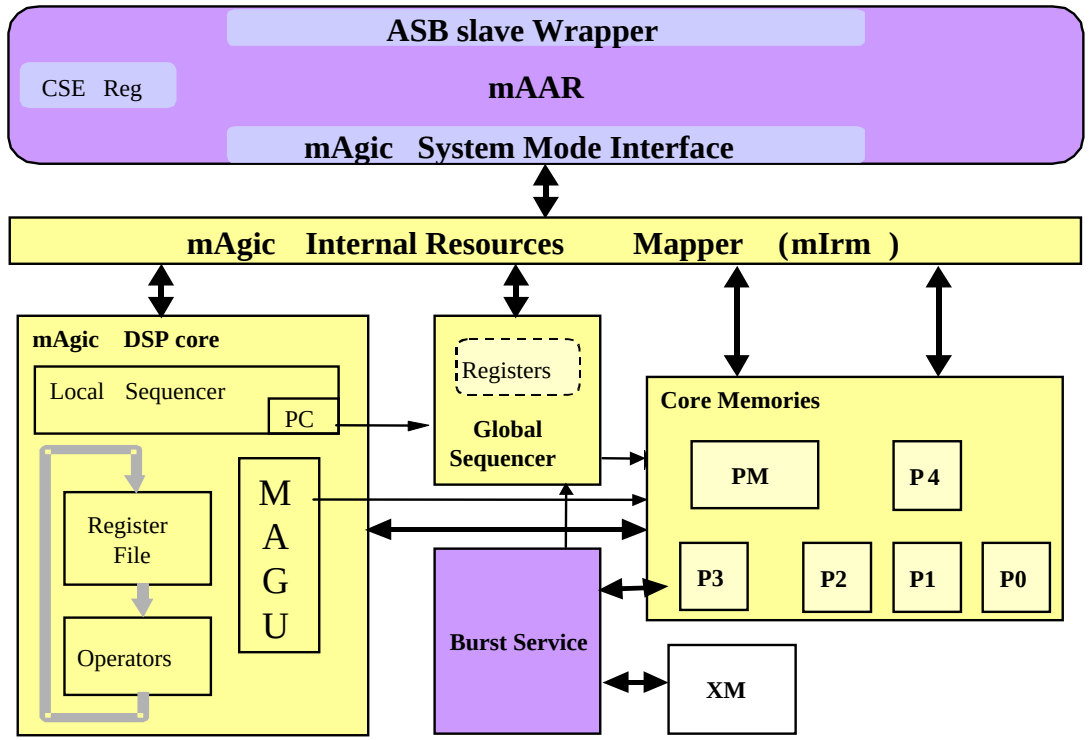
SLAMP fields and MAGU Addressing Modes

- **S: 11 bits Start reg, vector absolute base address or circular buffer starting address**
- **L: 11 bits Length reg, vector length**
- **A: 11 bits Address reg, offset or abs base address**
- **M: 7 bits Increment reg, increment**
- **P: 9 bits Page reg, for internal memories pages addressing**

	Description	Address out	Modified A	Assembly suffix
Linear: S=L=0	Just Use	S+A	A	-
	Modify & Use	S+A+M	A	M
	Use Modify & Update	S+A	A+M	U
	Modify Use & Update	S+A+M	A+M	MU
Offset: L=0	Just Use	S+A	A	-
	Modify & Use	S+A+M	A	M
	Use Modify & Update	S+A	A+M	U
	Modify Use & Update	S+A+M	A+M	MU
Modular:	Just Use	S+A	A	-
	Modify & Use	S+ (A+M)mod.L	A	M
	Use Modify & Update	S+A	(A+M)mod.L	U
	Modify Use & Update	S+ (A+M)mod.L	(A+M)mod.L	MU

mAgic™ DSP Core interface with SoC Bus and External Memories

- Slave memory mapped device on the controller's system bus
- 1.6 Mbit internal Program and Data Core Memories are memory mapped as well
- XM DMA and SoC System Bus activities run in parallel with the core on dedicated Double Port Buffers



Examples of target Gigaflops Applications

- Hands free home phone
  - Audio Beam-Forming
- Better audio hearing aids and ear prosthesis / Real time modeling of cochlea
  - Real-time Differential Equation Solution
- Missile Guidance / Seeker
  - Radar Beam-forming / Anti-jamming
- SW Ultrasound Scanner / Better Diagnostic Image Quality
  - Ultrasound Beam-forming
- ➔JANUS: An ARM7TDMI + mAgic VLIW DSP SoC for those applications.

Janus: a DUAL CORE VLIW DSP + RISC

mAgic VLIW FiPU DSP:
1.5 GOPS @ 100 MHz
(1.0 GFLOPS)

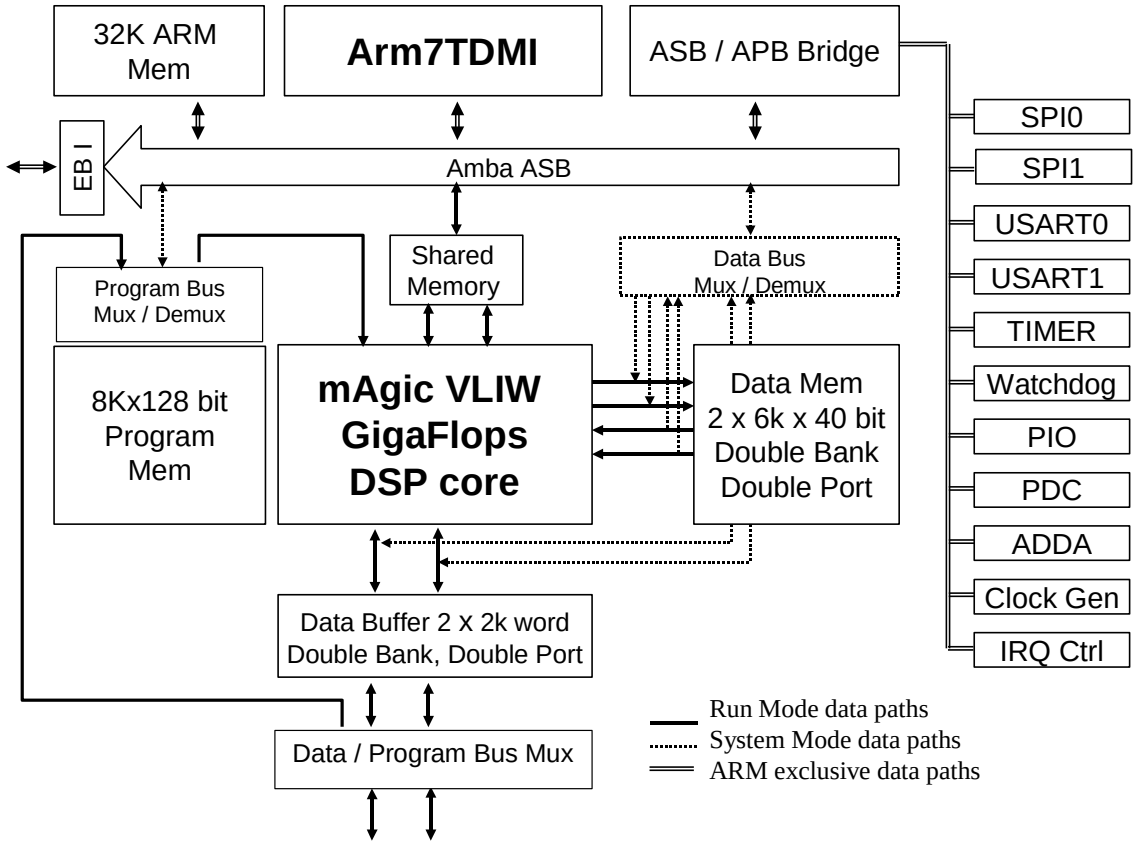
32 bit ARM7TDMI RISC

Set of SoC peripherals

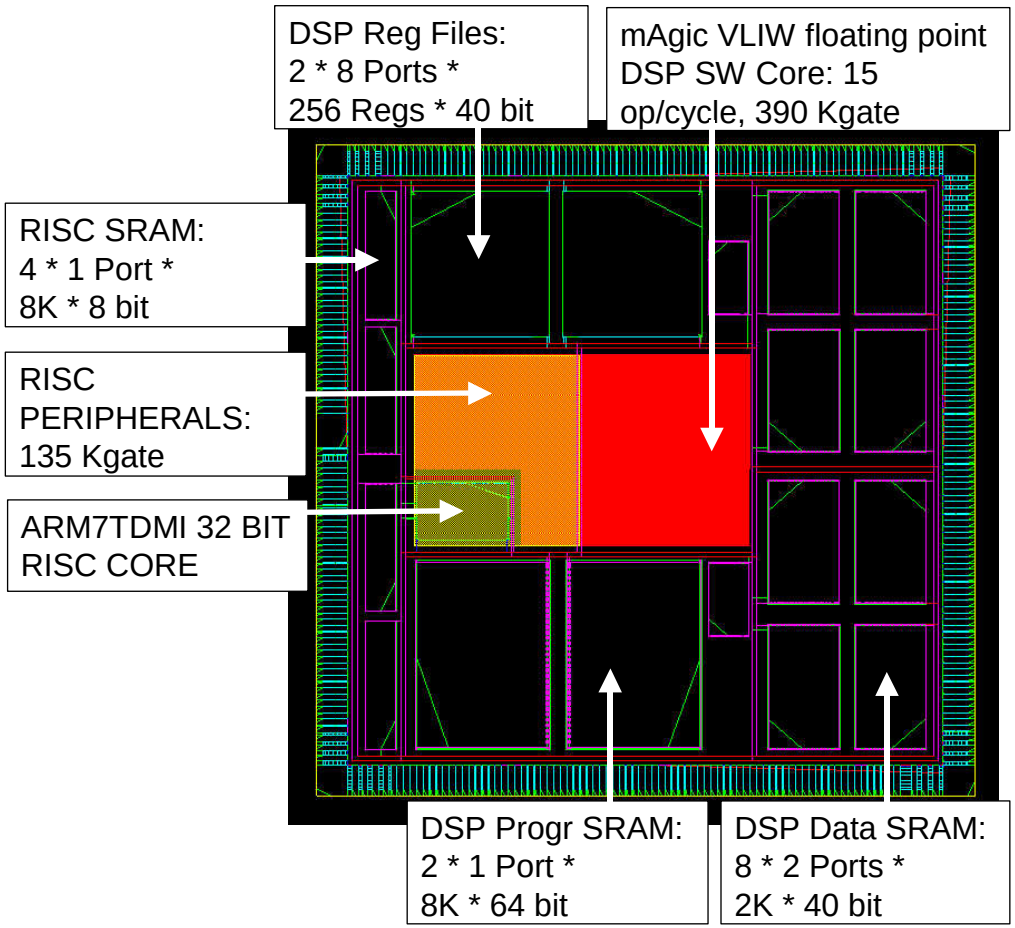
1.9 Mbit SRAM on Board

352 BGA, 243 functional I/O

1.2 W worst case @ 100 MHz



Janus Floorplan & Technological Measurements



Atmel 180 nm, five-level, Aluminum CMOS

Pad excluded, 39 mm2

Pad included, 55 mm2

243 functional IO

352 Ball Grid Array package

1.8 V (Core), 3.3 V (I/O)

<1.2 W (worst case) @ 100MHz

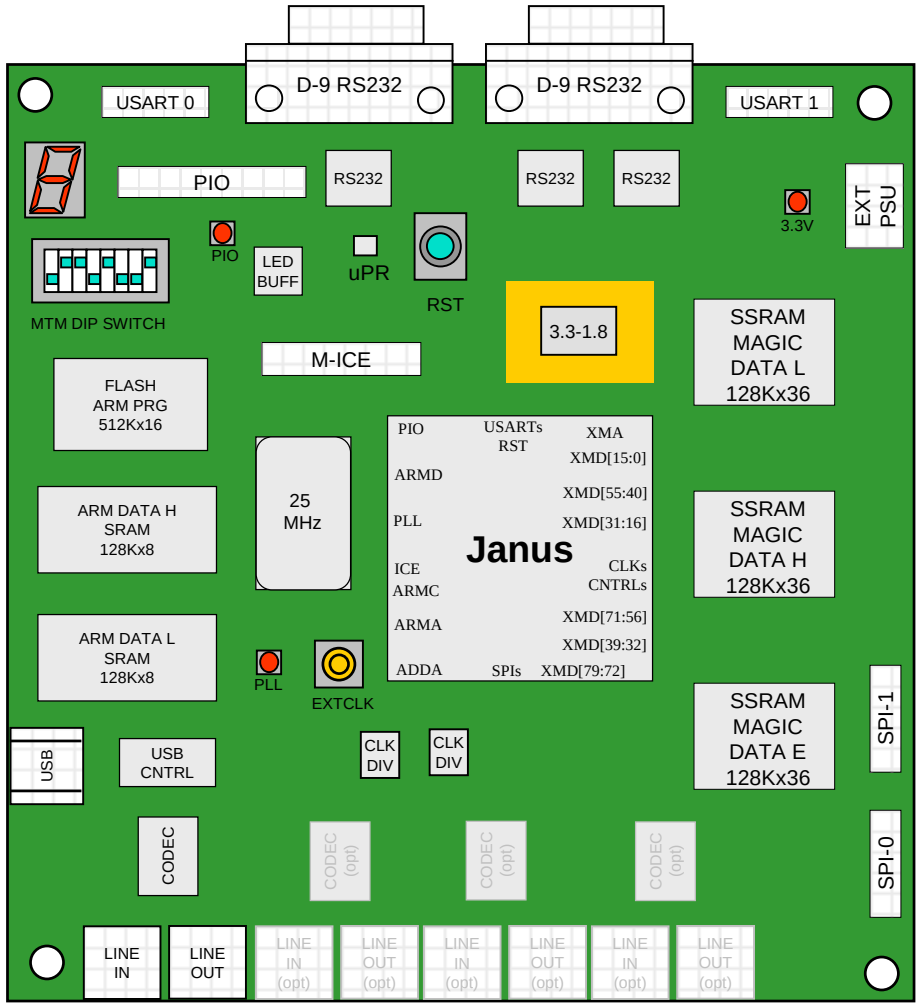
1.5 Gops, 1.0 Gigaflops

55 Kgate/mm2 effective density (10 mm2 for 550Kgate logic required for the software macros: VLIW DSP + Arm peripherals + testability stuff)

HW Tools: JANUS Test & Evaluation Board

MTM Works @ 100MHz and Provides the following resources:

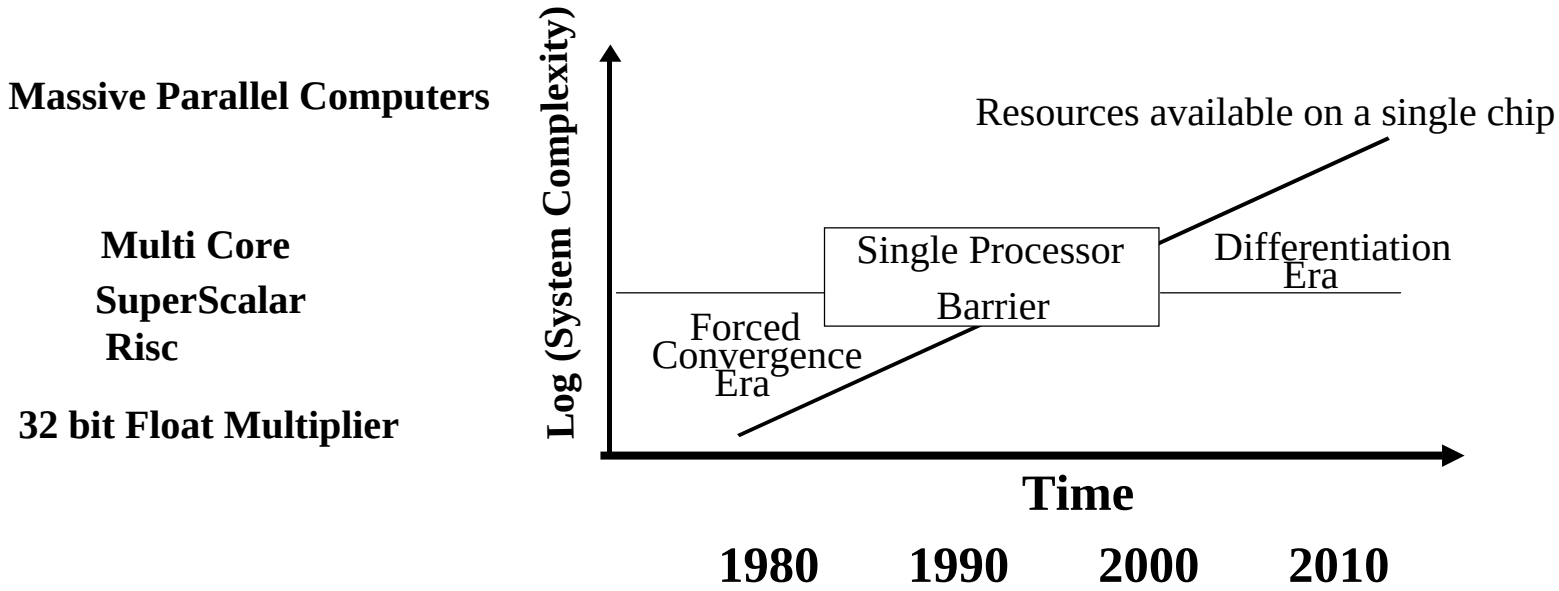
- Memories for mAgic and ARM
- Stereo Audio CODECs (up to 4)
- Serial I/O:
  - 1 USB 2.0 Full Speed (12 Mbps)
  - 2 RS232/LVTTL a/sync serial lines
  - 2 SPI serial I/O lines
  - 1 ÷ 4 audio codecs
- IO connectors (USART, SPI, PIO, AUDIO)
- Configuration DIP SWITCH
- Status 7-segment Display
- JTAG ARM M-ICE connector
- Size: 5 x 5 inch^2 (12.7x12.7 cm^2)



Development Effort

- **Our SIMD/VLIW mAgic DSP architecture is largely based on the know-how acquired by some of the authors thanks to their participation to three generations of the Massively Parallel Processing experiment APE, conducted since 1983 by INFN (Istituto Nazionale di Fisica Nucleare). The design and development of custom VLIW processors, hardware and system software for those machines accounted for more than 300 Person Years.**
- **From that background, the development and validation of mAgic VLIW DSP and the essential system software required approximately 65 Person Years.**
- **The integration and validation at Janus level with the ARM core and the set of pre-validated ARM peripherals, plus physical design and validation board activities should required approximately 10 Person Years.**

A Differentiation Era beyond the Single Processor Barrier



Power density, overhead logic and interconnect delays for monolithic high clock speed processor design are approaching embarrassing figures according to ITRS. The human brain has got a processing power >> 10^6 times than DSP processors of 2003, yet runs at <<100 Hz, ~10W. A precious Hint for adoption of moderate clock speed, better memory architectures and parallelism management to exploit higher silicon densities provided by DSM technologies?

Dimensional Analysis for Deep Sub-Micron Processor design with ASIC methodology

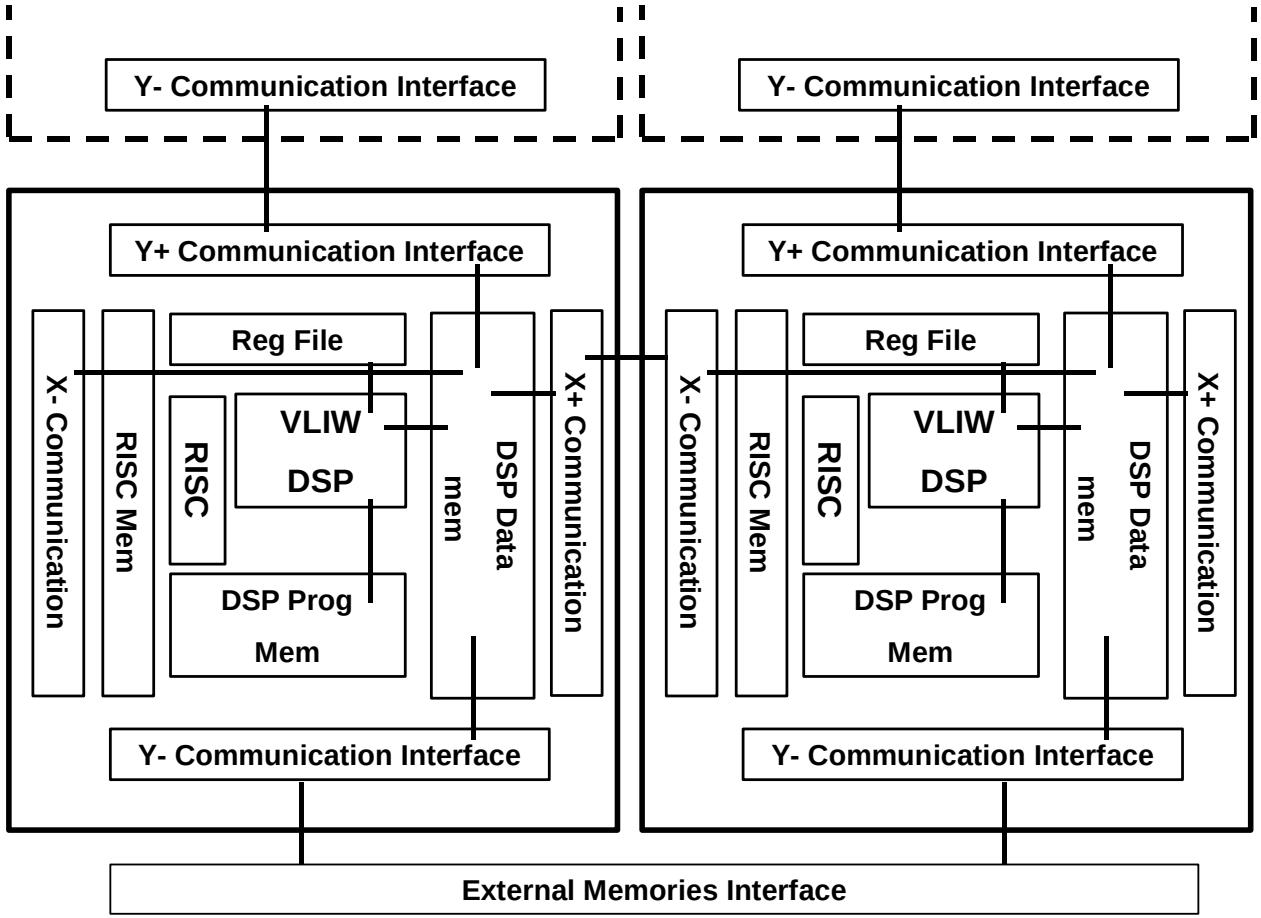
- **A possible concern regarding synthesizable cores for next decade SoCs:**

  maximum frequency dominated by wire delays, not by gate propagation

  ➔ our simple dimensional analysis suggests that:

  - **adequate ILP + multiple tiles, ➔ lower clock speed, lower pipelining, shorter wire lengths ➔ simpler design closure**
  - **floating point relatively un-expensive ➔ Balancing Memory area vs. Operating area**
  - **DSP treatment of wave phenomena ➔ useful ILP >= 15 ➔ native complex domain support**

Multiple Tile SoC: Tiles for Short Wires



ILP * frequency vs. Wire Delay

- r and c := technological resistance and capacitance per wire unit length (e.g. 180 nm →rc = 58 ps/mm2, 90 nm→rc = 160ps/mm2)
- L := processor's tile size; 2L:=worst Manhattan path length
- g:= gate density (e.g. 180 nm➔g=55Kgate/mm2; 90 nm➔g=200Kgate/mm2)
- o:= arithmetic operator cost (e.g. 7Kgate 24 bit floating point, 25Kgate 40 bit)

$$f_0 \le f_W = \frac{1}{.38RC} \le \frac{1}{.38rc(2L)^2} \quad (1)$$

logic delay→f_0, wire delay→ f_w. $f_0 << f_w$ indicates designs far away from interconnect troubles

$$2L = L_T = \sqrt{2\frac{t_{p1}}{.38rc}} \quad (2)$$

L_T repeater insertion critical length ~ 4.4mm ~ 419 ps on 180 nm

$$ILP \le \frac{g}{o}L^2 \quad (3)$$

L^2 areas support VLIW ILP determined by gate density over operator cost

$$G_W = f_W * ILP \le .66\frac{g}{rco} \quad (4)$$

peak power for a VLIW area below critical area (NOTE the interesting independency on size and ILP)

Dimentional Hints

Equation (4) Gw =fw * ILP <= .66 g/rco, provides suggestions:

- **At one extreme, it states the obvious. You should divide a die too large into N smaller tiles.**
- **At intermediate scale, it suggests to insert at least the number of operators that can be reached by non repeated wires. In fact a lower frequency reduces the number of local pipelines, permits the adoption of a classical ASIC RTL methodology and simplifies the adoption of lower V_{dd}.**
- **A lower bound for the ILP is imposed by:**
  - **adequate program and data memory inside each tile**
  - **maintain a higher granularity to avoid classical massive parallel processing inefficiencies**
  - **balance memory vs processing resources**

mAgic VLIW Arith Oper Gate Count

#Units		Combinatorial	Non Comb.	Total	Grand Total
4	40 bit Float Adder	10900	8400	19300	77200
4	40 bit Float and 32 bit Int Mult	24100	2700	26800	107200
4	32 bit Int Adder	900	1600	2500	10000
2	Float Div & Sqrt Seed	3300	700	4000	8000
2	40 bit Shift & Logic Unit	6600	800	7400	14800
2	Float<->Int Converter	4500	400	4900	9800
1	Decoder	1200	1700	2900	2900
	Total VLIW Arithmetic Operators				*251300*

➔ SUPPORT FOR NATIVE COMPLEX DOMAIN 40-bit FLOATING POINT ARITHMETIC <= 1.5 mm2 on 90 nm CMOS

mAgic VLIW Floating Point DSP Gate Count

	Combinatorial	Non Comb.	Total
VLIW Arithmetic & Logic Operators	186800	64500	251300
VLIW Multiple Address Generation Unit	18900	13100	32000
VLIW Flow Controller	8300	18000	26300
VLIW DMA + Global Status Controller	4600	11300	15900
VLIW Program Decompression Engine	7600	10500	18100
VLIW Local Memory Mux Logic & Bist	18700	13800	32500
VLIW<->RISC Memory Mapping Interface	1300	6800	8100
VLIW DSP ENGINE TOTAL GATE COUNT	*250400*	*141400*	*391800*

➔payload for mAgic VLIW core >= 70% grows to 90% considering processor + memory tiles

➔ equations (3) and (4) are reasonable approximations

Dimensional Analysis results

- On 180 nm Atmel technology, the gate delay for a 25 Kgate 40-bit floating point operator with two pipeline stages is 8 ns. Therefore $f_0 << f_w$ for the full VLIW core with ILP = 15. Complete RISC+VLIW logic area ~ 10 mm2, 550 Kgates
- On 90 nm copper CMOS, f_0 / f_w ~ 1 / 6for the 250 Kgate complex domain data path with 10 floating point operators. A pipeline stage will be required on core<->memory busses.
- 8 Gigaflops, 4 Janus tiles SOC feasible with ASIC methodology on 90 nm technology with classical RTL synchronous design. Insertion of repeaters and promotion of global wires on thicker layers helps, but is not yet mandatory.

Summary

- mAgic VLIW DSP: a synthesizable complex domain floating point core: 1.0 Gigaflops @ 100 MHz, 180 nm CMOS
- Janus: a 180 nm RISC+floating point VLIW platform for Gigaflops SoC applications
- A Dimensional Analysis based on the technological parameter g/rco provides an interconnect bound to the processing power of simple synthesizable RTL designs on DSM techologies with ASIC methodology
- We will follow a simple roadmap for SoC integration of multiple gigaflops on 90 nm using:
  - Tiles for Short Wires
  - Appropriate VLIW parallelism
  - Moderate Clock Speed
  - This methodology keeps the cost down to a few tens of designers and M$.