

The Architecture of the Intel[®] PXA800F Cellular Processor

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Agenda

- Architecture/Design Challenges
- GSM/GPRS overview
- Chip overview
- Architectural Features
- Reference Designs
- Performance Results
- Summary

Arch/Design Challenges

- Develop a high-performance low power embedded SoC arch with integrated memories for a GSM/GPRS phone
- Take advantage of small protocol code size requirements
- Integrate Flash memory (reprogrammable) into the chip
 - Lower latencies/higher perf with integrated memory
 - Consider options to keep memory closer to processors
 - Choose memory size sufficient for comm and apps
- Develop a new 0.13 Flash+Logic process
- Address leakage concerns with the 0.13u process to obtain good standby time for such a phone
- Have good performance for comm and apps sub-systems
- Optimize vectors such as performance, power, area, latencies, cost, energy/battery life, system efficiency

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The GSM/GPRS Standard

- Most widely-used standard in the cellular industry
- 850MHz, 900MHz, 1800MHz, 1900MHz bands
- TDMA with 8-slotted users in 200kHz channels
 - Time slot is of 577us duration
- GSM standard for Voice
 - Different frequency channels Rx and Tx
 - One time slot each for Rx and Tx
- GPRS standard for Data
 - Class 12 phone (4Rx + 1 Tx, 3Rx + 2Tx, 2Rx + 3Tx, 1Rx + 4Tx)
- Link adaptation used to switch between modulation and coding schemes depending on channel conditions

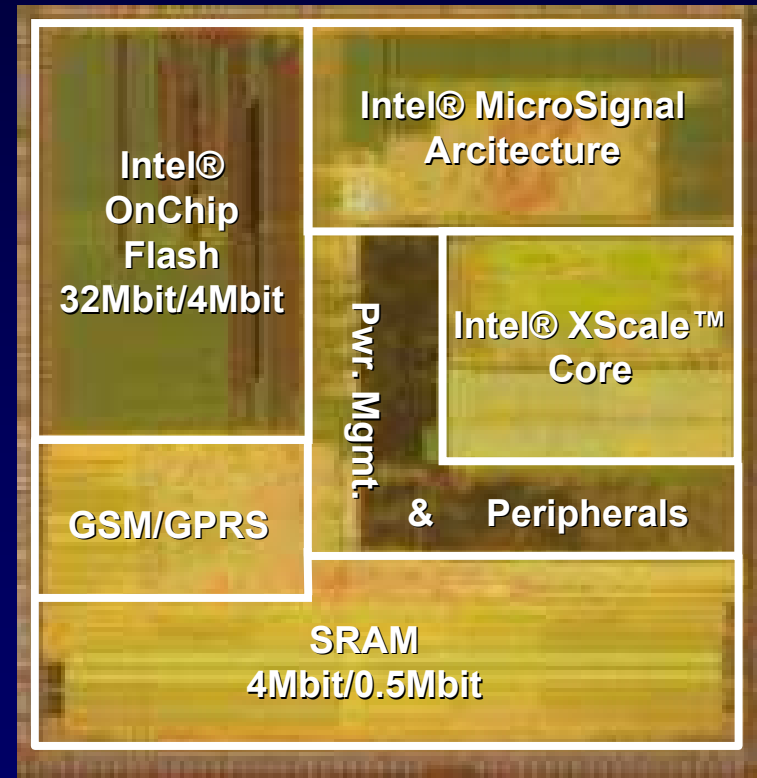
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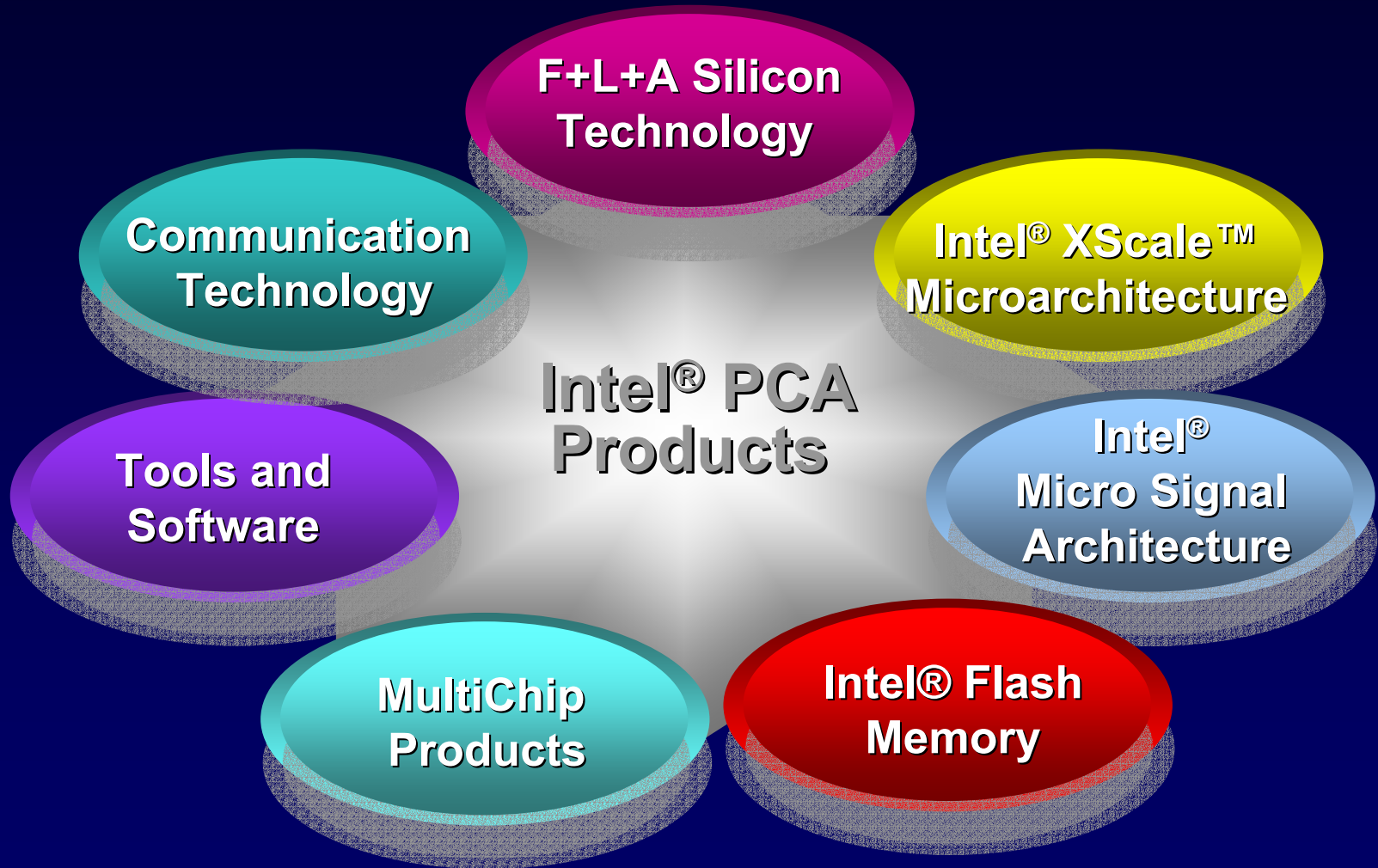
Intel® PXA800F Cellular Processor

Industry's 1st single-chip Flash+Logic GSM/GPRS solution for Enhanced Applications Capabilities in Mainstream Phones

- Intel® 0.13 μ Flash + Logic Process Technology
- Intel® XScale™ Microarchitecture
- Intel® Micro Signal Architecture
- GSM/GPRS baseband comm logic
- Integrated Flash and SRAM Memories -> 33% of chip area
- Integrated Power Management and Peripherals
- Approx 10⁸ transistors
- 12mm x 12mm TFBGA package



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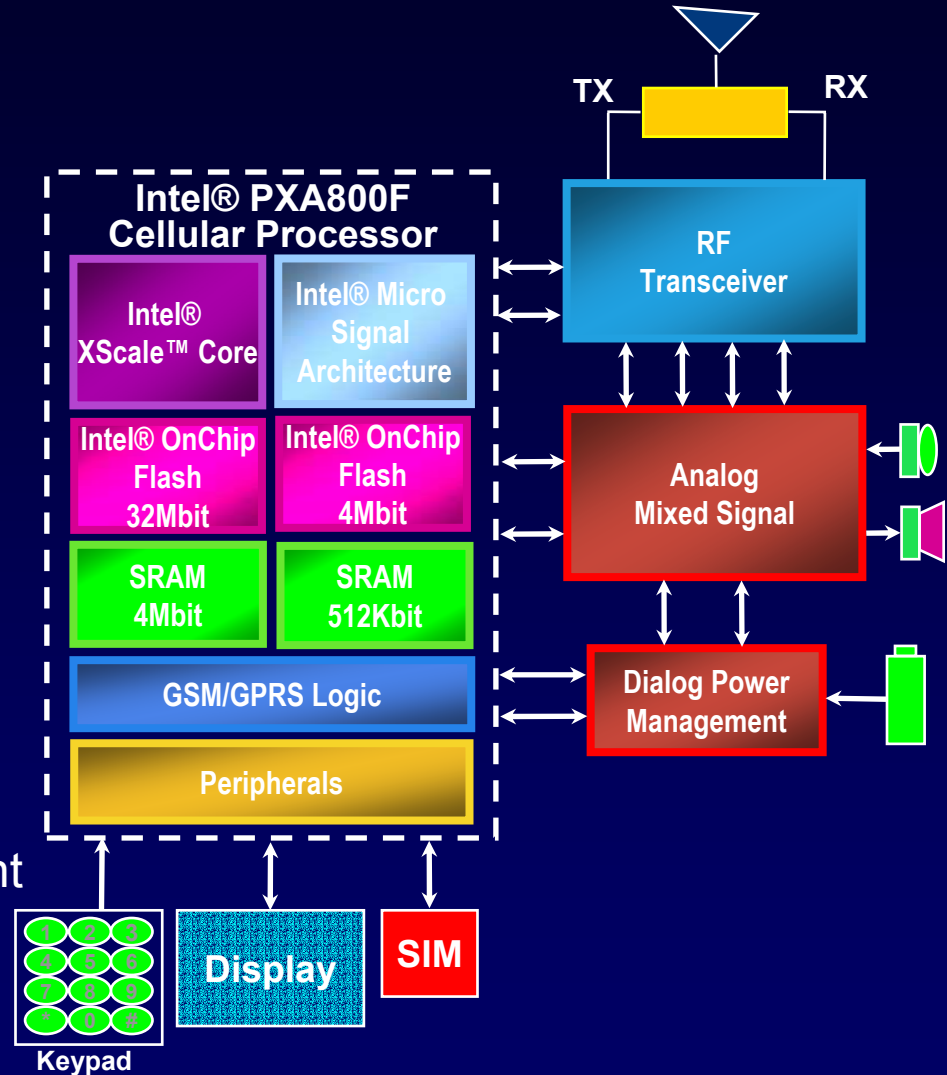
Intel® PXA800F Cellular Processor: 2.5G GSM/ GPRS Class 12

Complete Integrated baseband solution

- Intel® XScale™ Microarchitecture
 - ARM* V5TE compliant
- Intel® Micro Signal Architecture
 - Modified Harvard Architecture
- 36 Mb integrated Intel® OnChip Flash memory
- 4.5 Mb integrated SRAM memory

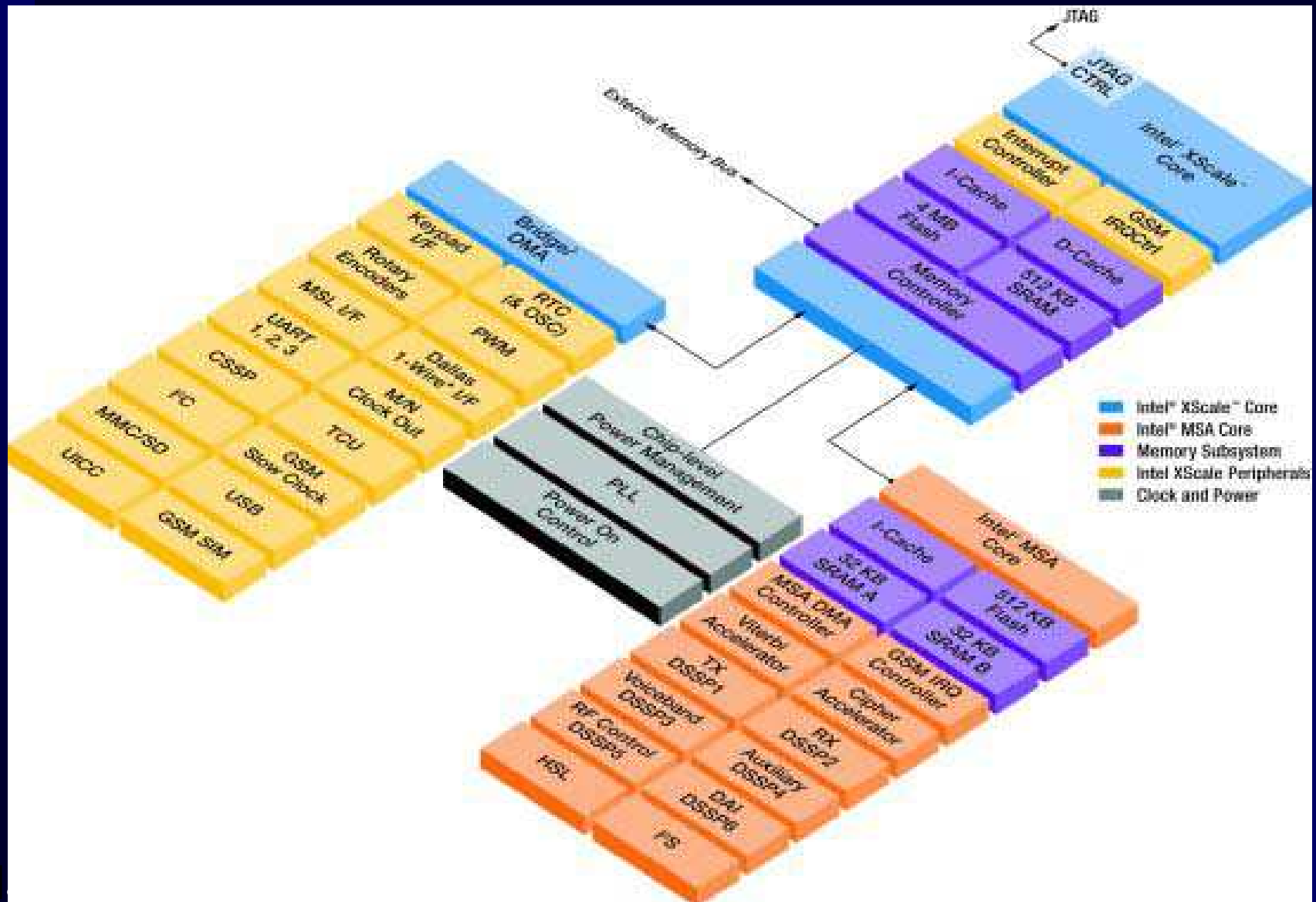
Total solution

- Full GSM/GPRS Class 12
- L1-L3 Comm protocol software
- RTOS Java-based platform
- API for customer apps development
- Designed for use with industry-proven mixed signal/RF solutions
- Optimized PowerMgmt IC (Dialog)
- Handset reference design (Elektrobit)



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Key Modules in the Chip



Intel® PXA800F Cellular Processor: Features

- **GSM/GPRS Communication Processor**
 - Integrated high-performance Intel® XScale™ processor
 - 32Mb Flash and 4Mb SRAM
 - Intel® 0.13μ integrated process technology
 - Re-programmable Micro Signal Architecture – digital signal processing with microcontroller features
 - 4Mb Flash and 64kB of SRAM
- **Intel® Personal Internet Client Architecture**
 - Supports Intel XScale™ application processors
 - Supports, MP3, Bluetooth*, and WAP
- **High-Speed Internet Access**
 - Class 1-12 GPRS
 - Voice + data & SMS, EMS, MMS
- **Broad Range of On-Chip Peripherals**
 - 52MHz, 16bit SDRAM I/F
 - Support for up to 32MB of SDRAM
 - Support for LCD controller chips
 - UART (3), CSSP (1), DSSP (6), USB, I²C, I²S, MMC/SD, GPIOs, U-SIM, PWM(4), 1-wire I/F, keypad, pwr mgmt cntrl, JTAG debug I/F
- **Bluetooth Interface (UART & SSP)**
 - Supports v1.0b compliant MAC & RF
- **Application & Data Storage Expansion**
 - x16 burst memory expansion interface
 - Supports Intel® Flash Data Integrator
- **Complete GSM Phase 2+ L1-L3 Protocol Stack**
 - Intel developed L1
 - Industry proven L2-L3
- **Dedicated IF & RF**
 - Proven mixed signal analog
 - Interfaces to DDC/ZIF RF solutions
- **Advanced Package Technology**
 - 12mm x 12mm TF-BGA (.65mm pitch)
- **Full Development Kit**
 - Includes RF, mixed signal, USIM, Pwr Mgmt, Bluetooth, and optimized SW
 - Supports MP3 and application processors based on Intel XScale™ microarchitecture
- **Reference Design**
 - FTA certificate verifying compliance
- **Full Customer Support**
 - Documentation, training, diagnostic tools

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Architectural Features

- Parallelism
- Integrated Code/data (Flash/SRAM) memories
- Reduced System-level latencies
- Higher System-level Performance
- Reduced System-level power
- Lower Energy
- Lower Cost for overall platform
- Reduced Area for the platform
- Reduced RF Edge Rate Noise Effects

Parallelism

- Wide independent buses from each core to integrated memories (Flash and SRAM)
 - Internal memory buses provide direct accesses to memories; are wider and faster than the 16-bit 52MHz external memory interface
 - Traditionally phone designs access memories from shared buses with arbitration penalties across narrow higher latency external memory interfaces which impacts performance
- Separate buses to access peripherals/ext mem
- Concurrency

Intel® XScale core



Integrated Flash/SRAM

Intel® MSA Core



Integrated Flash/SRAM

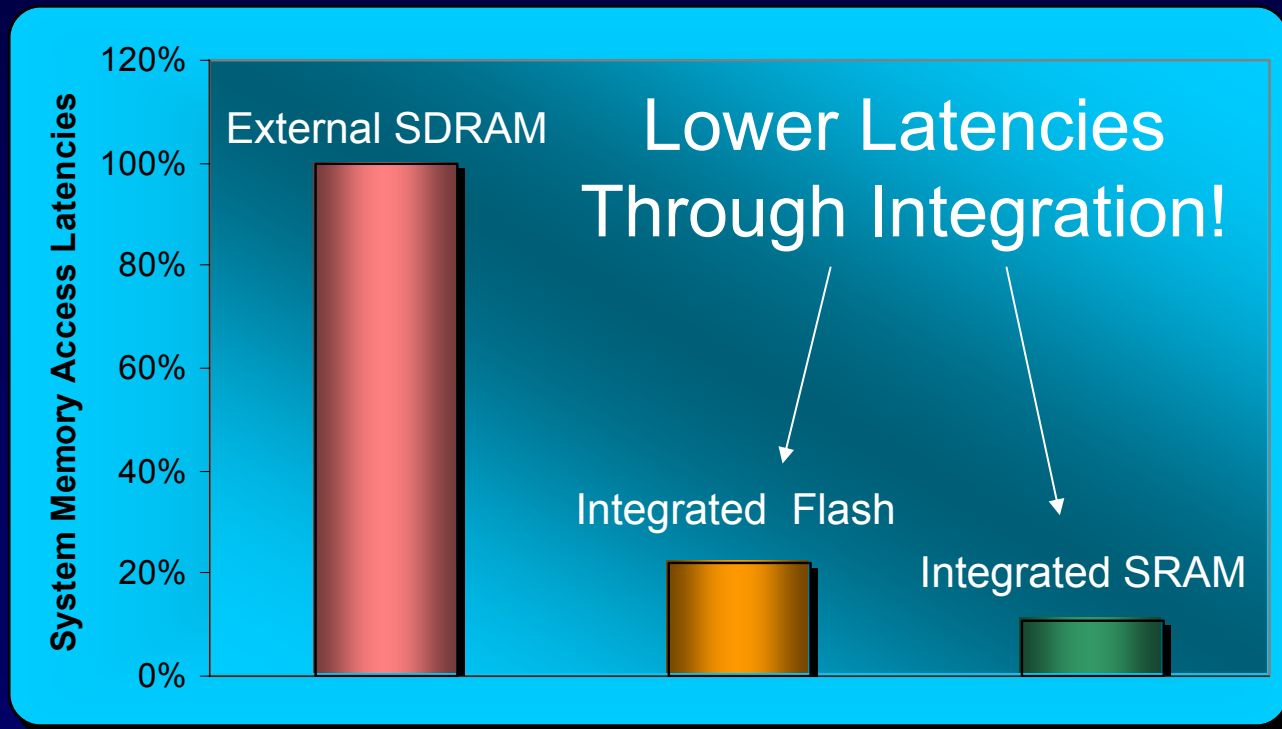
External Memory



Peripherals

Reduced System Level Latencies

- System-level latencies to integrated memories greatly improved due to direct access and optimized design
- Latencies in the application-processor sub-system shown as percentage of external memory access time



Higher System Level Performance

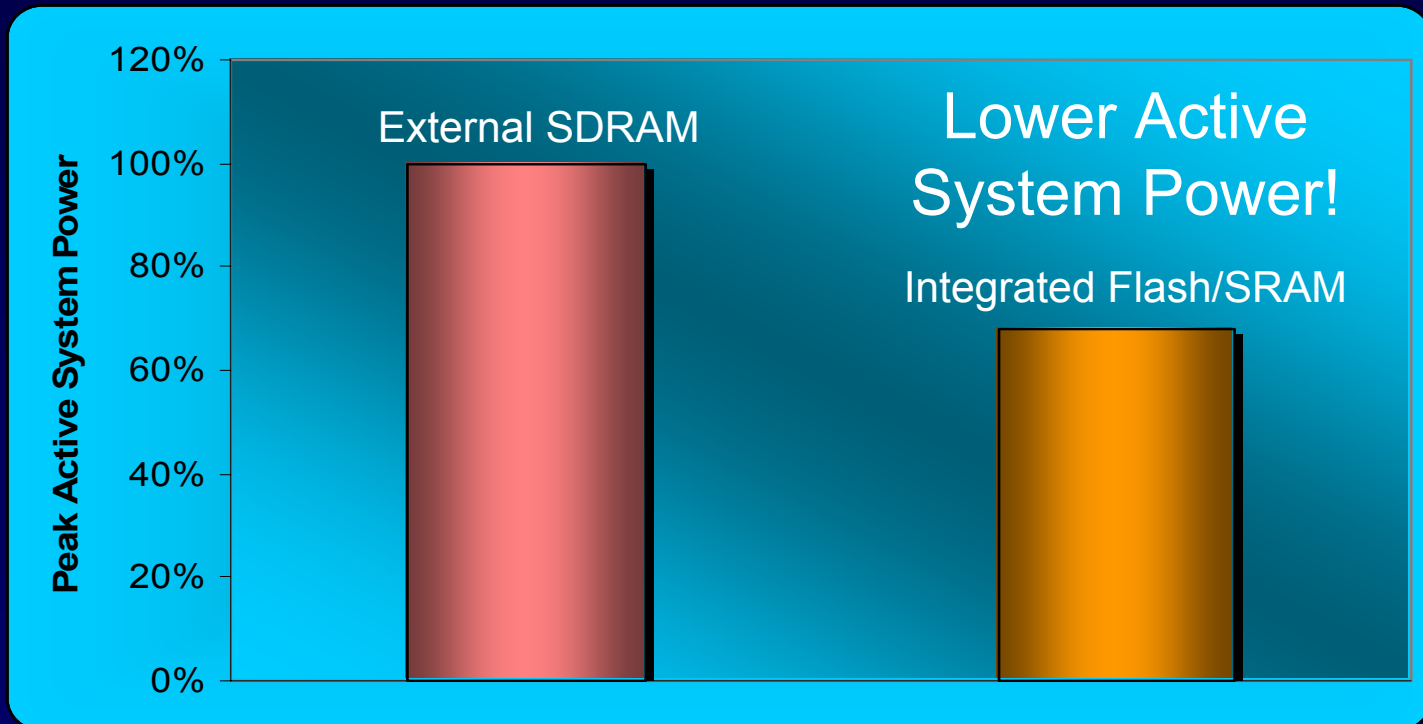
- $CPI_{Avg} = CPI_{Ideal} + R_i L_i + f_d R_d L_d$
- As an illustration, assume 99% ICache hit rate, 98% DCache hit rate, 50% of instructions accessing data, and a 312MHz XScale core.
- Assume external memory access penalty is X 312MHz cycles.
 - Internal Flash access penalty for an I-cache miss is approx 0.2X
 - Internal SRAM access penalty for a Dcache miss is approx 0.1X
- Average CPI when using external memory only
 - $= CPI_{Ideal} + 0.01 * X + 0.5 * 0.02 * X$
 - $= CPI_{Ideal} + 0.02 * X$
- Average CPI when using internal memories only
 - $= CPI_{Ideal} + 0.01 * 0.2X + 0.5 * 0.02 * 0.1X$
 - $= CPI_{Ideal} + 0.002 X + 0.001 X$
 - $= CPI_{Ideal} + 0.003X$
- Lower CPI
 - ➔ Core stalled for less time → Better processor utilization
 - ➔ Better MIPS (=MHz/CPI) availability

Higher System Level Performance

- Additional performance considerations such as
 - Prefetching data (PLD –prefetch load instr)
 - Consider only those data cache misses that caused data dependency stalls in the execution pipeline
- Ensure that all code and data fit in integrated memories
 - Code/data partitioning, with performance critical code/data in integrated memories, to improve performance (if external memory is required)
- Java-based execution environment with an OS used in the apps sub-system, with all code/data requirements for communications satisfied by using integrated memories.
- Improved overall system efficiency
- Excellent response times during task switching and peak loading

Reduced System Active Power

- Total Active System level power is reduced when not using external memory
 - Power shown relative to system power when using external memory



Power Management

- Innovative power minimization strategies
- Active, partial-idle, idle, standby, and off power modes
- Reduced leakage in standby mode
- Internal power management unit to
 - Handle transitions between various power modes
 - Frequency scaling to reduce power
- Power mode to use determined by
 - Transition times/energy costs involved in transitions
 - Expected time in a lower power mode
- Hardware & software for optimal energy usage
 - Hardware state machines to handle transitions
 - Software decision-making to enforce transitions
- Custom power mgmt IC for additional power mgmt

Power Modes

Mode	Cores	Peripherals	PLLs	I/O Ring	VCXO 13MHz Osc	RTC
Active	On	On	On	Active	On	On
Idle	Cores Inactive Clocks Disabled	Inactive (SW disable +Clocks disable)	On	Active	On	On
Standby	Cores Inactive Clocks Inactive Reduced Leakage States Retained	Inactive (except detection logic running with slow clock 32KHz)	Off	Inactive (sensing asynchronous inputs)	Off	On
Power Off	Powered Off (Real time clock active)	Off	Off	Off	Off	On

Lower Energy

- Reduced Power * Reduced Latencies (Time)
→ Reduced Energy
- Lower energy needed for task completion
- System moves to a lower power mode earlier
- Power = VI (Leakage) & CV^2F (activity) components
- Power consumed in full-system idle mode (gated clocks)
→ Approx 3% of the power consumed in active mode
- Power consumed in standby power mode (reduced leakage, inactive clocks, states retained) is
→ Approx 0.1% of the power consumed in active mode.
- Reduction in energy usage → increases battery life
- Expected standby time of around 250-300 hrs

RF Edge Rate Noise Reduction

- I/O digital buffers from the processor->memory interface exhibit a frequency spectrum determined by their edge-rates
- Faster edge-rates have broader frequency spectrum
- Spectrum can have RF components that interfere with the RF Rx channels
- Wireless data-centric phones suffer much worse due to extreme data transfer between a chip and external memories
- No I/O buffers in access path to integrated memories
→ RF Edge Rate Noise Effects Reduced

Overall advantages of on-chip memory integration

- Lower cache miss penalties
- Direct execution from integrated memories
- Higher System-level performance
- Lower power (less power wasted on the pins)
- Wider independent paths from memory to cache
- Outstanding response times during peak loading and task switching
- Greater Peak MIPS availability
- Reduces RF Edge Rate Noise Effects
- Reprogrammable Flash memory for communication and application sub-systems

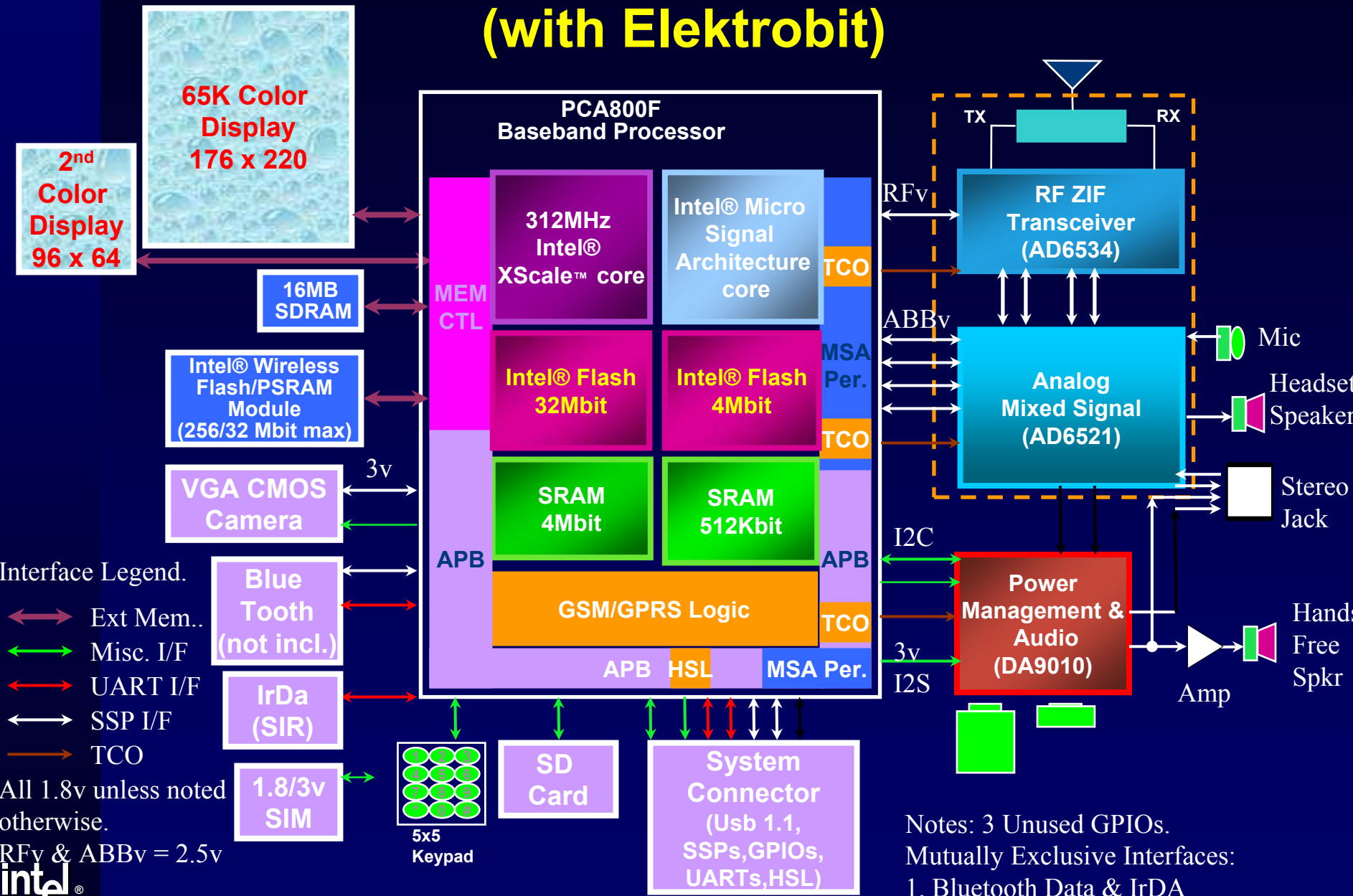
Validation & Software

- Pre-silicon phase
 - Hardware accelerators, module-level validation in a full-chip context, overall system-level validation
 - Multiple clock and power domains to consider
 - On-chip/off-chip clock sources, clock gating, sync/async interfaces
 - Standby/non-standby domain coupling, varying voltage domains
 - FPGA based emulation board
 - Enabled software development
 - Voice call simulation using a base station emulator
- Post-silicon phase
 - Evaluation board containing the chip used
 - Voice and data calls successfully achieved on live wireless networks
 - Java-based games and applications ported

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Intel® PXA800F Handset Reference Design (with Elektrobit)

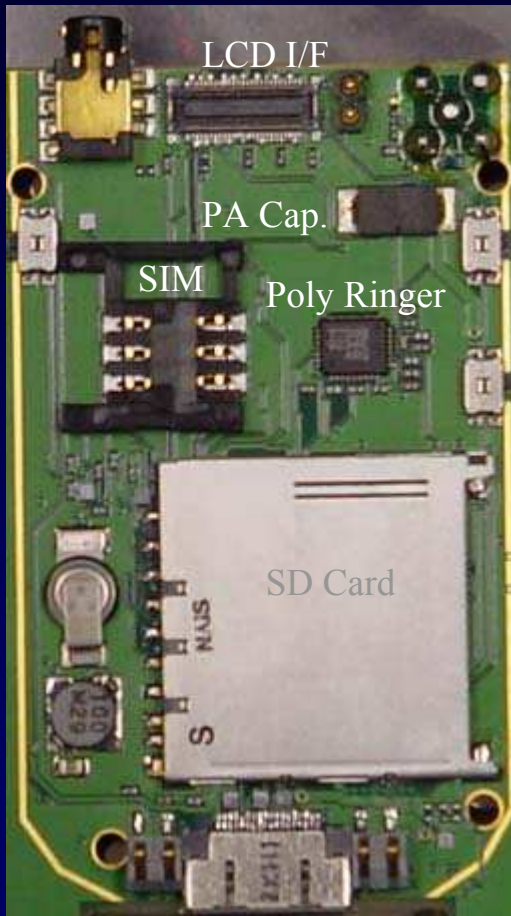


Notes: 3 Unused GPIOs.
Mutually Exclusive Interfaces:
1. Bluetooth Data & IrDA

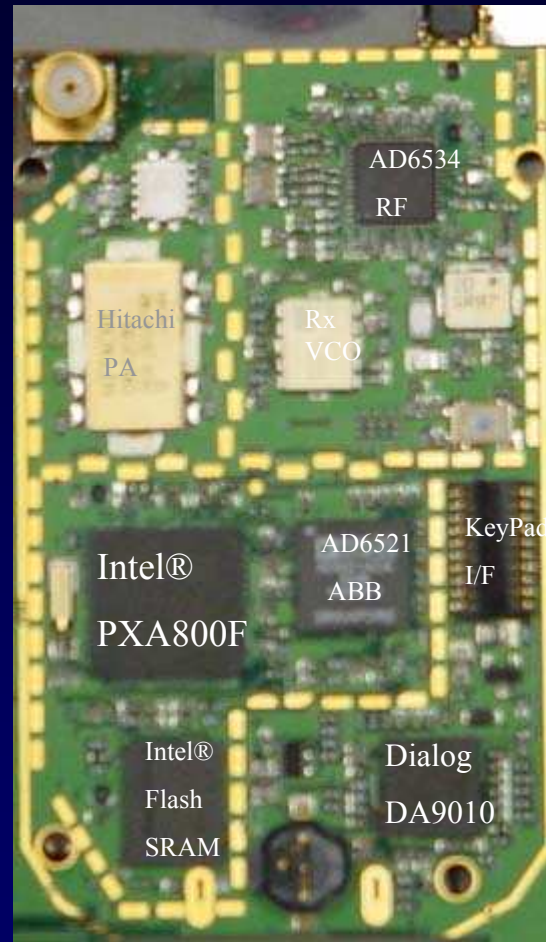


Intel® PXA800F Cellular Processor Handset Reference Design

Bottom



Top



900/1800
SAW

1900
SAW

Intel® PXA800F Cellular Processor Handset Reference Design Phone



ODM phone design with the chip



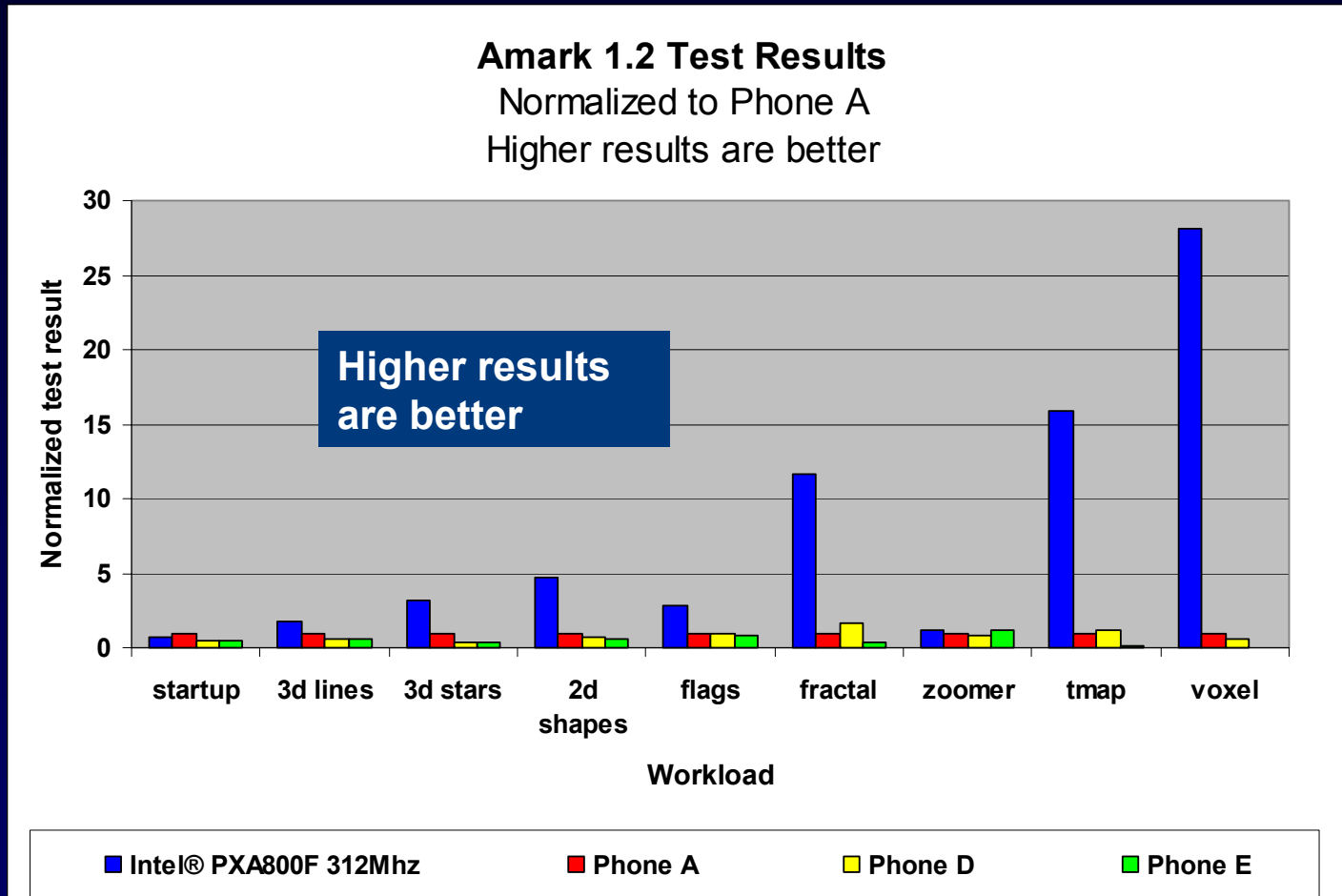
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Performance Results

- Preliminary results follow
 - Recorded test results from Amark* 1.2
 - Recorded test results from Pendragon Software's Embedded CaffeineMark* v3.0
 - Recorded observed frame rates from Jamdat Bowling* game
- Preliminary results show that the Intel® PXA800F cellular processor provides excellent performance in the applications sub-system in the cellular marketplace

Amark* 1.2 Results



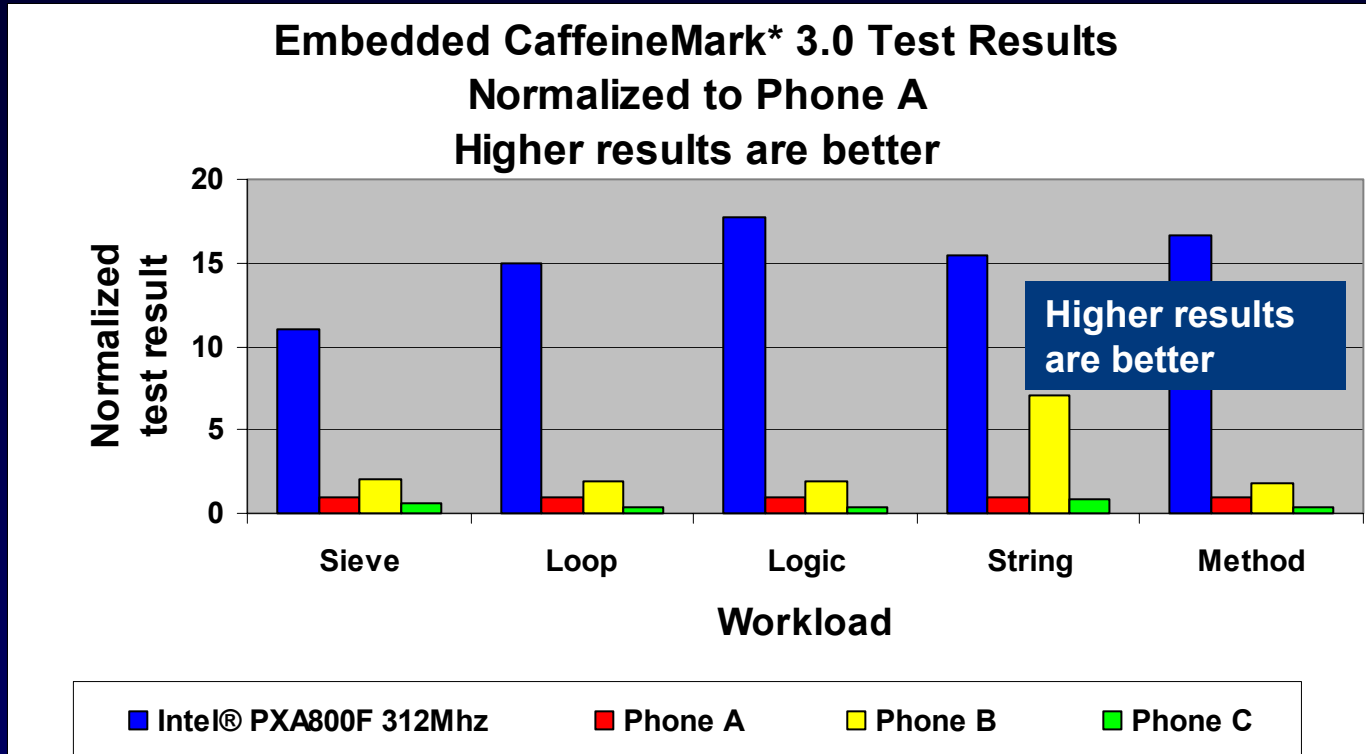
Source: Intel Corporation, using Amark 1.2 (written by Andrea Fasce) to generate test results. Downloaded from <http://www.anfyteam.com/dev/j2me/>.

Test Configuration: Development kit for the Intel® PXA800F cellular processor, with A2 silicon. Intel XScale™ technology running at 312 MHz. 220x176 LCD resolution with 16-bit color depth. Both platform software version 4.30.s02b and midlet were executing primarily from internal Intel flash. Tests conducted with voice call processing enabled with test SIM card inserted. Phone configurations available from manufacturer web sites. For each workload test result shown, the average score of three test runs was determined and then normalized.

Normalization was accomplished by dividing the corresponding workload test result average by the average result obtained by the fastest phone tested (e.g. voxel avg test result of X divided by voxel avg test for fastest phone equals normalized value). Performance tests and ratings are measured using specific computer systems and/or components and reflect the approximate performance of Intel products as measured by those tests. Any difference in system hardware or software design or configuration may affect actual performance.

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Embedded CaffeineMark* v3.0 Workload Results

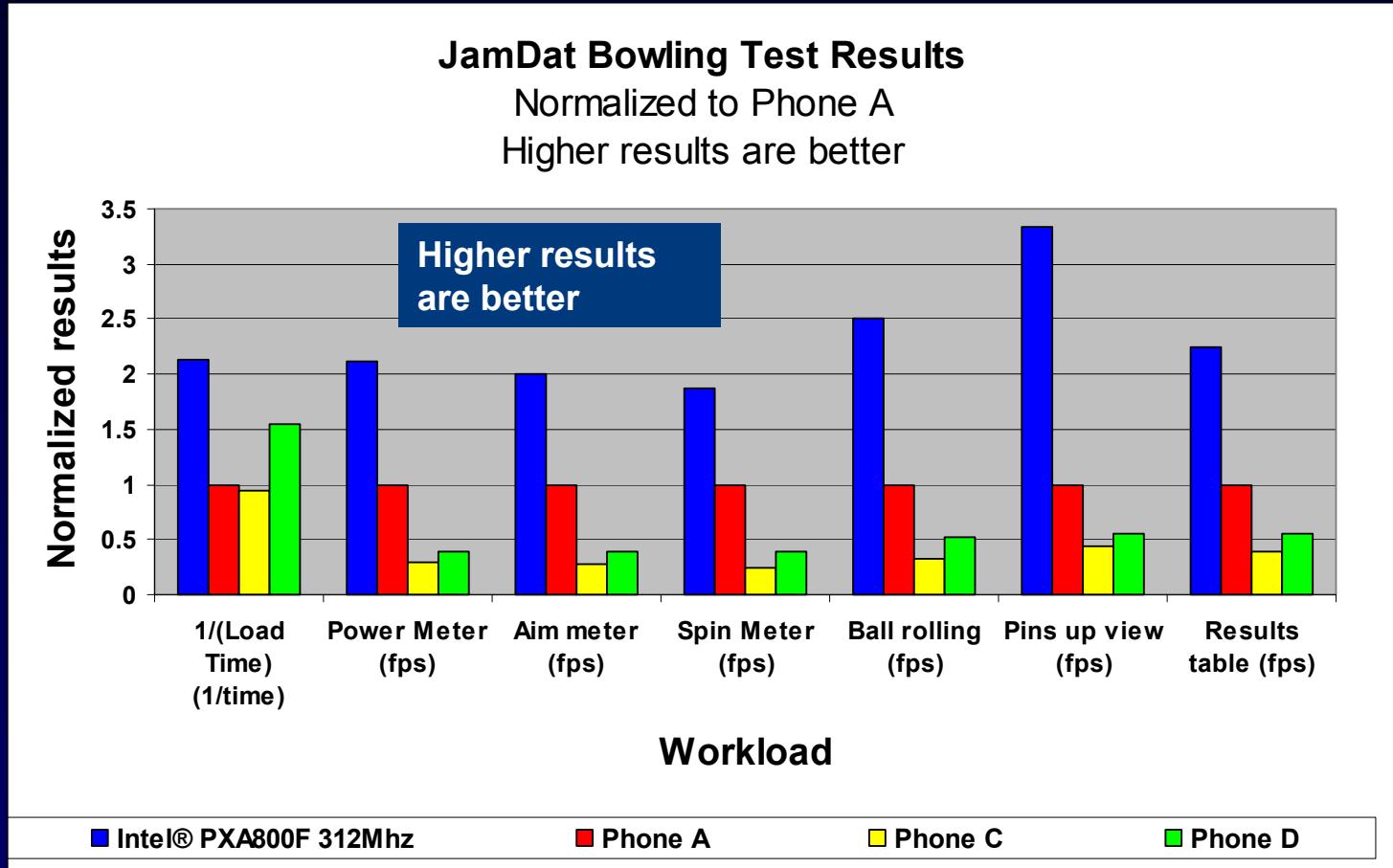


Source: Intel Corporation, using Embedded CaffeineMark* 3.0 software to generate test results. CaffeineMark is a trademark of Pendragon Software. The test was performed without independent verification by Pendragon Software, and they make no representations or warranties as to the result of the test. float workload not tested.

Test Configuration: Development kit for the Intel® PXA800F cellular processor, with A2 silicon. Intel XScale™ technology running at 312 MHz. 220x176 LCD resolution with 16-bit color depth. Software version 4.30.s02b and midlet executing primarily from internal Intel flash. Tests conducted with voice call processing enabled with test SIM card inserted. Phone configurations available from manufacturer web sites. For each workload test result shown, the average score of three test runs was determined and then normalized. Normalization was accomplished by dividing the corresponding workload test result average by the average result obtained by the fastest phone tested (e.g. Sieve avg test result of X divided by Sieve avg test for fastest phone equals normalized value). Performance tests and ratings are measured using specific computer systems and/or components and reflect the approximate performance of Intel products as measured by those tests. Any difference in system hardware or software design or configuration may affect actual performance.

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Jamdat Bowling* Game Results



Source: Intel Corporation, using Jamdat Bowling* game with frame counter enabled. Received midlet from Jamdat.

Test Configuration: Development kit for the Intel® PXA800F cellular processor, with A2 silicon. Intel XScale™ technology running at 312 MHz. 220x176 LCD resolution with 16-bit color depth. Software version 4.30.s02b and midlet executing primarily from internal Intel flash. Tests conducted with voice call processing enabled with test SIM card inserted. Phone configurations available from manufacturer web sites. Each un-normalized test run consisted of observing frames/sec (fps), except for load time, which was time measured by a stopwatch and inverted. The average score of three test runs was determined and then normalized. Normalization was accomplished by dividing the corresponding workload test result average by the average result obtained by the fastest phone tested (e.g. Power Meter avg test result of X divided by Power Meter avg test for fastest phone equals normalized value). Performance tests and ratings are measured using specific computer systems and/or components and reflect the approximate performance of Intel products as measured by those tests. Any difference in system hardware or software design or configuration may affect actual performance.

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- The Intel® PXA800F cellular processor integrates three key Intel technologies...
 - Intel® XScale™ Microarchitecture
 - Intel® Micro Signal Architecture
 - Intel OnChip Flash
- Integration of flash and SRAM memories with dedicated access from cores
 - Provides excellent performance in both apps and comm sub-systems
 - Enables low latencies, power, energy, area, noise, and cost
- Chip has successfully achieved simultaneous optimization of the targeted architecture and design vectors for a GSM/GPRS phone

