DSP™ TEXAS INSTRUMENTS TECHNOLOGY

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TMS320DM310 - A Portable Digital Media Processor

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Portable media devices

- Increasing demand for technology that provides smarter imaging, video, and audio capabilities
- High-performance requirements at a very low power budget
- Need faster time-to-market, upgradeability, multi-standard flexibility, and low overall system cost with high degrees of integration

DM310: A high-level overview

- Highly integrated multimedia engine manufactured in a 0.13µ process (288 pin µ-star BGA package)
- Dual-core SOC with an ARM and a DSP along with several specialized IP blocks and peripherals
- Offers high performance at a low power for portable imaging, video, and audio products
- Fully software programmable solution

Targeted applications

Digital Camcorder

Digital Camera

eBook

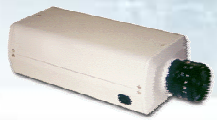
Snapshot Photo Printer

TMS320DM310 DSP

WebPAD

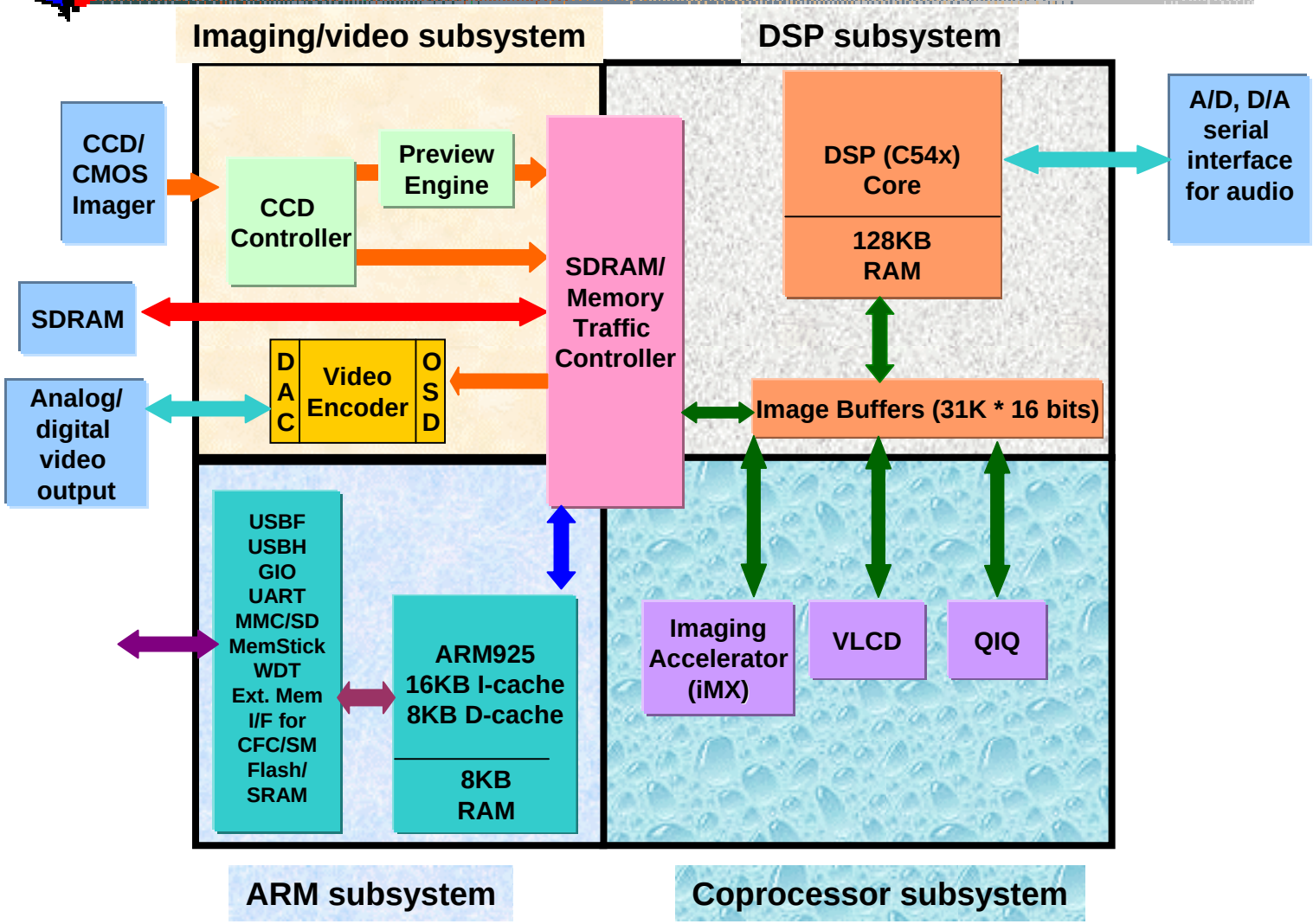
Digital Photo Frame

PDA Cameras



Security Camera

Block Diagram



DSP and Coprocessor subsystems

- Realizes the bulk of the signal processing computations (audio/image/video processing)
- TMS320C54x DSP with 128 KB on-chip RAM
- iMX – an 8-way SIMD/vector processor with dedicated memories for programmable image and video processing
- QIQ and VLCD – programmable hardware blocks that accelerate several image and video compression standards (JPEG, MPEG, H.263, etc)
- DSP clock up to 72 MHz and coprocessor clock up to 144 MHz

ARM subsystem

- Realizes the bulk of the system level tasks (including hosting any operating system)
- ARM925 with 16 KB I-cache, 8 KB D-cache, and a dedicated 8 KB of RAM
- ARM controls all the on-chip blocks except the DSP subsystem (can communicate with DSP if needed)
- Several peripheral blocks are integrated into the ARM subsystem
- Clock frequency up to 120 MHz

Peripherals (ARM subsystem)

- Seamless interface to several media cards (can support 2 cards at the same time) – SD, MMC, CFC, SM, and MS
- Integrated USB host & function, serial I/F, UART, and timers
- Glue less interface to 8-, 16-, and 32-bit external hosts
- Support for Flash (Nand/Nor) and external SRAM
- Multiple on-chip DMAs for data movement between peripherals without ARM intervention

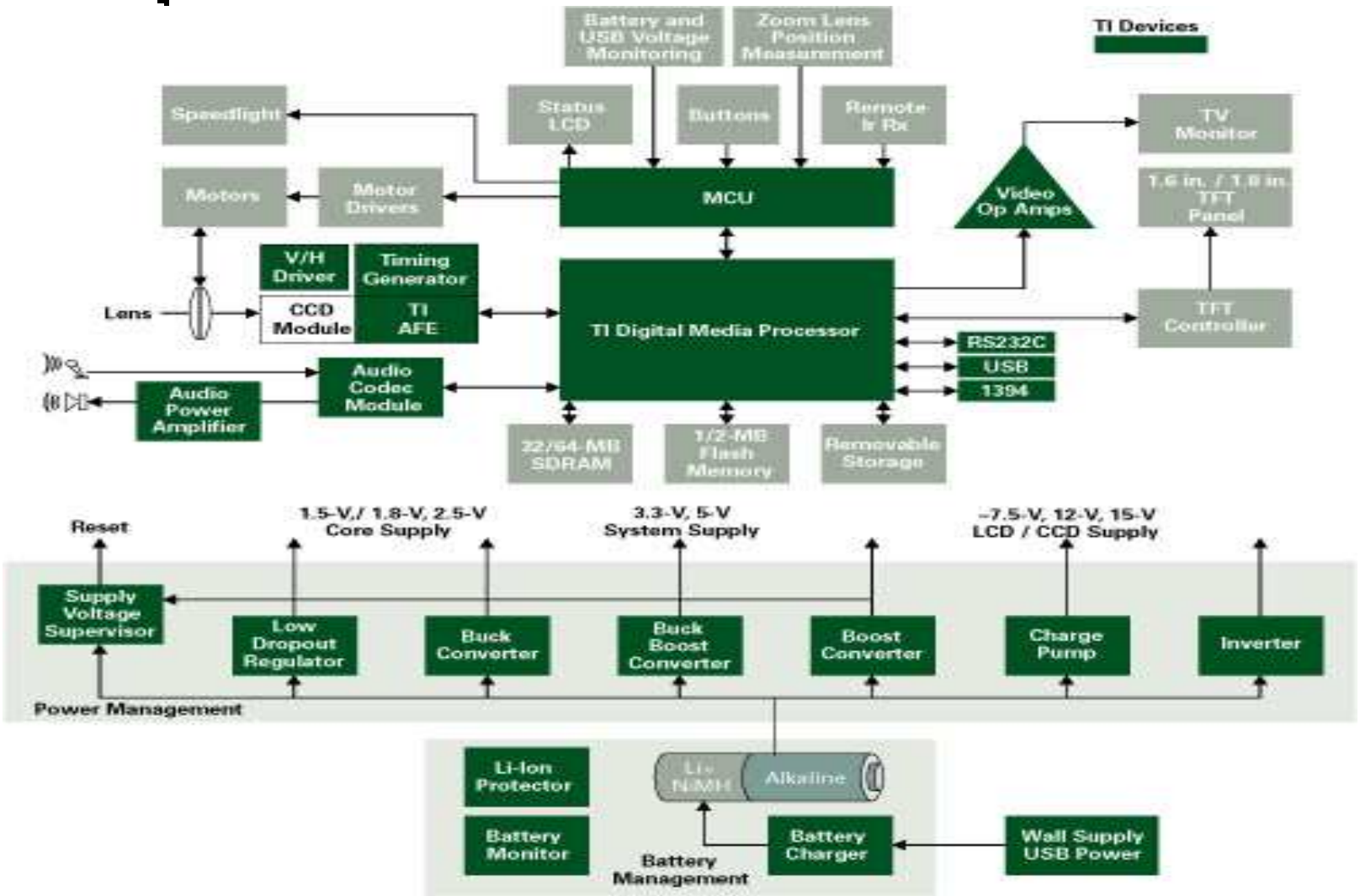
Imaging/video subsystem

- A CCD controller that can interface with all CCD and CMOS sensors and perform pixel processing
- A preview engine that supports real-time (30 f/s) NTSC/PAL video data along with live digital zoom
- A versatile OSD (on-screen display) that can simultaneously display two video, two OSD, and one cursor windows
- A video encoder that supports NTSC/PAL/RGB video output (supports 3 on-chip DACS) and also digital interface for LCDs

SDRAM/Memory traffic controller

- Several sources and sinks to SDRAM exist in the DM310 processor
- All requests are routed through the SDRAM/Memory traffic controller
- Optimized to realize optimum throughput and latency via buffering
- Programmable priority scheme to each requestor in the system
- Several latency intolerant blocks (for functional correctness) exist in the chip

Example end equipment – Digital Still Camera



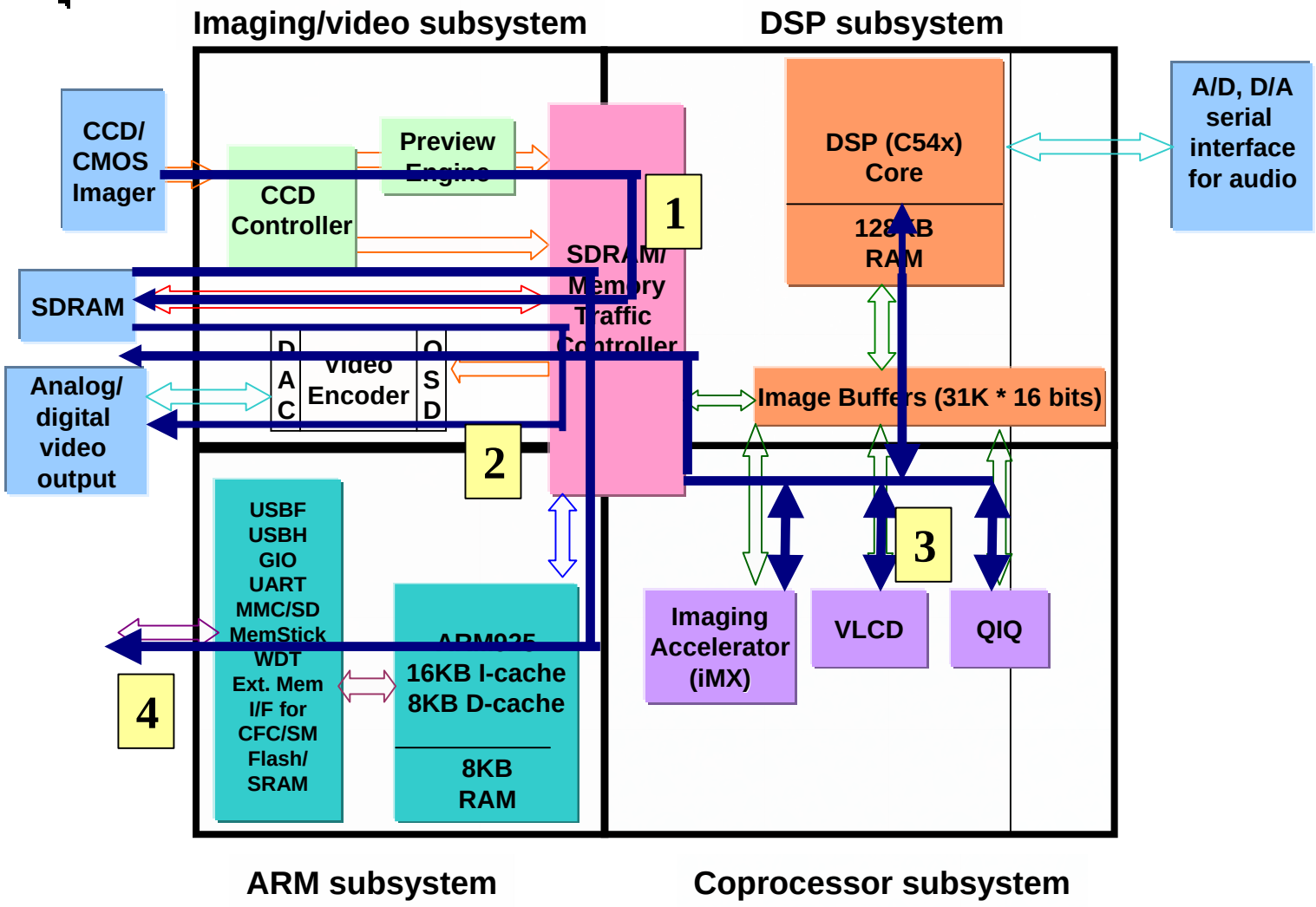
Typical modes of operation

- Still image capture
- Live preview mode
- Still image playback
- Video encode
- Video decode/playback
- Audio encode
- Audio decode
- Photo printing

Example dataflow – Video encode

- Raw data from CCD/CMOS sensor is processed by CCD Controller & Preview engine and written to SDRAM
- Data from SDRAM is read and processed by OSD & video encoder for live viewing on LCD screen
- Data from SDRAM is processed by DSP & coprocessor subsystem for MPEG-4 compression and the compressed data is written back to SDRAM
- Compressed bitstream in the SDRAM is read by the on-chip DMAs in the ARM subsystem and written to a media card

Example dataflow – Video encode (contd.)



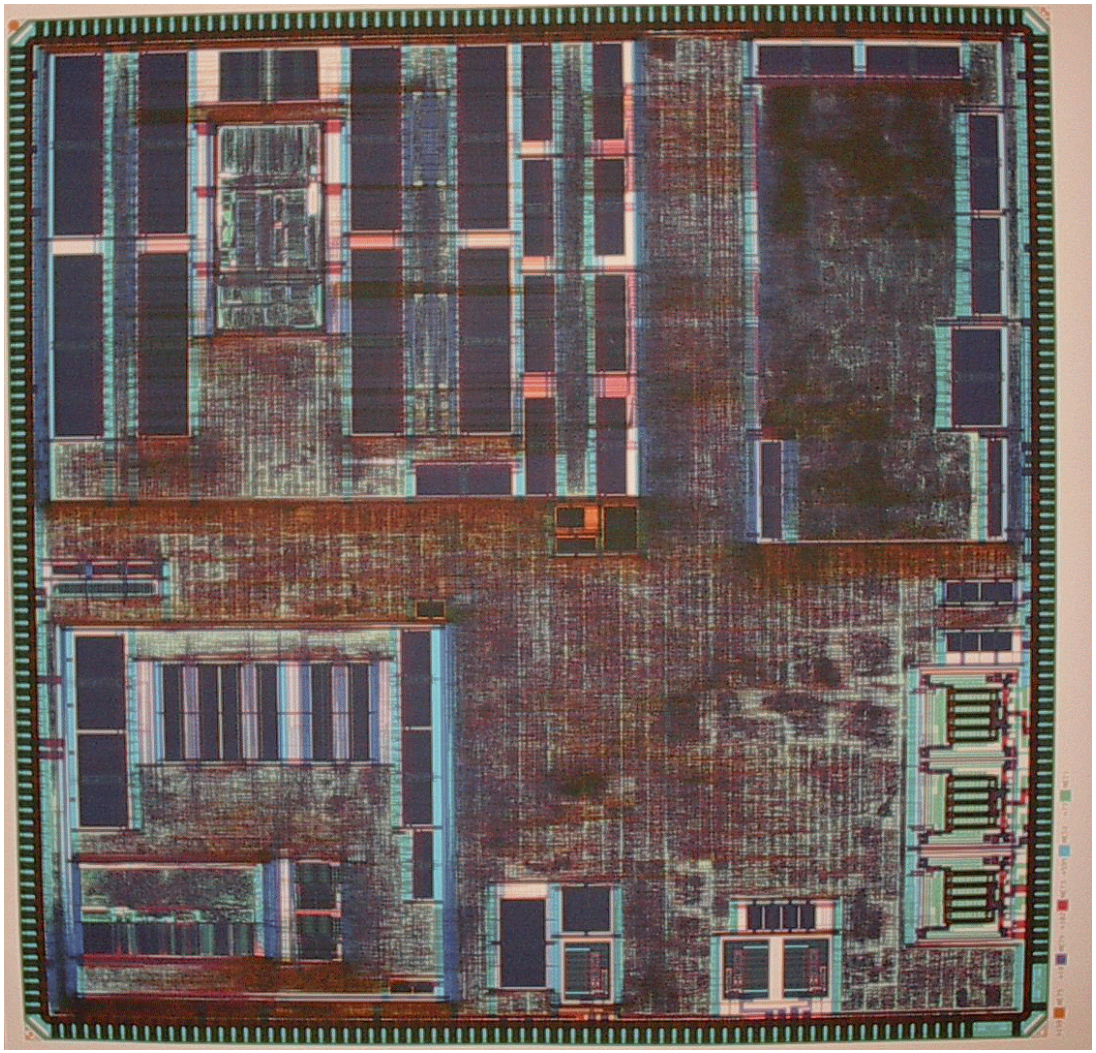
Performance specifications

- Supports multiple applications and file formats including MPEG-1, 2, 4, WMV, H.263, H.264, JPEG, JPEG2K, M-JPEG, MP-3, AAC, and WMA
- Real-time (30 f/s) MPEG-1, 4 video encode at CIF resolution (352 x 288)
- Real-time (30 f/s) MPEG-4 video decode at VGA resolution (640 x 480)
- One-second shot-to-shot delay for processing a raw 6-megapixel image including JPEG compression

Power specifications

- Consumes 250 mW in the video preview mode (whole chip)
- Consumes 400 mW while performing video encoding or video decoding
- Consumes 400 mW while performing still capture of an image (processes 6 Mega pixels/second including JPEG compression)

DM310 die photo



- 0.13µ copper process (GS40) with 5 layers of metal
- 3 analog PLL's on-chip to derive several clock frequencies (highest clock is 144 MHz)
- ~2.3 million gates

DM310 summary

- Serves as the brain behind a wide range of end equipments in the imaging, video, and audio space
- High performance at a very low power budget
- Fully programmable, modular development architecture that supports multiple CODECs, upgrades, and modifications
- Lower overall system cost due to integration of a number of peripherals on-chip

References

- Texas Instruments Inc., press release. *Available at:* http://focus.ti.com/docs/pr/pressrelease.jhtml?prelId=sc02005
- Texas Instruments Inc., “Video and imaging solutions guide”. *Available at:* http://focus.ti.com/pdfs/vf/vidimg/VI_SG_20021125.pdf
- Texas Instruments Inc., “TMS320DSC21- A high-performance, programmable, single chip digital signal processing solution to digital still cameras”. *Available from the digital still cameras link at:* http://focus.ti.com/docs/apps/appshomepage.jhtml
- Texas Instruments Inc., “Programmable DSP platform for digital still cameras”. *Application note available at:* http://www-s.ti.com/sc/psheets/spra651/spra651.pdf