RAMP-IV: A Low-Power and High-Performance 2D/3D Graphics Accelerator for Mobile Multimedia Applications

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3D Embedded
by KAIST RAMP-IV

Outline

- Introduction
  - 3D Graphics on Hands
  - Technical Barriers
  - RAMP Overview
- RAMP-IV Architecture
  - High Performance @ Low Power
  - Low Cost Implementation
- Demonstration
  - REMY : System Evaluation Board
  - MobileGL : Graphics Library for Mobile Devices
- Conclusions

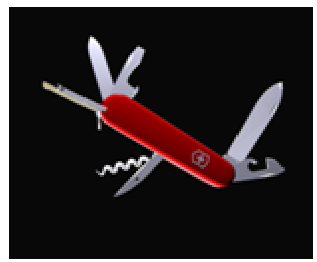
Evolution of the Cell-Phone

- Mobile Multimedia Center
  - Camera
  - 2D Graphics
  - MP3 Audio
  - MPEG-4 Video
  - Java Gaming

- **3DCG is the next step !**

Avatar

Game



Advertisement

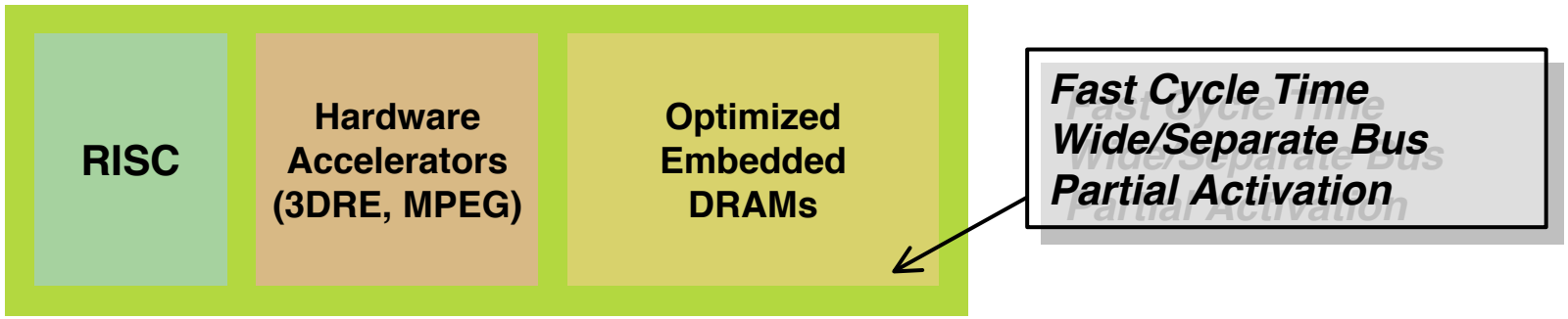
Technical Barriers

- **Limited** Energy supplied by Battery
  - 200mW for 3DCG : 2~3hrs Playback
- **Limited** Resources
  - 400MHz Host Processor without FPU
  - 400MB/s System Memory
- **Limited** Footprint
  - Not Enough Space for 2D/3D Accelerator + Graphics Memories
- **Low** Cost
- **No** Standard 3D Graphics API for Mobile Devices

Low-Power 2D/3D Accelerator integrated with Rendering Memories by DRAM Process Technology → RAMP

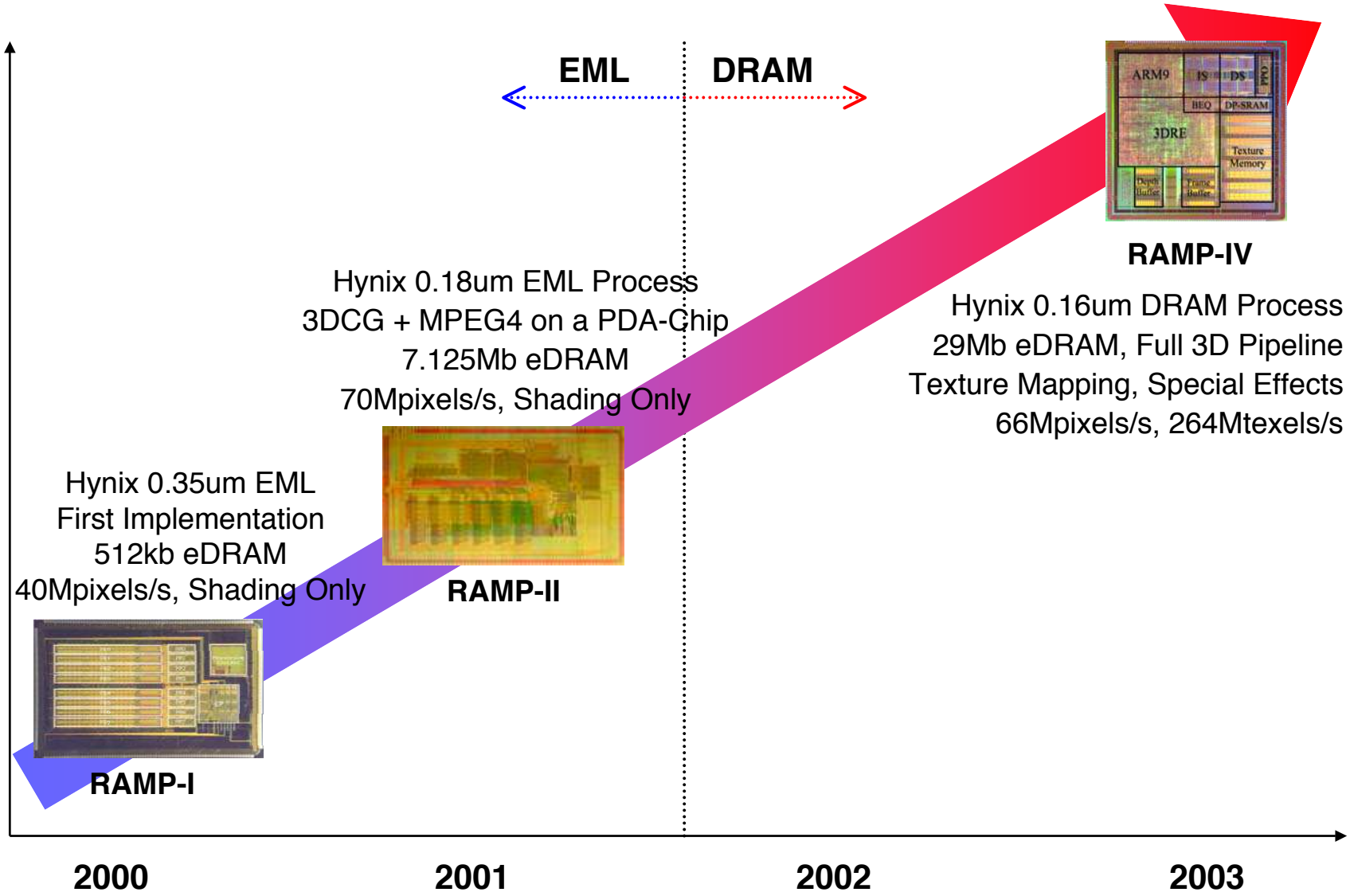
What is RAMP ?

- RAMP : RAM + Processor
  - Mobile Multimedia Processor with Application Specific Embedded DRAMs
    - High-Level of Integration
    - Low Power Consumption
    - High Performance through Huge Memory Bandwidth
  - Platform integrated with IP Cores



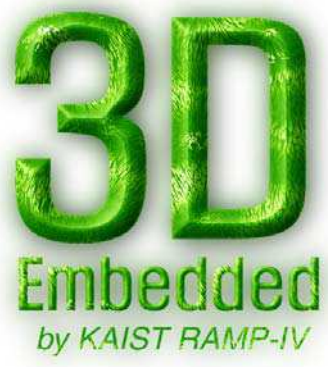
  - Merged-DRAM Fabrication Process
    - Embedded Memory Logic (EML)→ Pure DRAM

RAMP History

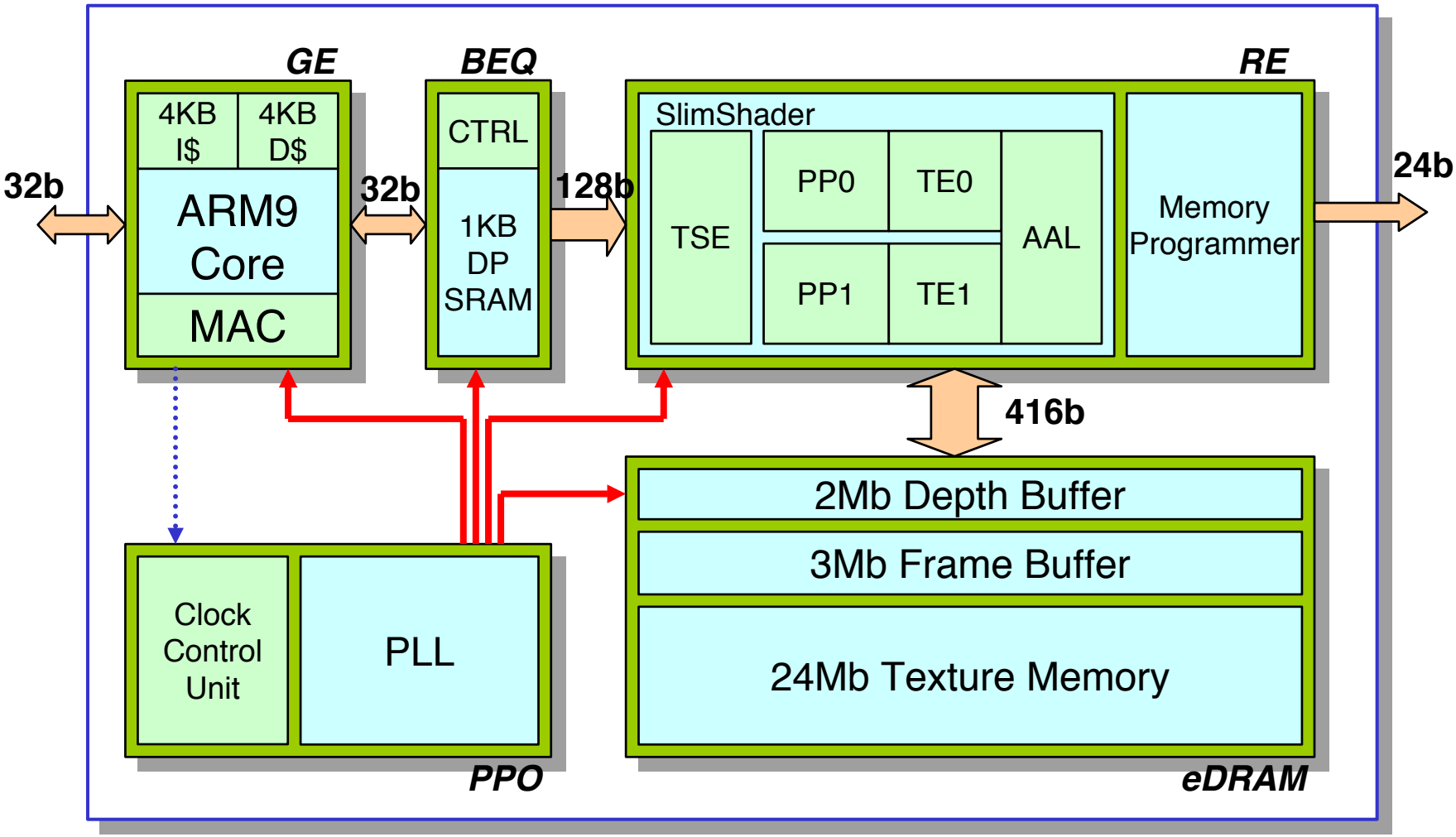


RAMP-IV Standouts

- Highest Performance @ Low Power
  - Highest Integration Level
  - Full 3D Pipeline with Complete Rendering Memories
    - Texture Mapping, Special Effects
    - Large On-Chip Memory
- Low-Power Techniques
  - Datapath
  - Shading / Texture Unit
  - Memory Activation
  - Clock Gating / Management
- Low-Cost Implementation
  - 256Mb DRAM Process

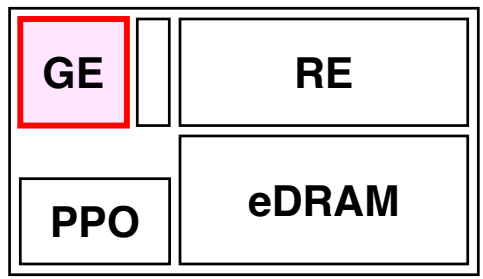


RAMP-IV Architecture



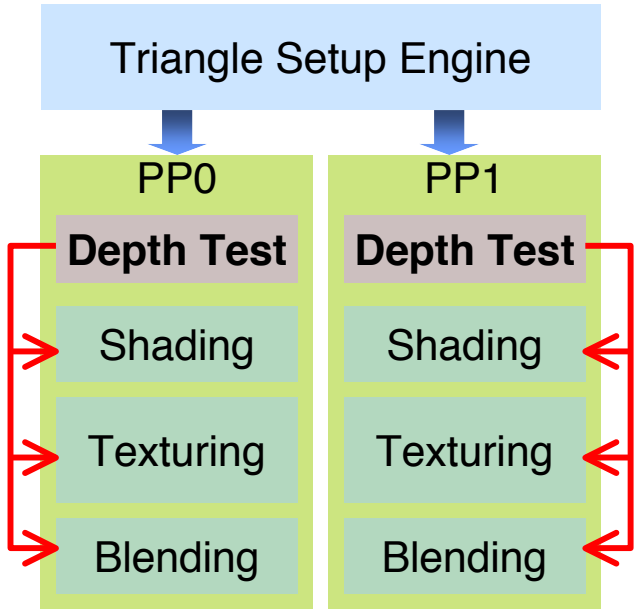
Geometry Engine

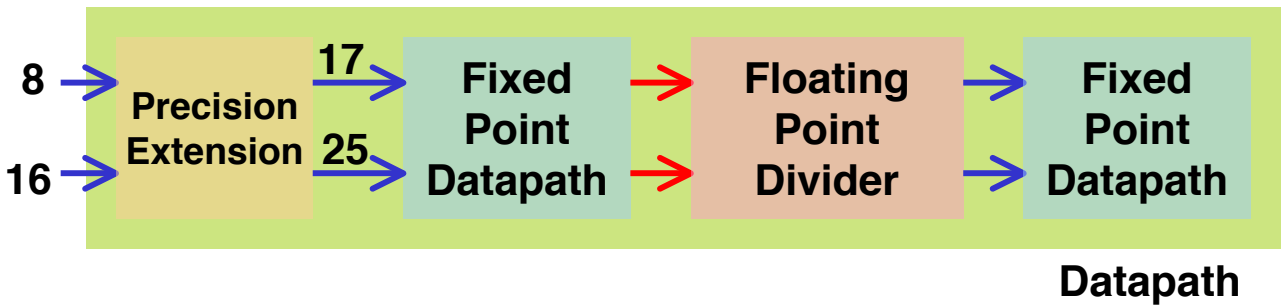
- General Purpose RISC + MAC
  - 133MHz 32bit ARM9 ISA
  - Programmability : No Hard-wired T&L Engine
    - Main Host Processor forStandalone Configuration
  - Enhanced MAC : 32b x 32b MAC in a single cycle
    - 3D Geometry, MPEG Acceleration
    - 1.04Mvertices/s Transformation (**43% Improvement**)
- Working with Proprietary MobileGL
  - Hand-Optimized for ARM Datapath with Integer MAC
    - Fixed Point Arithmetic
    - **x10 Improvement** against Floating-Point Emulation
  - Subset of de-facto Standard OpenGL
  - 70kB Library Size

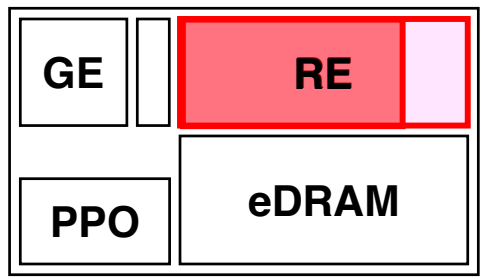


Rendering Engine : SlimShader

- Main Rendering Pipeline
  - 3D Acceleration
  - 2D through 3D Datapath
- Pipeline Clock Gating
  - Early Depth Test
  - Pixel-Level Gating
- Precision-Controlled Datapath
  - **95% Power and 85% Area Reduction**

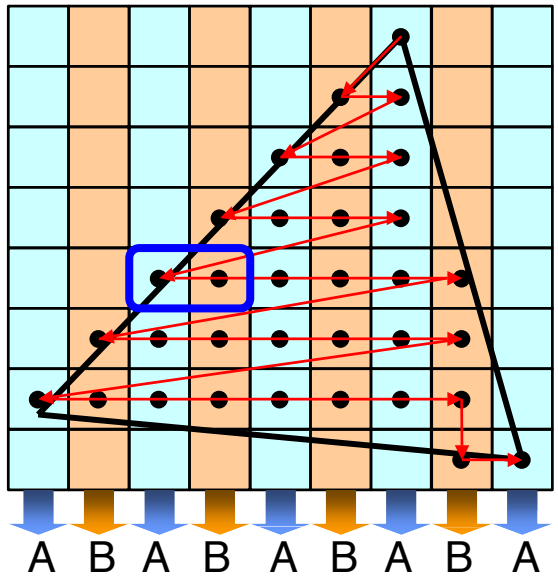


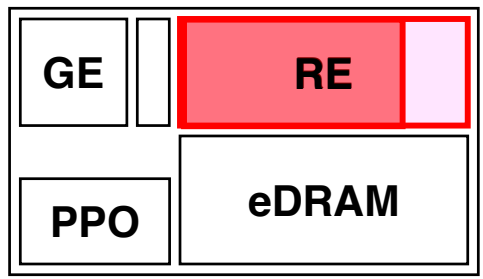




Rendering Engine : SlimShader

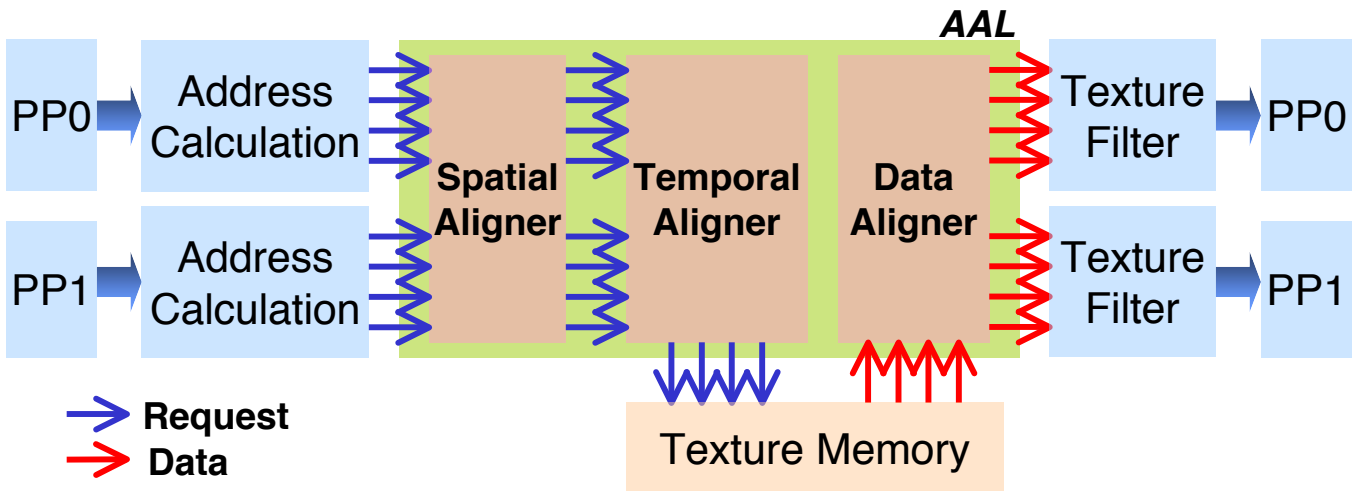
- Frame/Depth Buffer
  - Vertical-Stripe Assignment
  - Independent Access Ports
- Per-Triangle Parameter Setup
  - Horizontal-Order Rasterization
    - Easy Memory Addressing
    - Simple Pipeline Control
    - DRAM Page Issues : Solved by 3D-Optimized DRAM
- Two Pixel Processors
  - Energy Efficient : Address Alignment Logic
  - Render Horizontally-Adjacent Pixels
    - Easy to Gather Texture Addresses
    - Simple Assignment

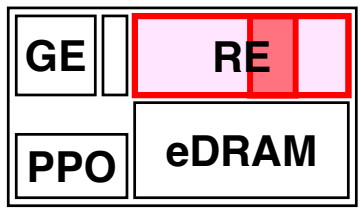




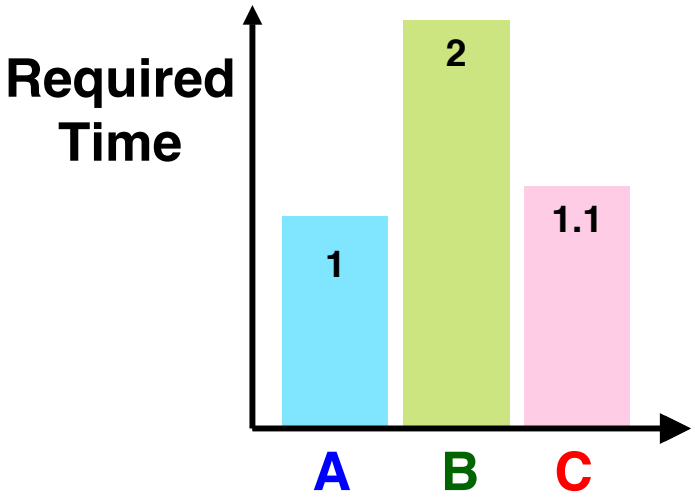
Rendering Engine : Texture Unit

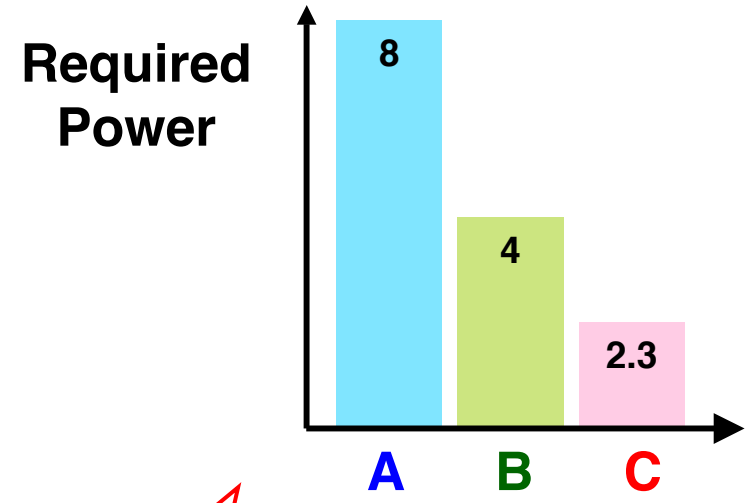
- Two Texture Units
  - Single-Cycle Per-Pixel Dividers for Perspective-Correction
  - Single-Cycle Bilinear MIPMAP Filter
- Address Alignment Logic
  - Energy-Efficient Texturing Unit
  - **Attached to 4 Texture Memories**
  - Exploiting Locality without using Complex Texture Cache
  - Using Pipeline Latches to store Recently-Used Texels

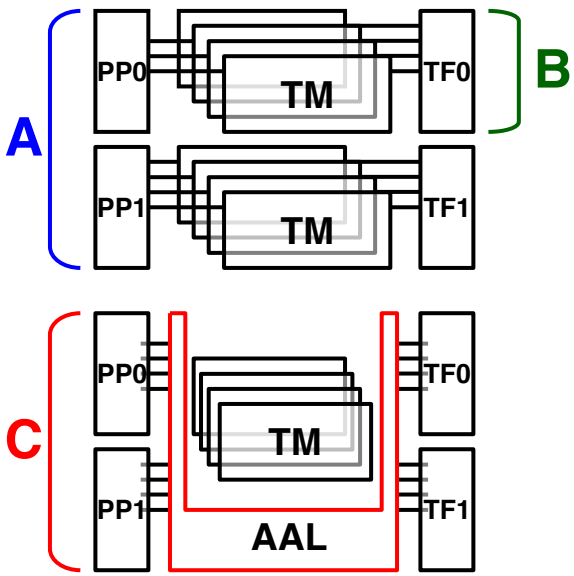


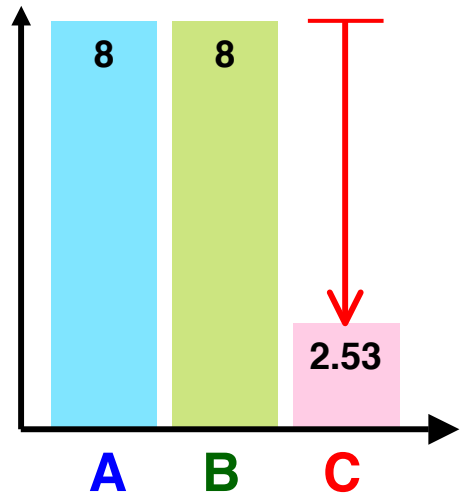


Benefit of Address Alignment Logic



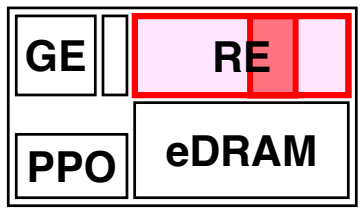




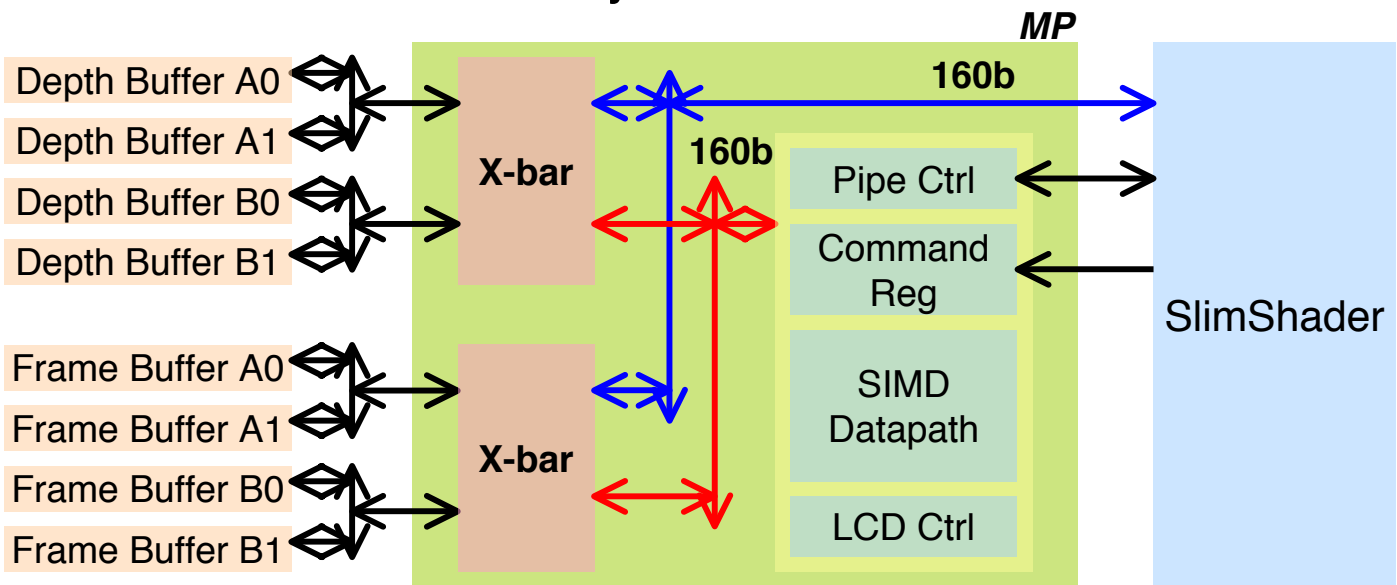


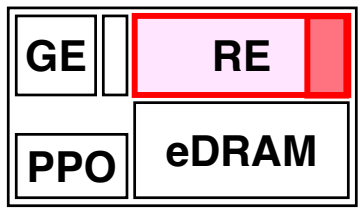
Required Energy

68% Reduction

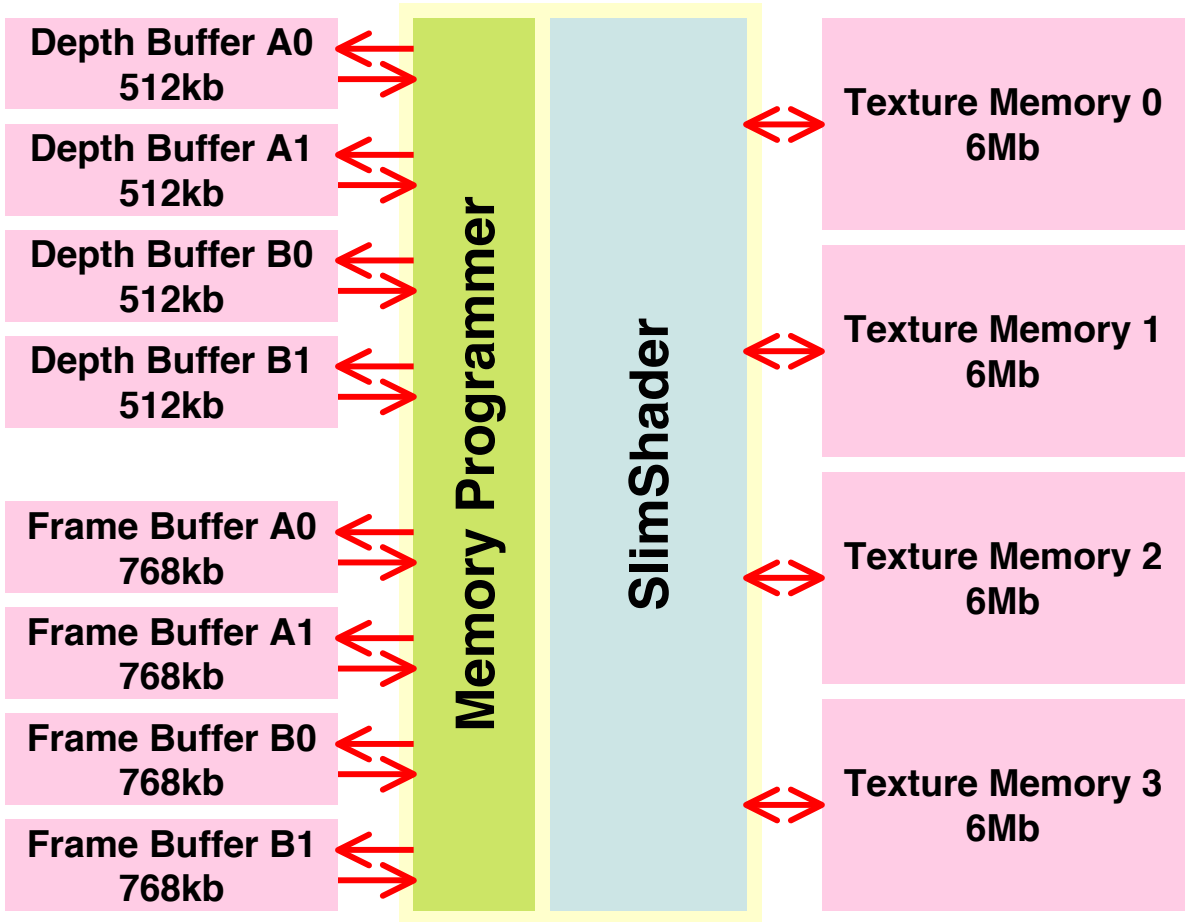


- Post Processing Unit
  - **Pixel-Programmability without Cycle Penalty**
  - Special Rendering Effects
    - Antialiasing, Fog, Motion Blur
  - Working in Parallel with SlimShader
    - 2-pixel-wide SIMD-Parallel Datapath
    - 160-bit Memory Crossbar



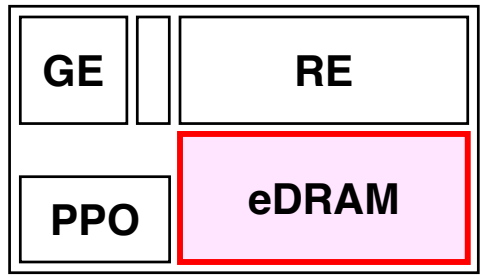


- Memory Configuration

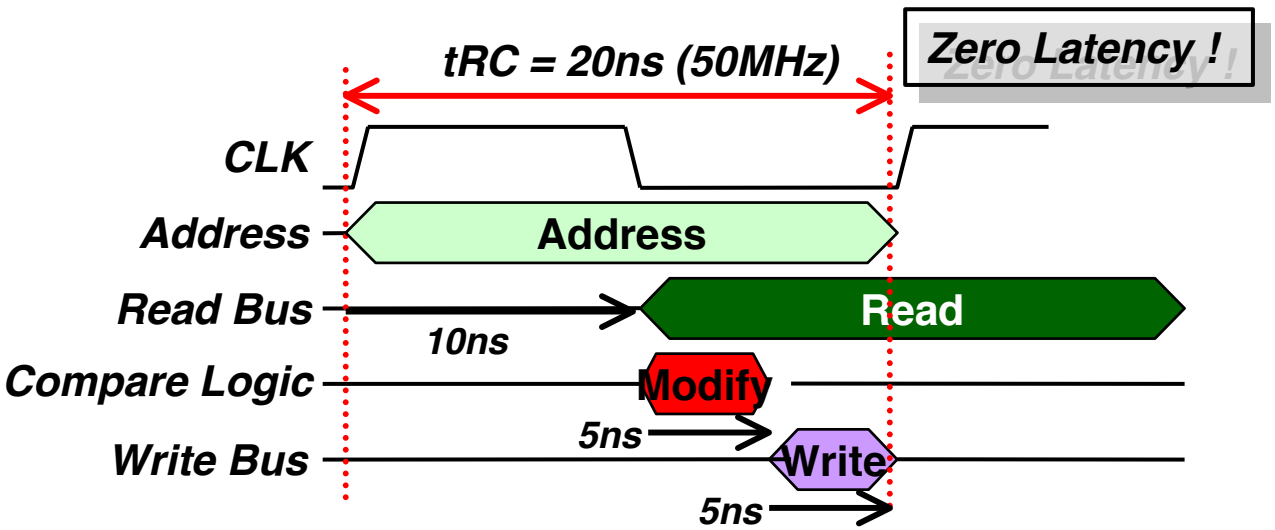


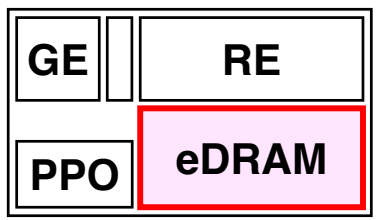
Selective Activation
- Optimized Access
- 75% Power Reduction

Huge Bandwidth
- 416bit
- 1.6GB @ 33MHz



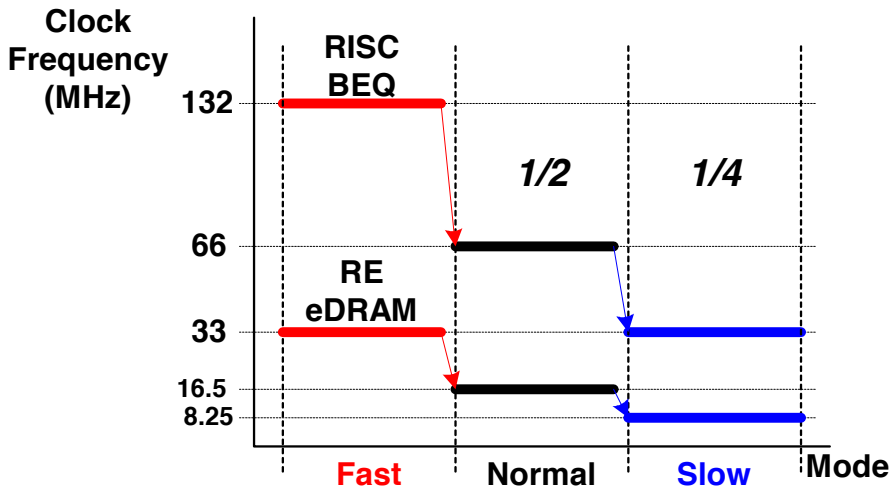
- Optimized for 3D Graphics
  - Fast Random Row Cycle
    - Matched with Maximum Logic Cycle
    - No Need to Worry about Page-Access
  - Single-Cycle Read-Modify-Write
    - Ideal for Depth-Test, Alpha-Blending
    - Simple Memory Interface



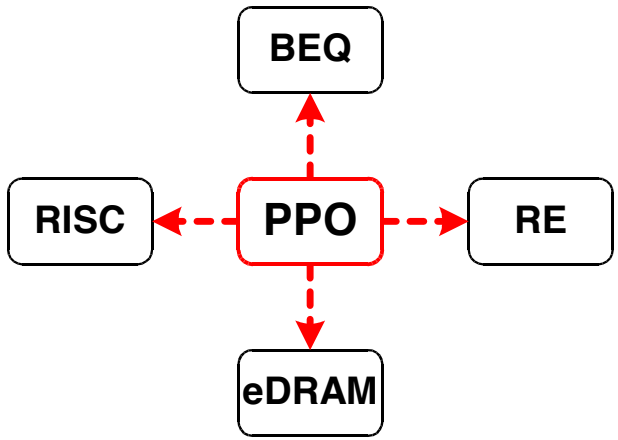


Programmable Power Optimizer

- Run-time Clock Control

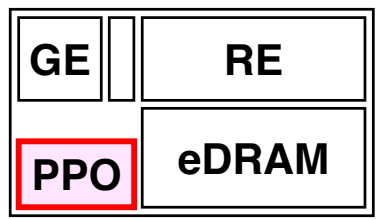


Frequency Scaling



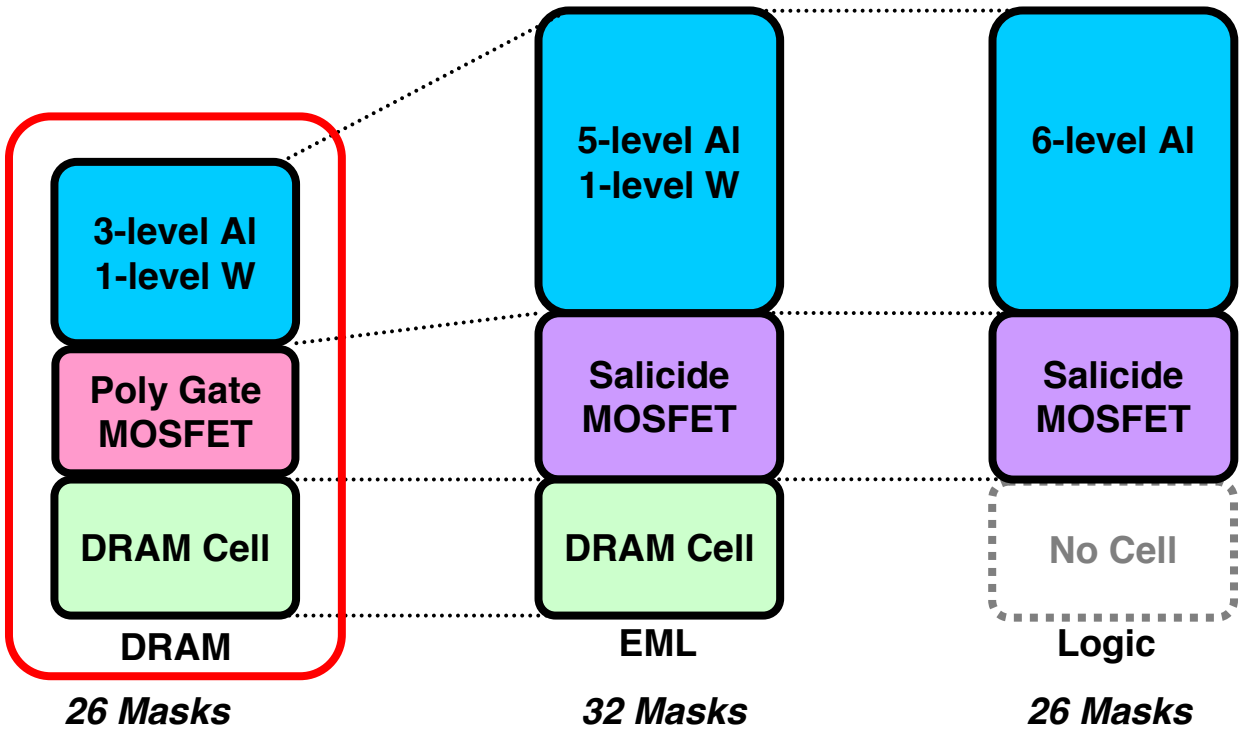
Coarse-Grained CLK Gating

- Fully Controlled by the Software
- Adjusting the Frame-Rate during Run-time
- Zero-latency Frequency Change

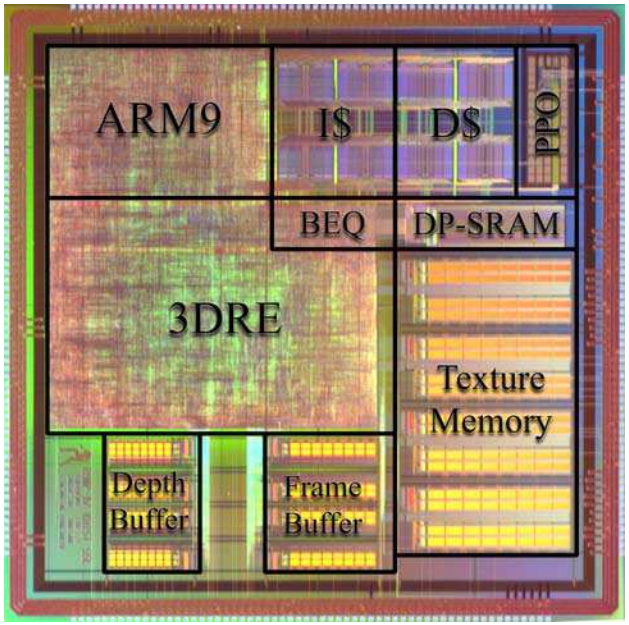


Low-Cost Implementation

- DRAM-based SoC Implementation
  - Low Cost : 256Mb DRAM
  - **"Embedded Processor" into a DRAM-die**
  - Large On-Chip Memory
  - Inherently Low-Leakage Current
  - Adequate for Mobile Multimedia Processors

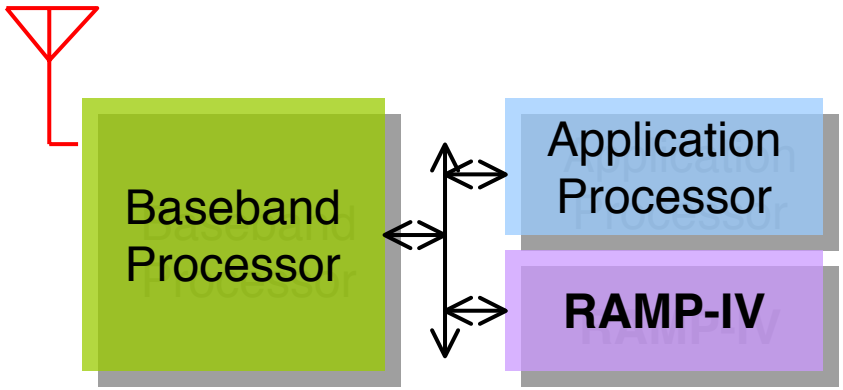


RAMP-IV Characteristics

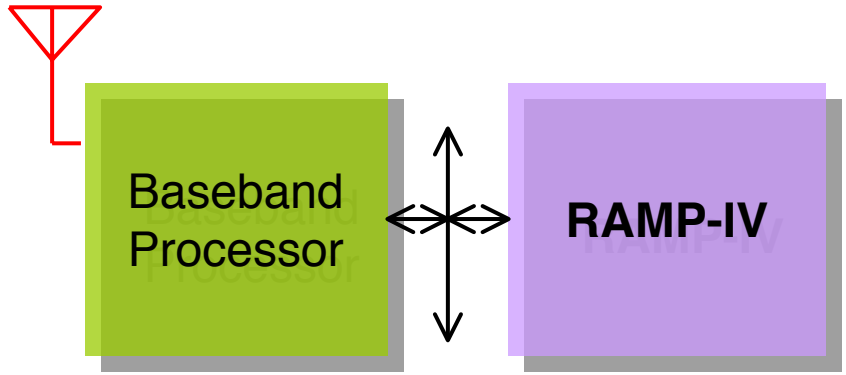


- 0.16um Hynix**DRAM** with 1-W 3-Al
- Power Supply
  - 2.0V (eDRAM : Core Transistors)
  - 2.5V (Logic : Periphery Transistors)
  - 3.3V (I/O)
- Power Consumption
  - **<210mW (Textured 3D @ FAST)**
  - <145mW (Non-Textured 3D @ FAST)
  - < 85mW (MPEG-4 @ FAST)
- Die Size
  - **121mm^2** (11mm x 11mm)
- **Rendering Performance**
  - **1Mvertices/s with MobileGL**
  - **66Mpixels/s, 264Mtexels/s**
  - **Perspective-Correct Bilinear MIPMAP Texturing**
  - **Special Rendering Effects**
  - **29Mb Rendering Memories**

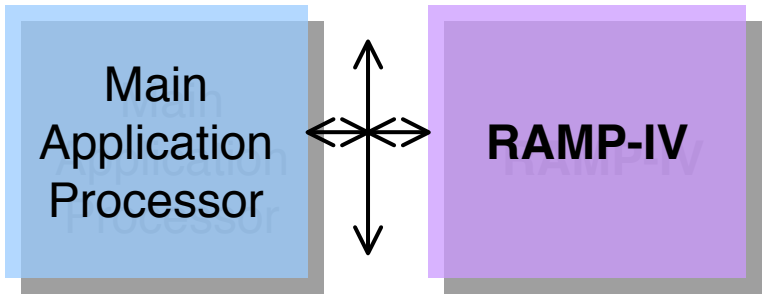
Target Configuration



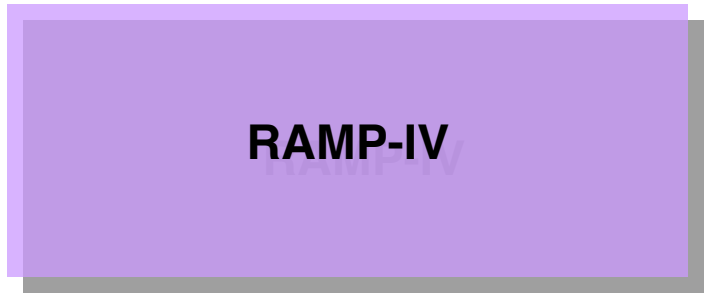
Integration with existing A.P.
→ Highend Cell-Phone



Replacement of existing A.P.
→ Low-Cost Cell-Phone



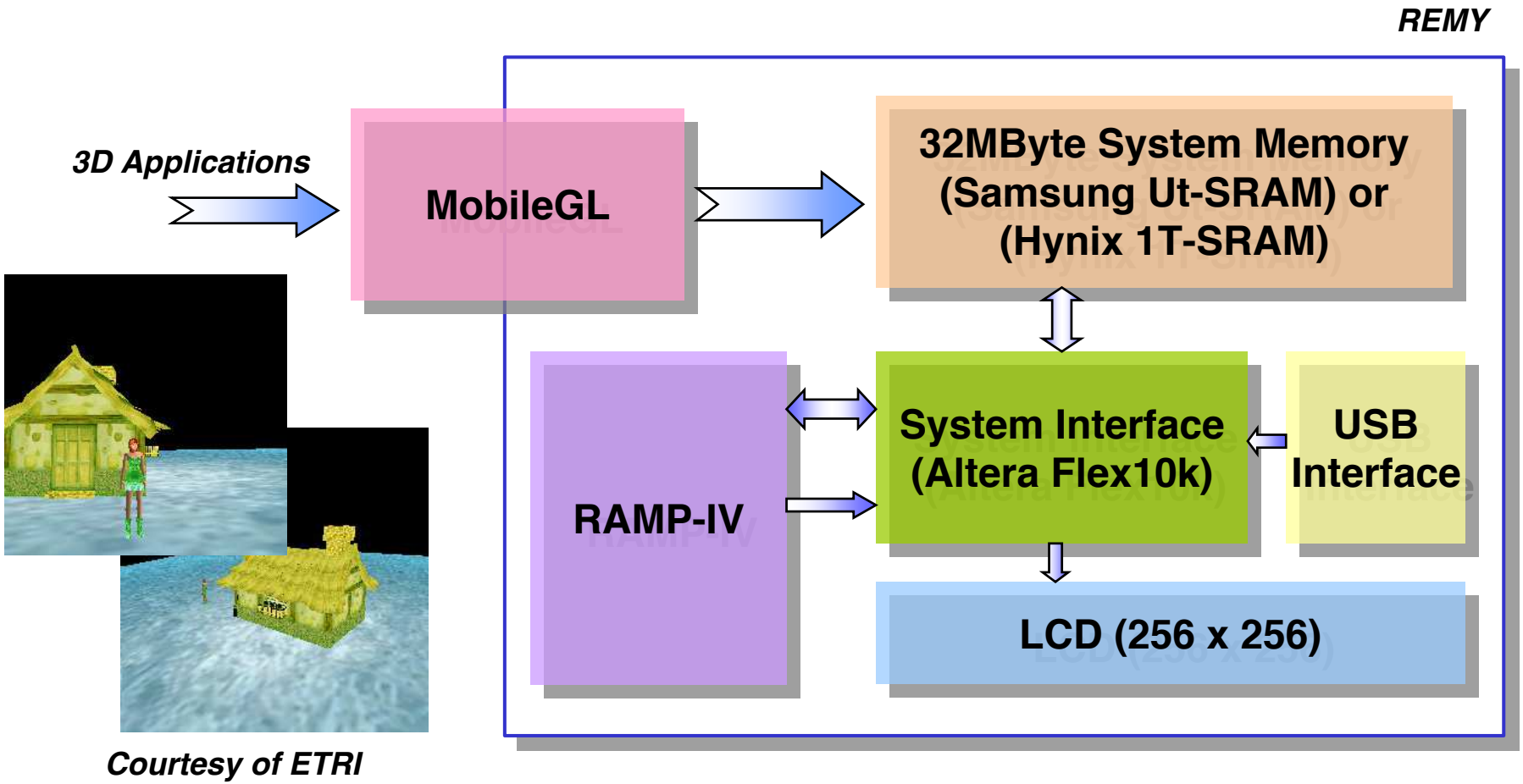
Attached to main A.P.
→ Highend PDA
→ Highend Game Terminal



Standalone Processor
→ Low-Cost Game Terminal

REMY : System Evaluation Board

- System Configuration
  - Standalone Processor



Courtesy of ETRI

REMY : Demonstration Video

- REMY-I

REMY : Demonstration Video

- REMY-II

Conclusions

- RAMP-IV
  - 2D/3D Graphics Accelerator for Mobile Multimedia Applications
  - Highest Level of Integration : GE + RE + DRAM + PPO
  - Highest Performance : 66Mpixels/s, 264Mtexels/s
  - Low Power Consumption : Less than 210mW
  - Low Cost 256Mb DRAM Technology
- FEMY
  - Demonstration System
  - MobileGL : Fixed-Point Graphics Library
- 3DCG is Ready for Cell-phones and PDAs !

Related Materials

- Ramchan Woo, et al, “A 210mW Graphics LSI Implementing Full 3D Pipeline with 264Mtexels/s Texturing for Mobile Multimedia Applications,” in *ISSCC Digest of Technical Papers*, pp. 44-45, Feb. 2003

- Ramchan Woo, et al., “A 120mW 3D Rendering Engine with 6Mb Embedded DRAM and 3.2Gbyte/s Runtime Reconfigurable Bus for PDA-Chip,” *IEEE J. Solid-State Circuits*, vol. 37, pp. 1352-1355, Oct. 2002

- Chi-Weon Yoon et al, “A 80/20MHz 160mW Multimedia Processor integrated with Embedded DRAM, MPEG-4 and 3D Rendering Engine for Mobile Applications,” *IEEE J. Solid-State Circuits*, vol. 36, pp. 1758-1767, Nov. 2001

- Yong-Ha Park, et al, “A 7.1-GB/s Low-Power Rendering Engine in 2-D Array-Embedded Memory Logic CMOS for Portable Multimedia System,” *IEEE J. Solid-State Circuits*, vol. 36, pp. 944-955, Jun. 2001

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