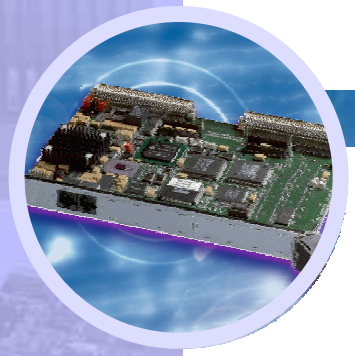

A UMTS Baseband Receiver Chip for Infrastructure Applications

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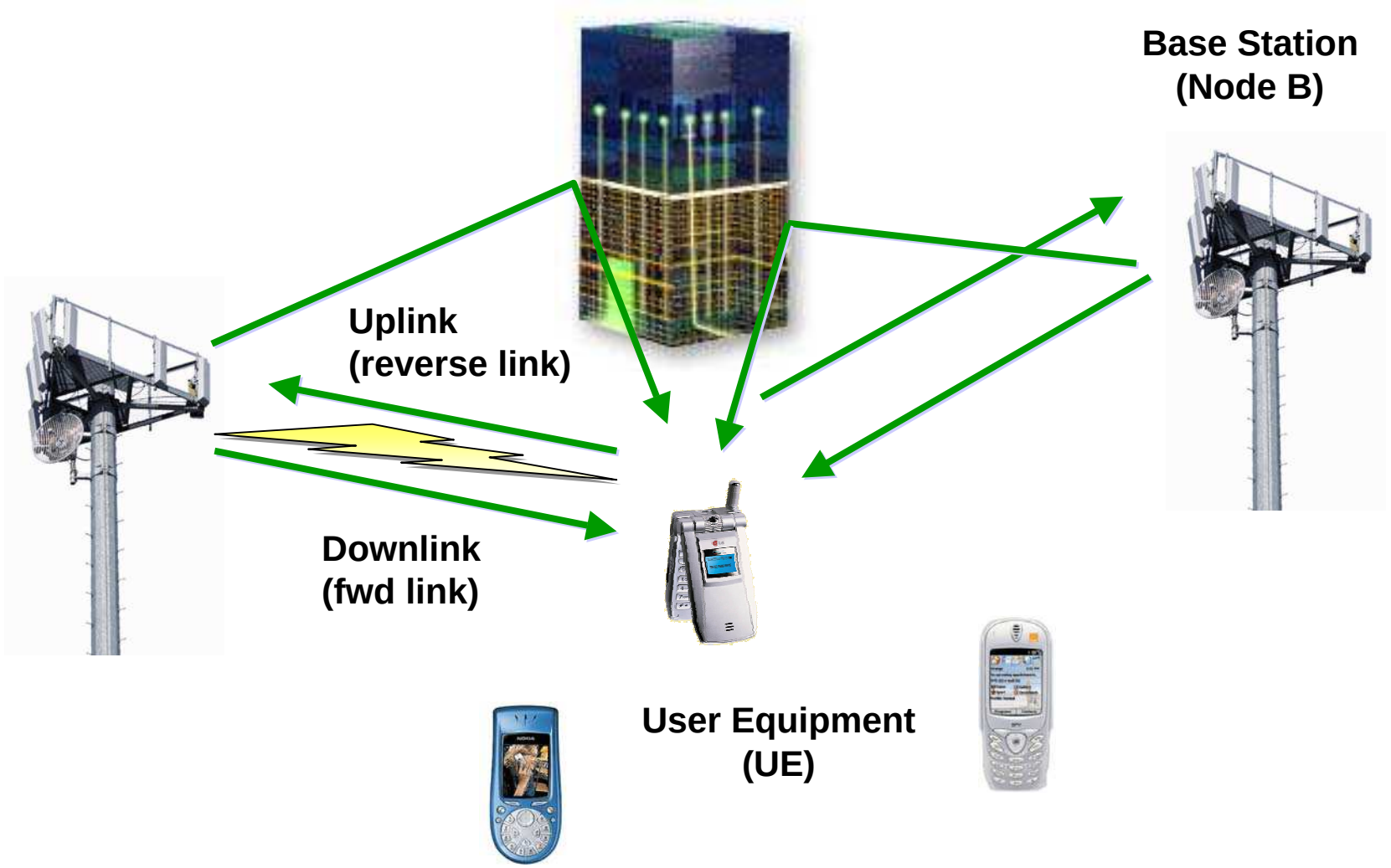
Outline

- UMTS/CDMA Cellular System Overview
- CDMA Base Station Receiver Functions
- System Partitioning
- The TCI110 Receive Chip-rate Application Specific Signal Processor (ASSP)
  - Correlator architecture
  - Front-end buffer
  - Finger de-spreader
  - Path searcher
  - Preamble detector
  - Host Interface
- Summary

Cellular System



UMTS FDD 3G Standard

- **Frequency Division Duplex**
- **Wideband CDMA**
- **Variable data rates and associated services**
  - **2 MBPS peak rate**
- **Network backward compatible to GSM**

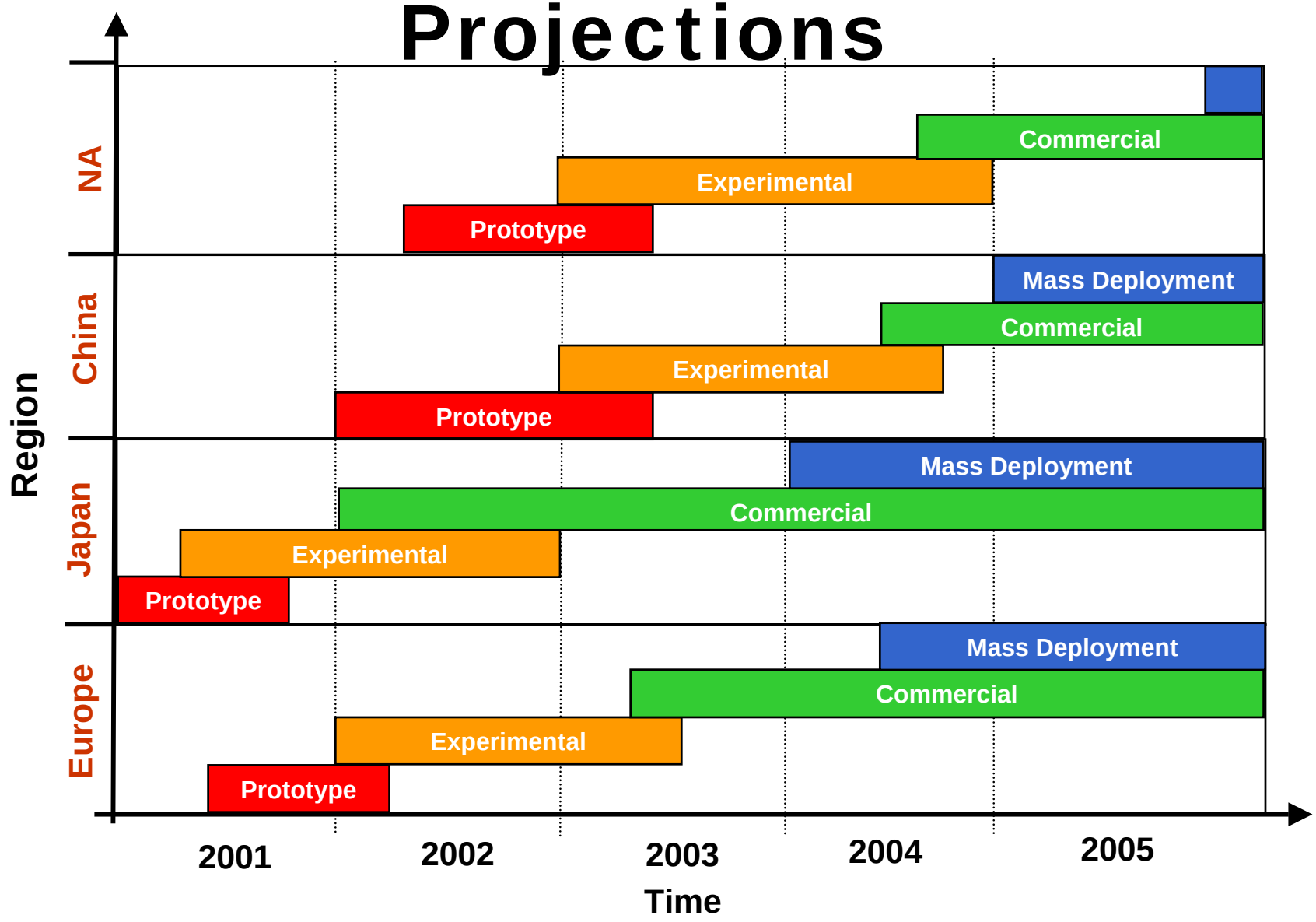
3G Base Station: Key Care-abouts

Cost per channel

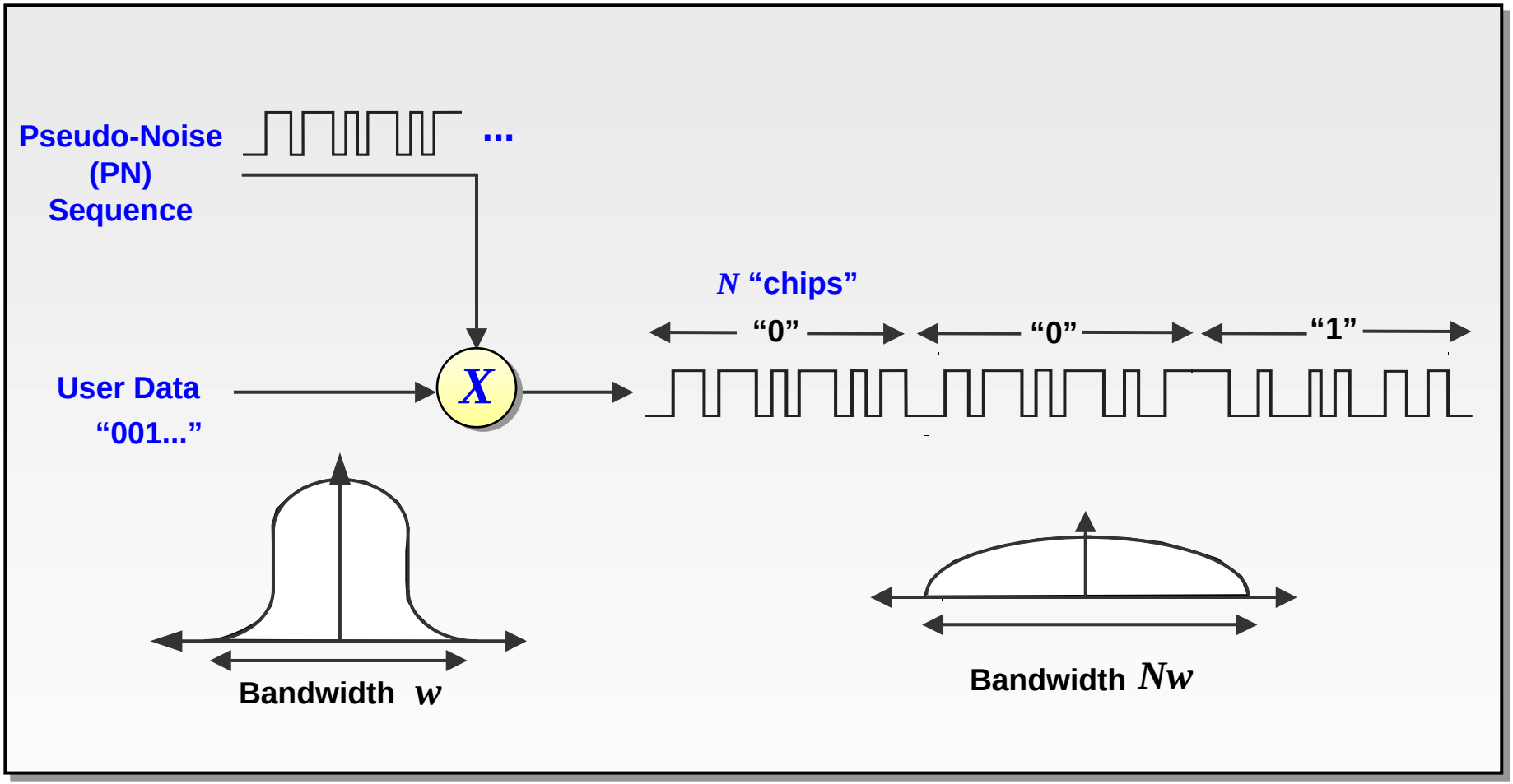
Flexibility

- Variable data rate and traffic
  - Mix of rates from 12.2Kbps (voice) up to 2Mbps (data)
- Flexible cell sizes
  - Macro/Micro/Pico/In-door
- Support of disparate environments
  - Vehicular, pedestrian, stationary
- Flexible resource allocation
  - Seamless processing/memory trade-off between various traffic scenarios
- Flexible implementation of base-band algorithms
  - Allow for field upgrades/enhancements

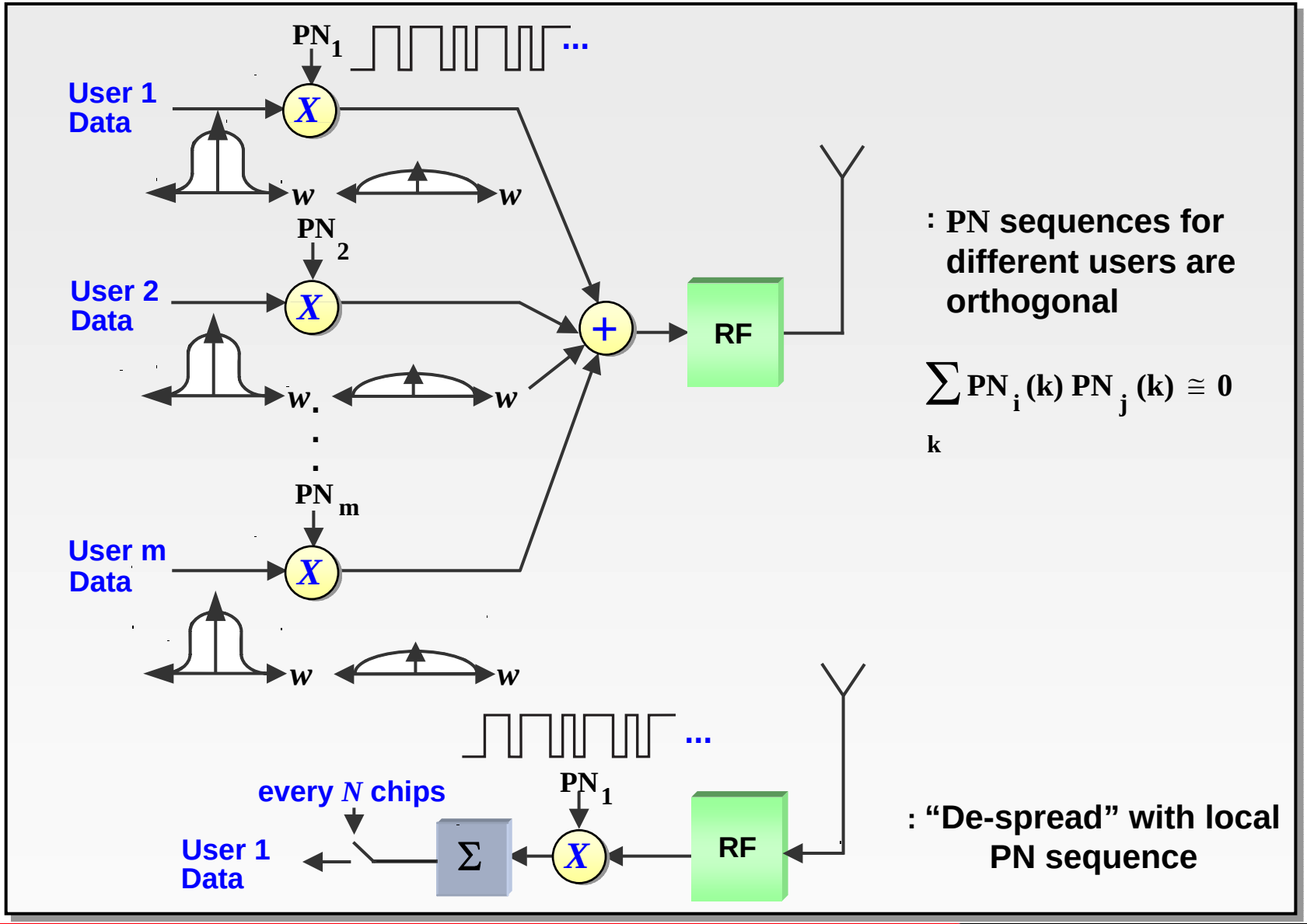
UMTS/W-CDMA Deployment Projections



Spread Spectrum



CDMA

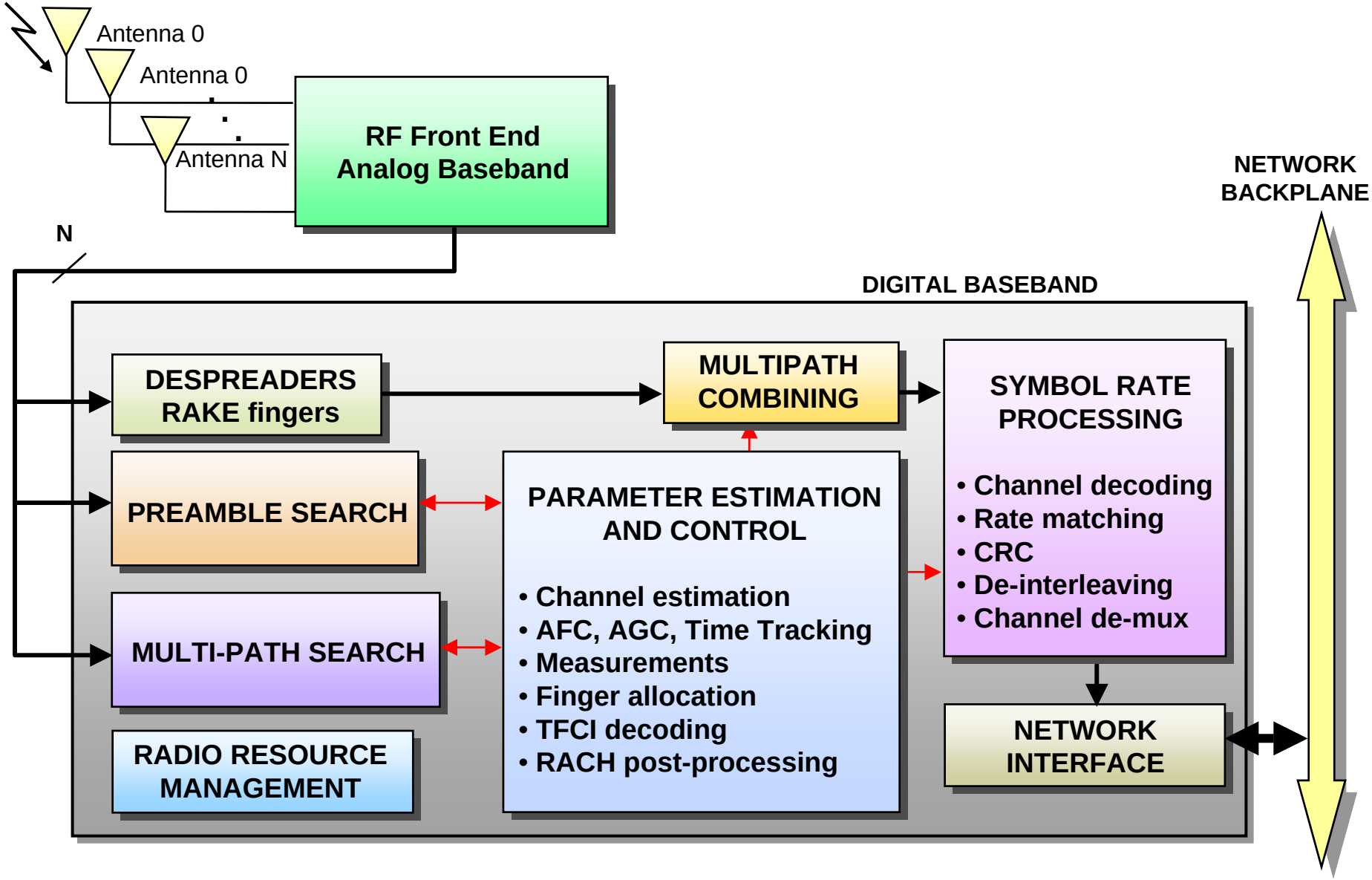


: PN sequences for different users are orthogonal

$$\sum_k PN_i(k)\, PN_j(k) \cong 0$$

: "De-spread" with local PN sequence

Base Station Receiver Functions



Chip-Rate Processing Front-End

De-spreader functions

- Implements Rake “fingers”
- Inner product function:

$$y(k) = \sum_{n=0}^{SF-1} x(k.SF + n) * pn(k.SF + n)$$

Search functions

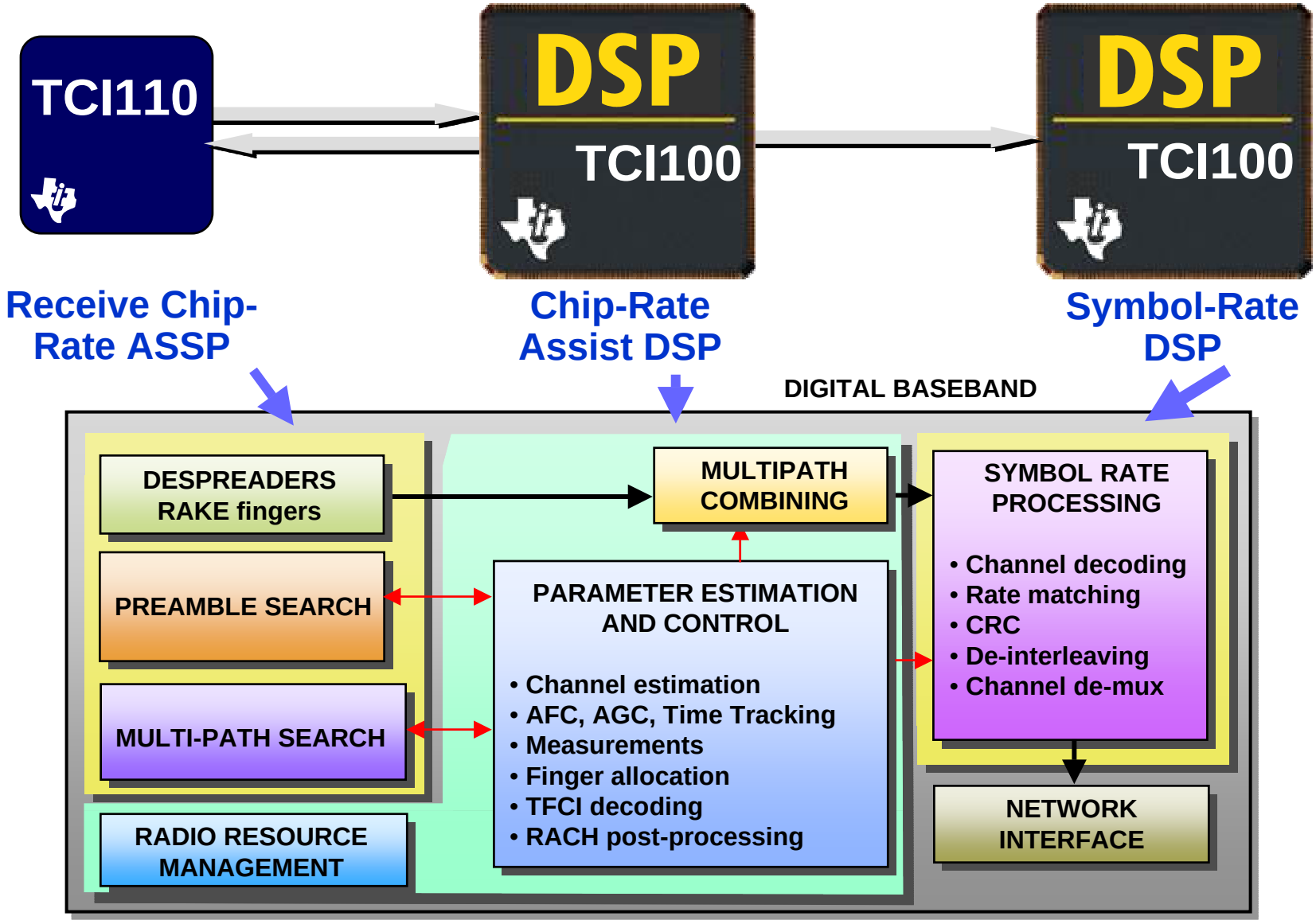
- Path search and Preamble search
- Search for pilot signal within a time window of uncertainty
- Matched filter function:

$$y(k) = \sum_{n=0}^{M-1} x(k - n) * pn(n)$$

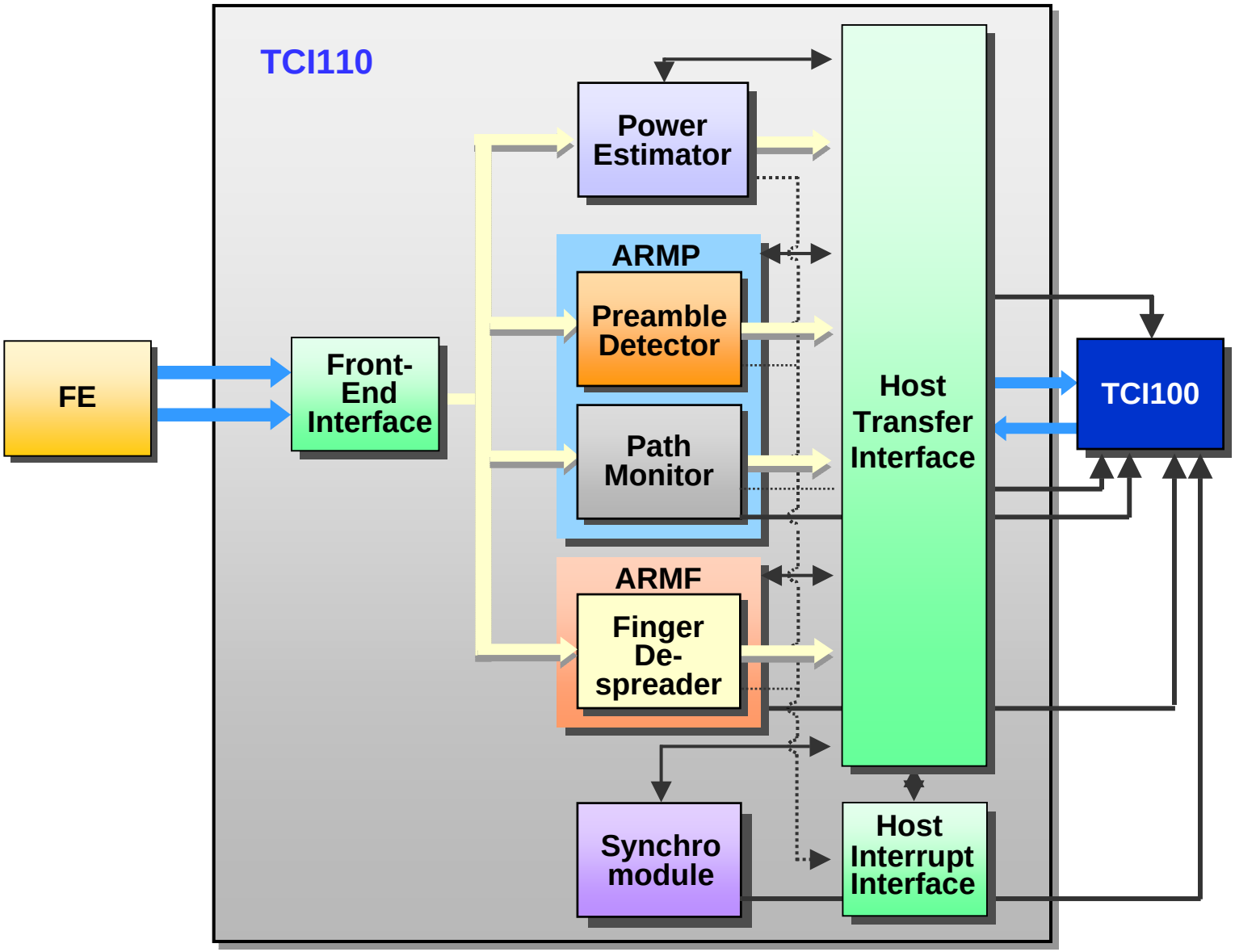
Very high computation rates involved

- > 150 Billion Complex “Multiply Accumulates” per second
- Relatively low processing rate *downstream* of the correlator

System Partition



TCI110 Architecture



Correlator Architecture

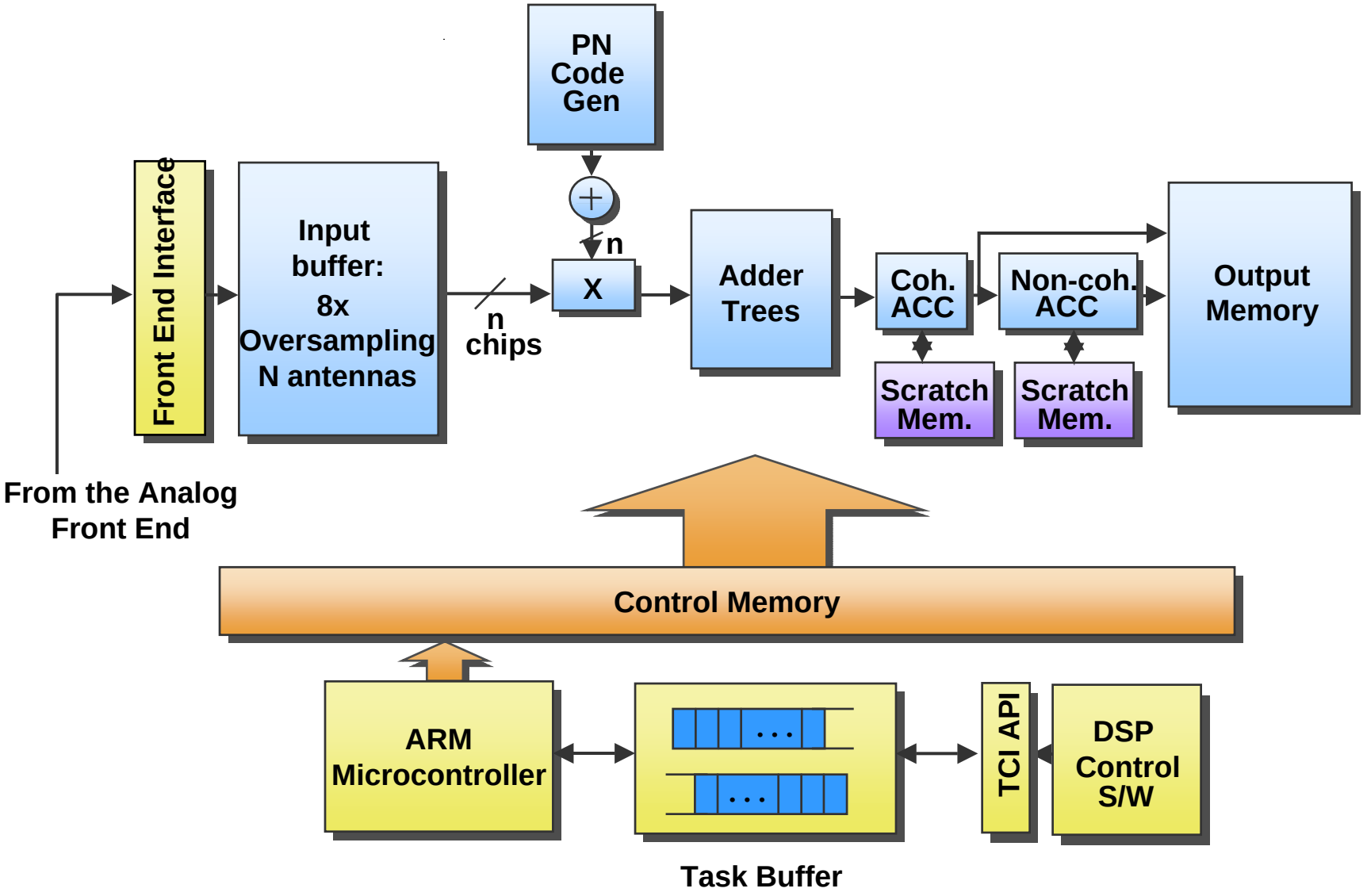
Four task-based accelerators

- Finger de-spreader, Path monitor, Preamble detector, and Power estimator
- Tasks set-up through software running on a programmable DSP
- Results transferred to DSP periodically via DMA

Each accelerator employs a vector-correlator architecture

- Datapath and control customized for specific functions (FD, PM, PD, PE)
- Control includes two ARM micro-controllers
- All tasks mapped to a accelerator run on the same data path in a time-multiplexed manner

Correlator Architecture



Front-End Interface

Function

- Distribute
  - Up to 24 sample streams (including 2 delay streams to FD)
- Interpolate for FD
  - From 8x, or 4x, or 2x samples/chip to 8x samples/chip
- Decimate for other modules
  - From 8x, 4x, 3x samples/chip to 2x for PD and PM and 1x for PE

Typical configurations:

Bus Mode	Oversampling Factor		
	2	4	8
16 bits	12	6	3
32 bits	24	12	6
48 bits	24	12	6

Finger De-Spreader

Performs de-spreading of received multi-path components in a CDMA RAKE receiver

- Data/Control channel despreading
- Includes Early/On-time/Late-time de-spreading with energy accumulation for time tracking
- Flexible allocation of a pool of correlation resources

Usage scenarios:

Finger Despreader		
SF	Fingers	UEs
256	512	64
128	512	64
64	512	64
32	512	64
16	364	45
8	192	24
4	99	12

Finger De-Spreader Usage Examples

- 2048 chip-rate de-spreaders running in parallel
- May be flexibly configured in a number of ways
  - 64 UE at 12.2Kbps, 8 Fingers/UE
    - DPDCH de-spreading
    - DPCCH despreading
    - Early/On-time/Late correlation results on DPCCH for time tracking

    OR
  - 128 UE at 12.2Kbps, 4 Fingers/UE
    - DPDCH de-spreading
    - DPCCH despreading
    - Early/On-time/Late correlation results on DPCCH for time tracking

    OR
  - 51 HSDPA UE, 8 Fingers/UE
    - ADPCH de-spreading
    - HS-DPCCH de-spreading
    - DPCCH despreading
    - Early/On-time/Late correlation results on DPCCH for time tracking

    OR
  - Combinations of the above within the 2048 de-spreader limit

Path Monitor Performance

Performs multi-path search for all received users

- Flexible time-multiplexing of resources among users
- Includes flexible coherent and non-coherent (energy) accumulation

Typical usage:

- 64 Users, Search over 2 antennae in parallel
- 128 chip window (at ½ chip resolution), 1/8th activity factor

Other usage scenarios:

Path Monitor				
Total UEs	Activity Profile			
	UEs	Activity	Search Window	
			Chips	Samples
44	8	1/2	128	2
	4	1/1	128	2
24	16	1/2	128	2
	8	1/1	128	2
12	8	1/1	128	2
	4	1/1	256	2

Preamble Detector Performance

Implements a sliding window correlator for detection of Random Access Channel Preamble

- Flexible coherent and non-coherent accumulation intervals
- Parallel search over all 16 RACH signatures

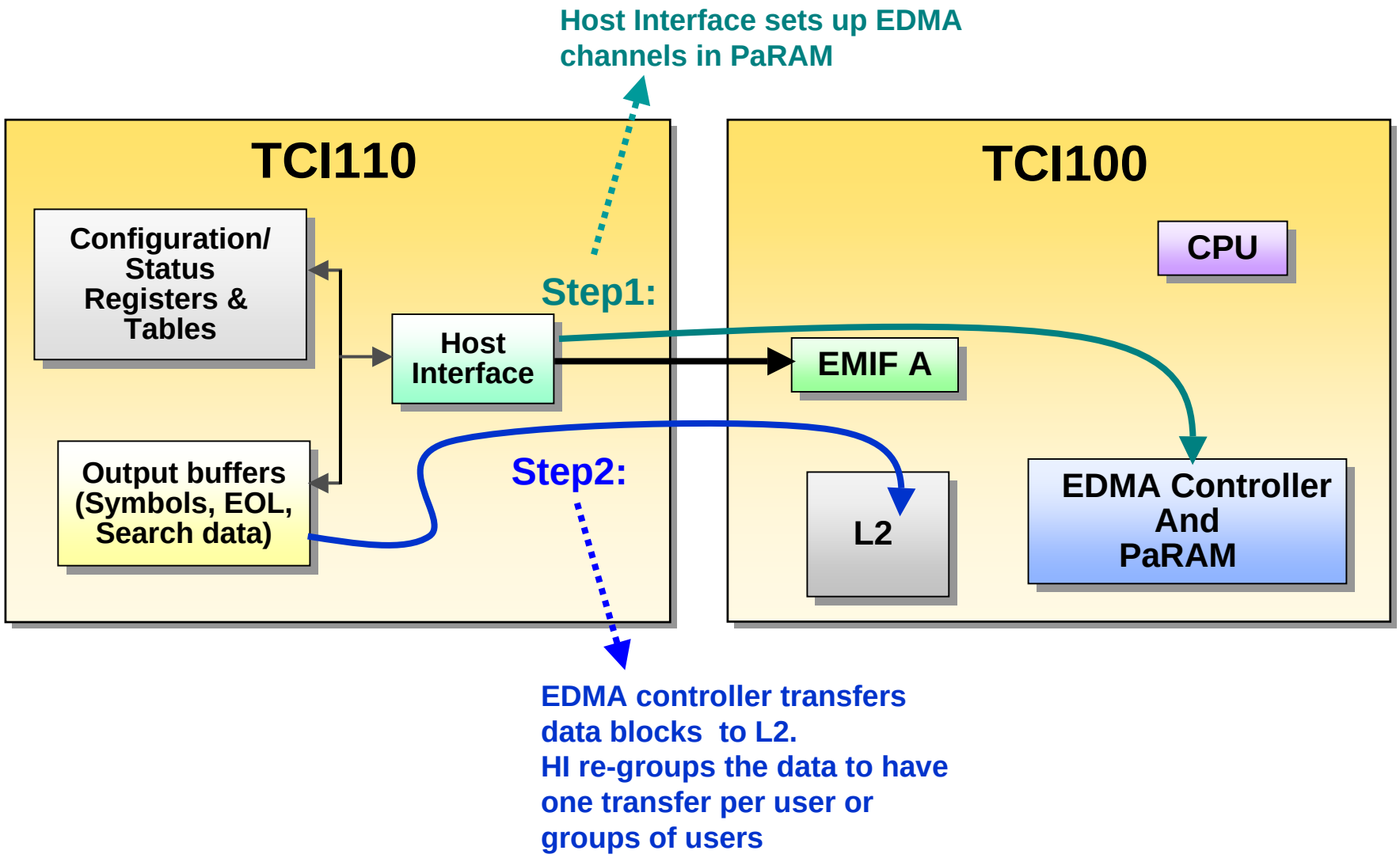
Typical usage

- Correlate over complete preamble (4096 chips)
- 512 chip window, ½ chip resolution (20Km cell radius)
- Search over 2 antennae in parallel

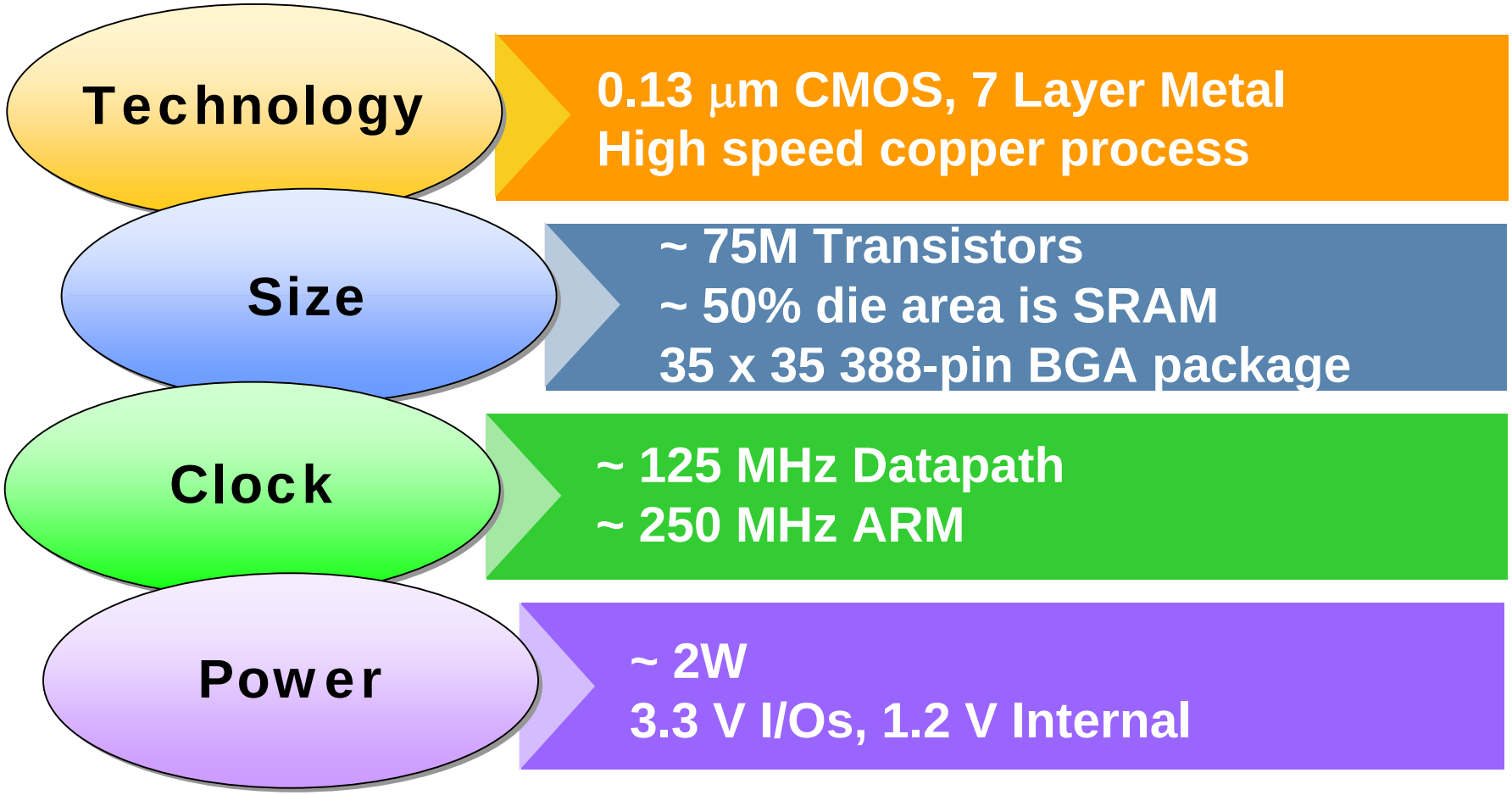
Other usage scenarios:

Preamble Detector				
Scr. Codes	Signatures	Activity	Search Window	
			Chips	Samples
2	16	1/2	1024	2
	16	1/1	512	2
4	16	1/1	512	1
8	16	1/2	256	2

Host Interface



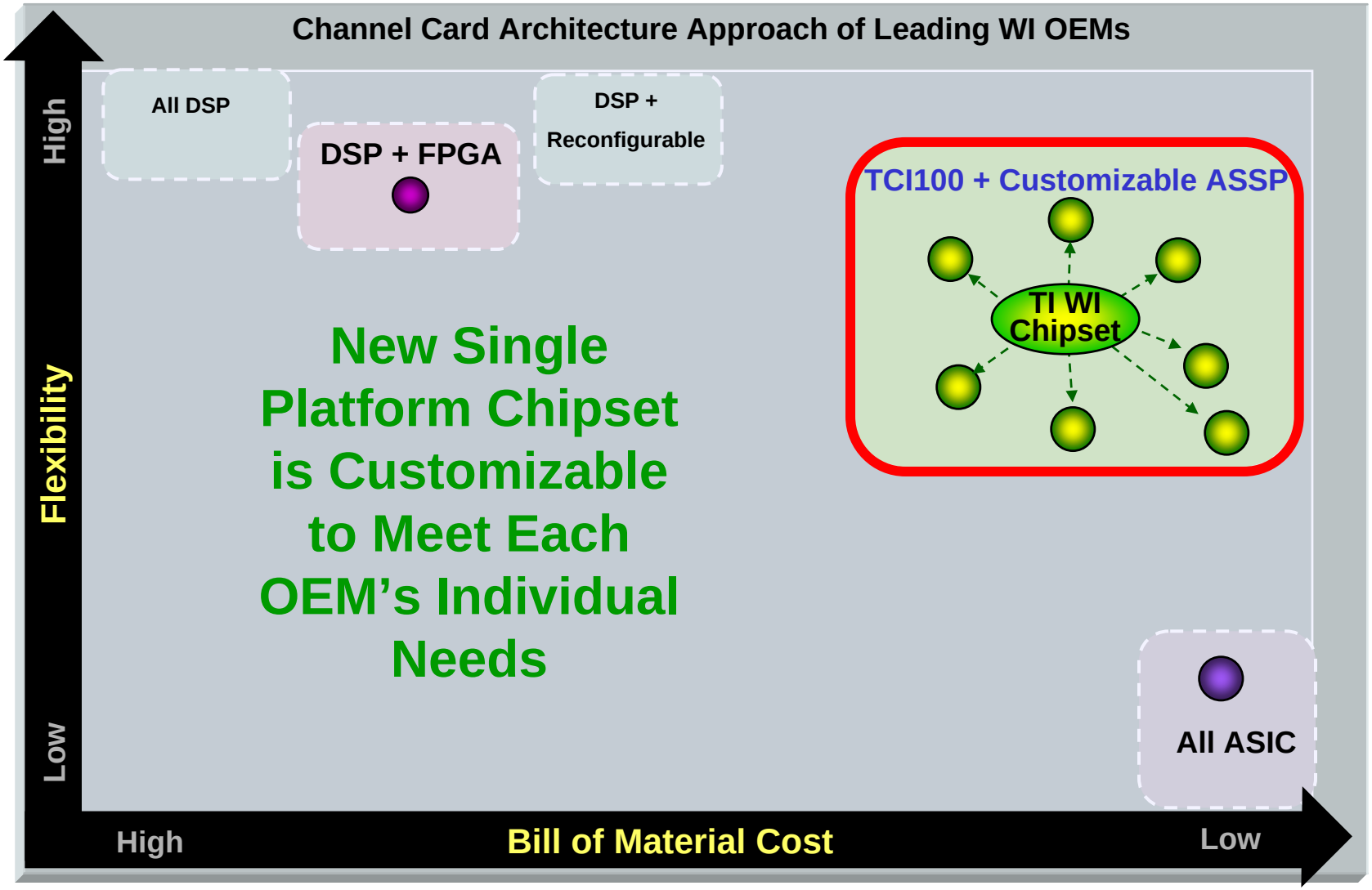
TCI110 Chip Metrics



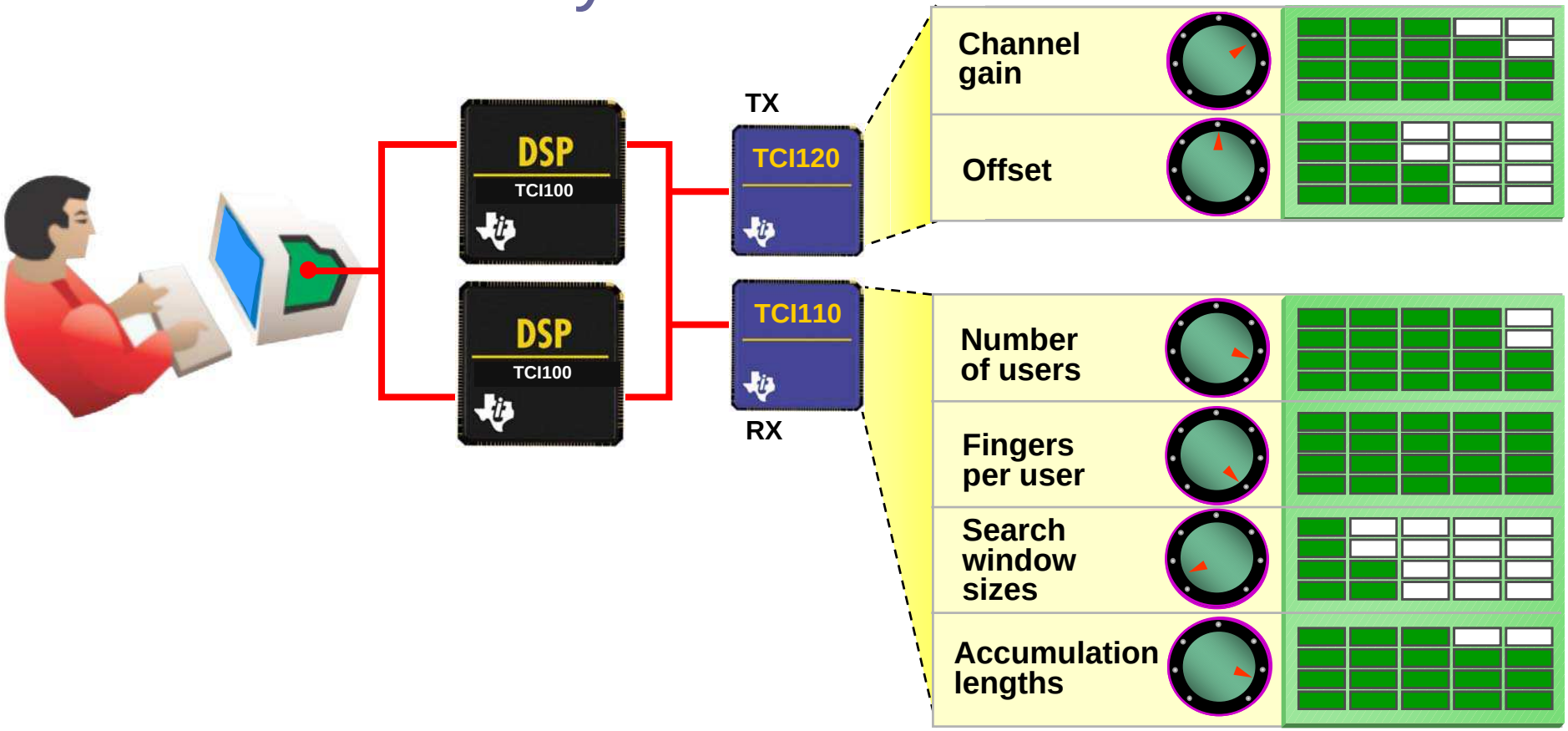
TCI110 Summary

- **Lowest cost per channel enabled via**
  - **Time-multiplexed datapath architecture that allows memory sharing**
  - **Highly integrated SOC**
- **Flexible / Programmable**
  - **“Pool of Resources” concept for flexible resource allocation in a multi-channel context**
  - **Inherently flexible design enhanced with the programmability of embedded cores**
  - **Yet optimized for chip rate applications:**
    - ~ 200 Billion chip operations per second
    - Parallel datapaths for finger de-spreading, path monitoring, preamble detection
    - Dedicated interface and distribution of antenna data
    - Highly optimized transfer of results data to C64x
- **Enhanced time-to-market**
  - **Programmable approach allows bug fixing / feature enhancement in Software**

Flexibility/Cost Combination of DSP + Custom ASIC



Customizable Chipset Maintains OEMs Ability to Differentiate



High-performance, programmable DSP

Flexible hardware configured via registers and commands under DSP software control