VASA: Single-chip MPEG-2 422P@HL CODEC LSI with Multi-chip Configuration for Large Scale Processing beyond HDTV Level

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Outline

- History of MPEG-2 Chips in NTT
- Background and Motivation
- Key Features and Functions
- Main Architecture
- Chip Implementation
- Software Architecture
- Multi-chip Applications
- Summary

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History of MPEG-2 Chips in NTT

Systems

Chips

Portable HDTV Encoder
(ICCE2001)

HDTV Camera Encoder
(NAB2001)

-Various professional systems
-Very small HDTV board/module
-New applications beyond HDTV level

PCI Encoder Board for PC
(Globecom95)

Encoding PC card
(ICCE2000)

Multi-chip HDTV

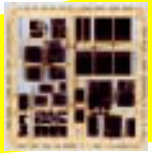
High quality

High compression

Low delay

Single-chip HDTV

Multi-chip configuration



SuperENC-II(‘00)

VASA (′02)
(Hot Chips 14)

SuperENC (‘98)
(Hot Chips 10)

Enc-C,Enc-M (‘95)
(Hot Chips 7)

VASA:
Versatile Advanced
Signal processing Architecture

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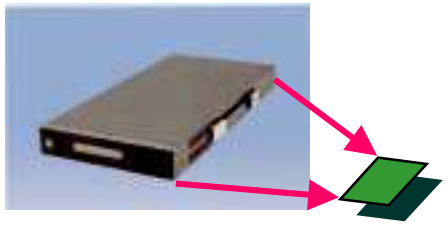
Background and Motivation

- Global wave of digitization in TV broadcasting.
  - Terrestrial digital broadcasting will start in Japan in 2003. Producing programs and exchanging them over broadband digital network will boost their circulation.
- Professional and compact HDTV CODEC systems.
  - 1U half-rack -> *Very small board/module*
  - 9-chip HDTV -> ***Single-chip HDTV***
- Requirements:
  - *Small space & low power consumption*
  - *New applications beyond HDTV level*



- ***VASA: New Single-chip MPEG-2 422P@HL CODEC LSI with Multi-chip Configuration***

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Key Features and Functions

- Single-chip Applications:
  - Traditional and advanced high quality CODEC (encoding/decoding),
  - Pre-processing for extracting picture characteristics
  - Watermarking for digital content protection
- Multi-chip Applications:
  - Large scale processing beyond HDTV level for digital cinema and multi-angled live TV
  - Multi-view profile for stereo image CODEC
  - Multi-channel CODEC with TS multiplexing and de-multiplexing

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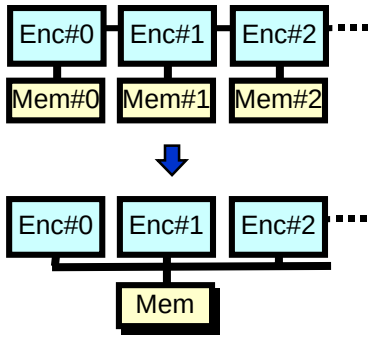
Main Architecture (Approach)

- Re-modeling of "Parallel Encoding"
  - Previous: Individual address spaces model
  - Current: Unique address space model



- Control and data hierarchy
  - Macroblock pipeline schemes in each parallel encoding core (intra-core) and inter-core (intra-chip: top)
  - Two level memory hierarchy for intra- and inter-core

- HFCA: Hierarchical Flexible Comm. Architecture
  - Dual hierarchical backbones linked to every module
    - ***Small*** control information: *CPU-BUS*
    - ***Huge*** picture data information: *System-BUS*

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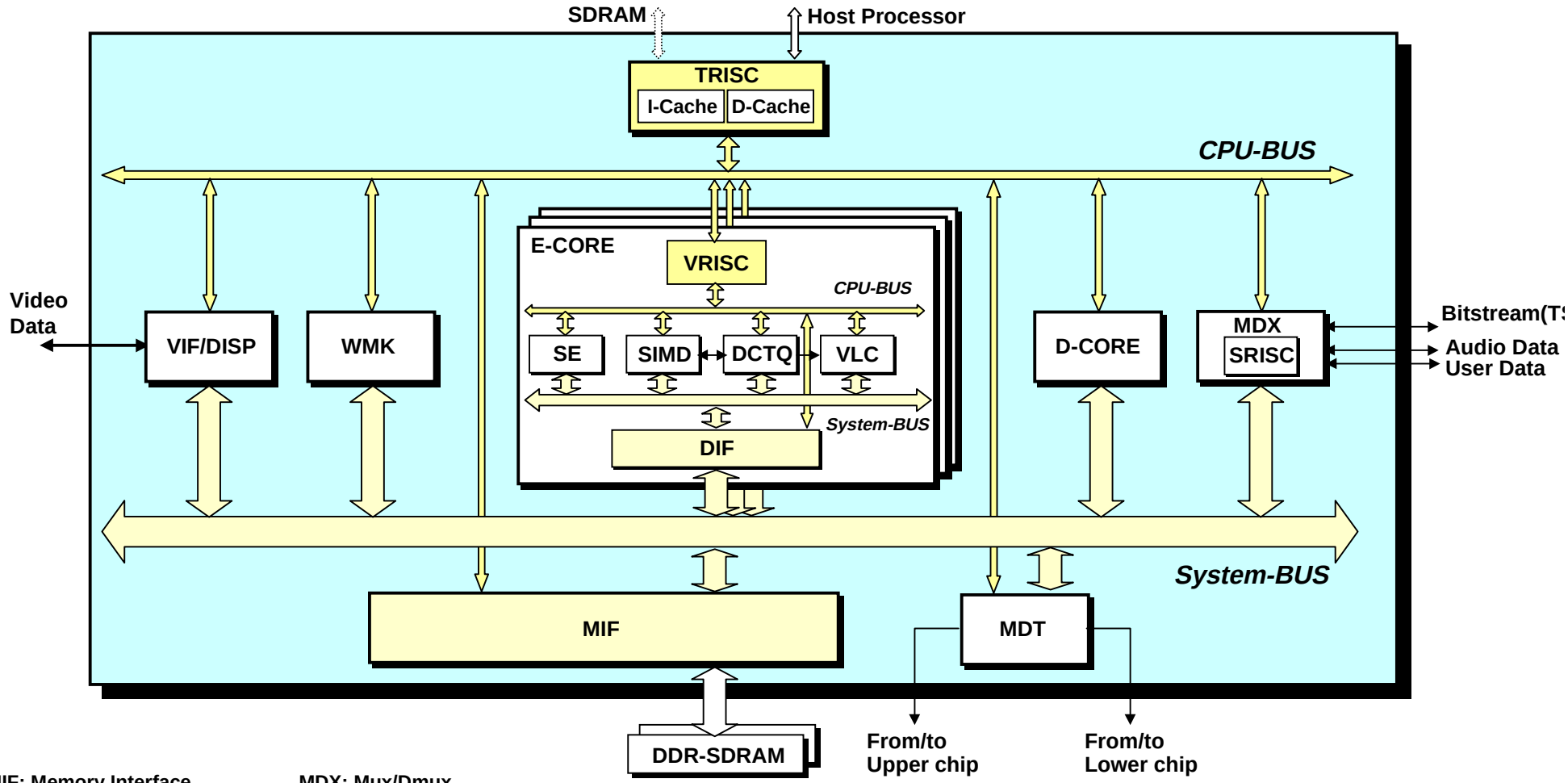
Main Architecture (Block Diagram)



MIF: Memory Interface
MDT: Multi-chip Data Transfer
D-CORE: Decoder Core

MDX: Mux/Dmux
VIF/DISP: Video Interface/Display
WMK: Watermark

E-CORE: Encoder Core
SE: Search Engine
SIMD: SIMD Processor

DCTQ: DCT&Q & inverse ones
VLC: Variable Length Coding
DIF: Data Interface

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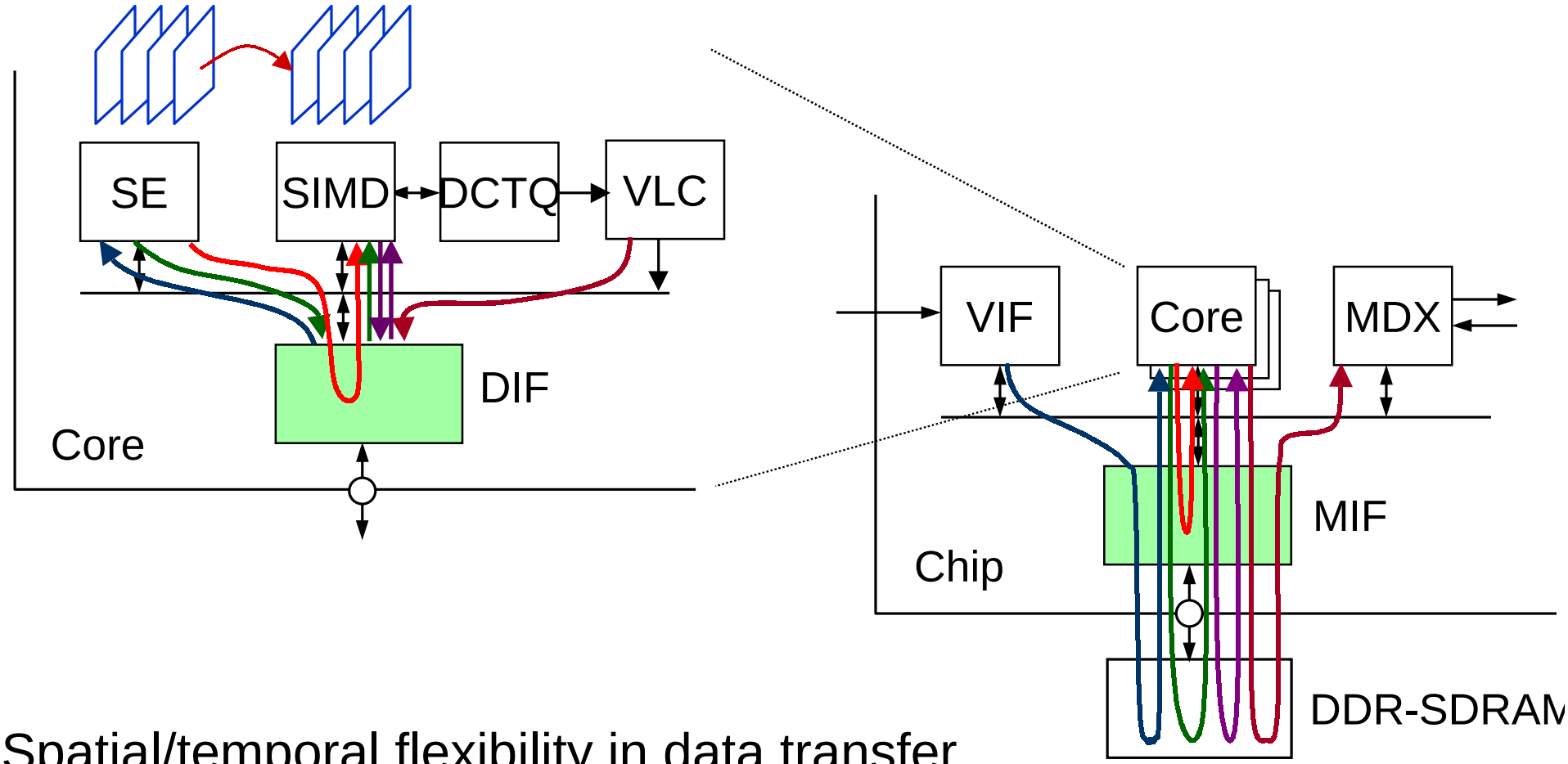
Main Architecture (Intra-core/Intra-chip Comm.)



- Spatial/temporal flexibility in data transfer via software on ***DIF*** in each core and on ***MIF*** in a chip

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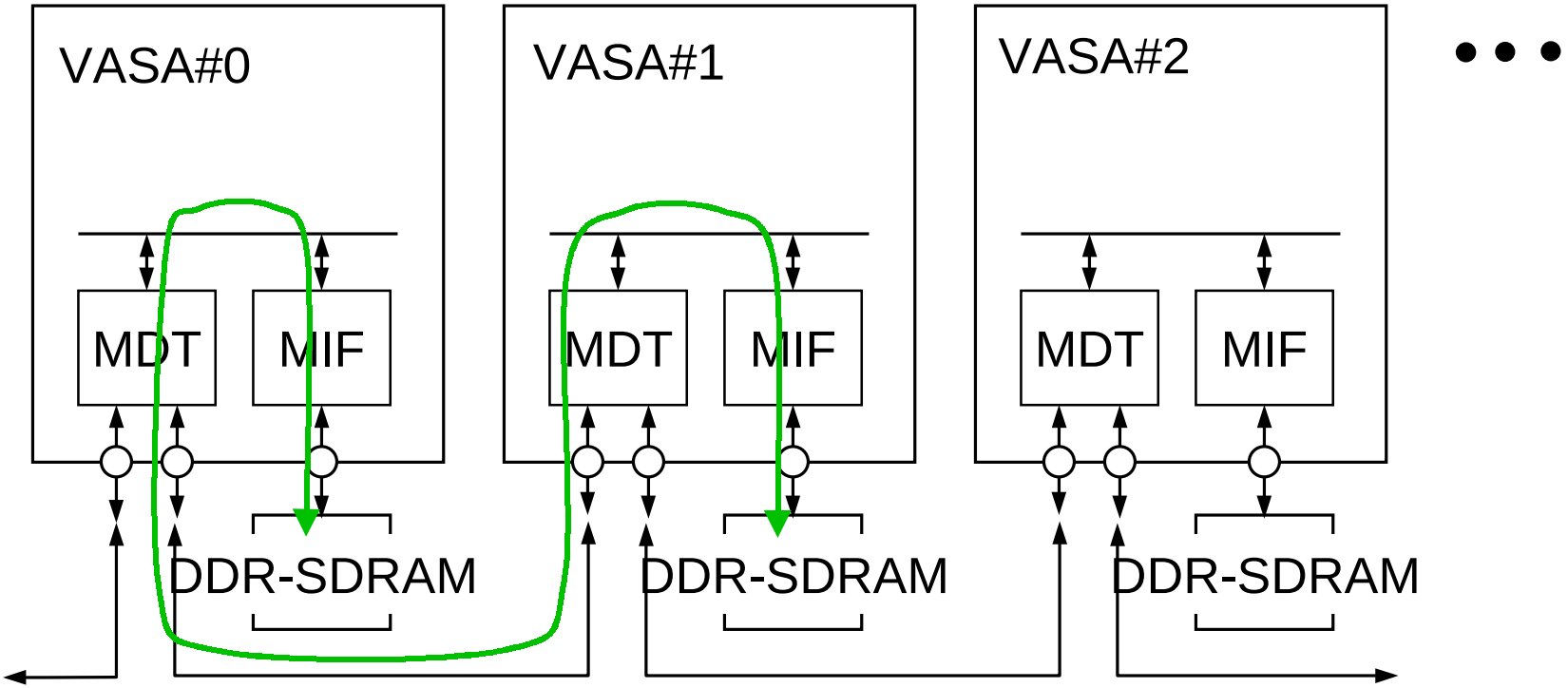
Main Architecture (Inter-chip Communication)



- Multi-chip configuration (scalability) for large scale processing beyond HDTV level

Main Architecture (Summary)

- HFCA (*with MIF & DIF*) Feature and Functions:
  - Space and time switching:

    Data transfer between each chip, core, module, and sub-module *immediately* or *after a certain time interval* in the same manner.
  - Hierarchical structures:
    - CPU-BUS: TRISC + VRISC x 3
    - System-BUS: MIF + DIF x 3
  - Controlling DDR-SDRAM and optimizing its active bandwidth
    - Ordinal encoding: 70% (average ratio)
    - Advanced encoding: 85% (average ratio)

- HFCA provides sufficient *performance* and *flexibility* for recent high quality CODEC technologies.

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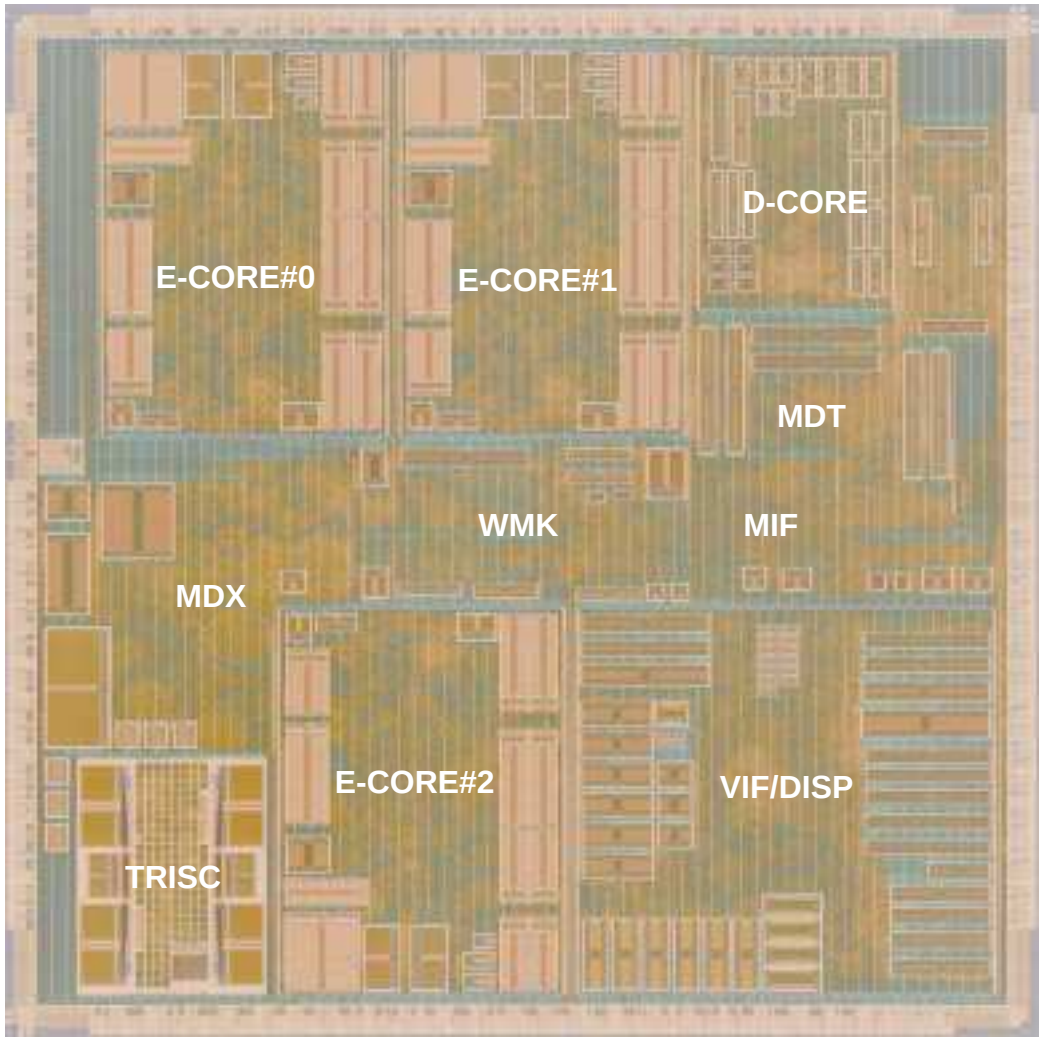
Photograph of VASA



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VASA Physical Features

Technology	**0.13-μm 8-level metal CMOS**
Number of transistors	**61.4 million**
Die size	**14.0 mm x 14.0 mm**
Clock frequency	**200-MHz**
Supply voltage	**Core: 1.5V / I/O:3.3V / DDR: 2.5V**
Power consumption	**3.0 W (at 1080I 422P@HL)**
Package	**1008-pin FCBGA (35 mm x 35 mm)**
External memories	**256Mbit (32-bit) 200MHz DDR-SDRAM x2 (for images) and 32Mbit (16-bit) 100MHz SDRAM x1 (for TRISC large firmware, *if necessary*)**

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VASA Functional Features

Video:	Profile and level	MPEG-2 {422P,MP}@HL, {422P,MP}@H-14,{422P,MP,SP}@M
	Search range	narrow: -225.5/+211.5 (H), -113.5/+125.5 (V) wide: -449.5/+435.5 (H), -128.0/+127.5 (V)
	Resolution & rate	single-chip: 1920/1440 x 1080 at up to 30 frames per second : 1280 x 720 at up to 60 frames per second multi-chip: Max. 4096 x 2048 up to 60 frames per second
	Pre-processing	Macro block based sophisticated functional filter
	Multi-view profile	Stereo image CODEC
	Watermark	Original watermark insertion/extraction
Audio:	I/O format	Liner PCM or encoded stream (AAC)
User:	I/O format	PES format for timecode and other audio and data
ystem:	I/O format & bitrate	MPEG-2 TS (188/204 bytes) Max. 300 Mbps
	Multi-channel CODEC	Encoding/decoding by TS multiplexing/de-multiplexing

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Evaluation and Validation

- Before fabrication,

  HW/SW were carefully evaluated and validated using VCS and ASIC emulator through small- and/or full-size images.

- After fabrication,

  HW/SW were evaluated and validated using VASA CODEC evaluation boards.

- The first silicon is *successfully* implemented with complete software.

VASA chip

VASA module

Evaluation board

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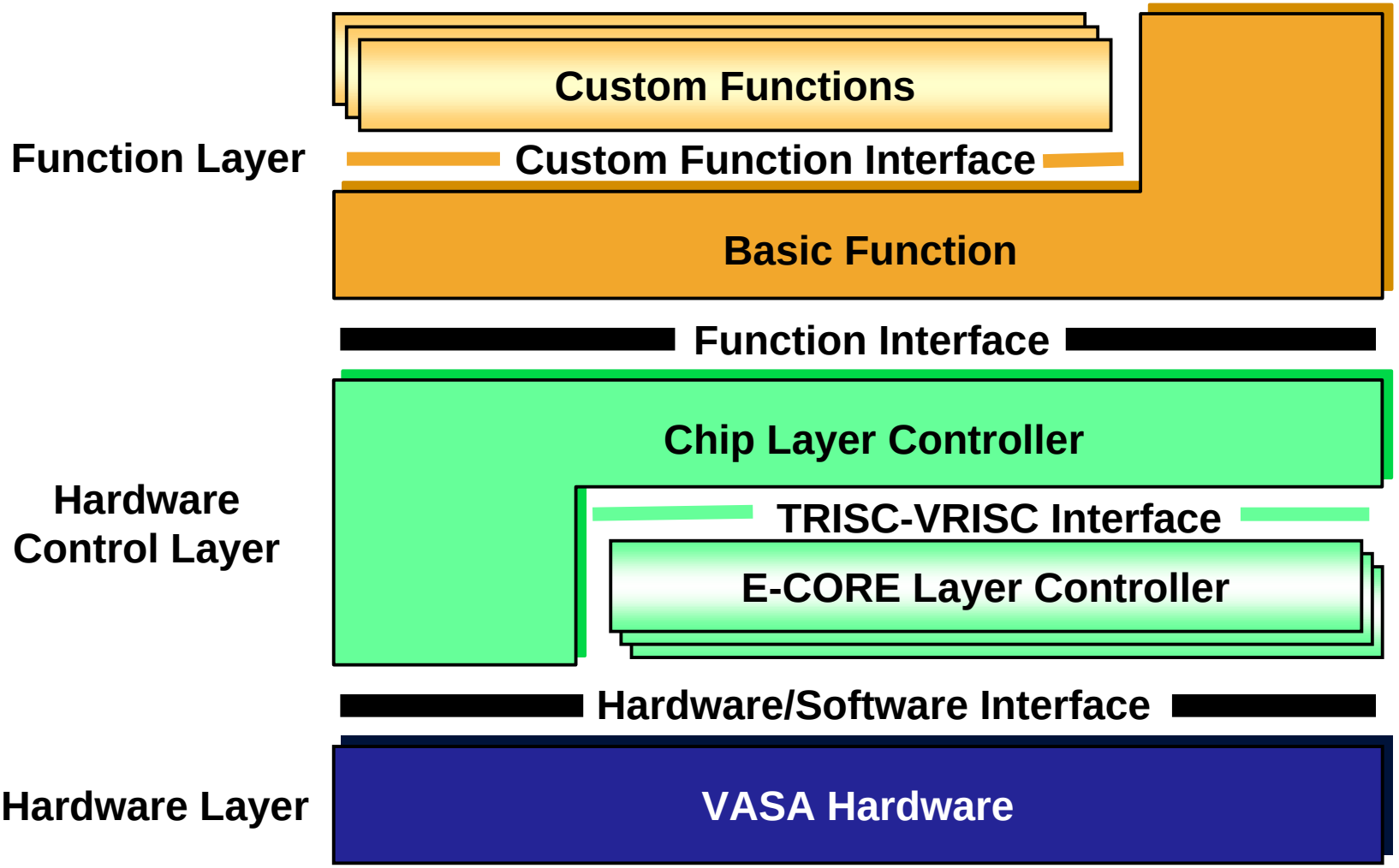
VASA Software Architecture



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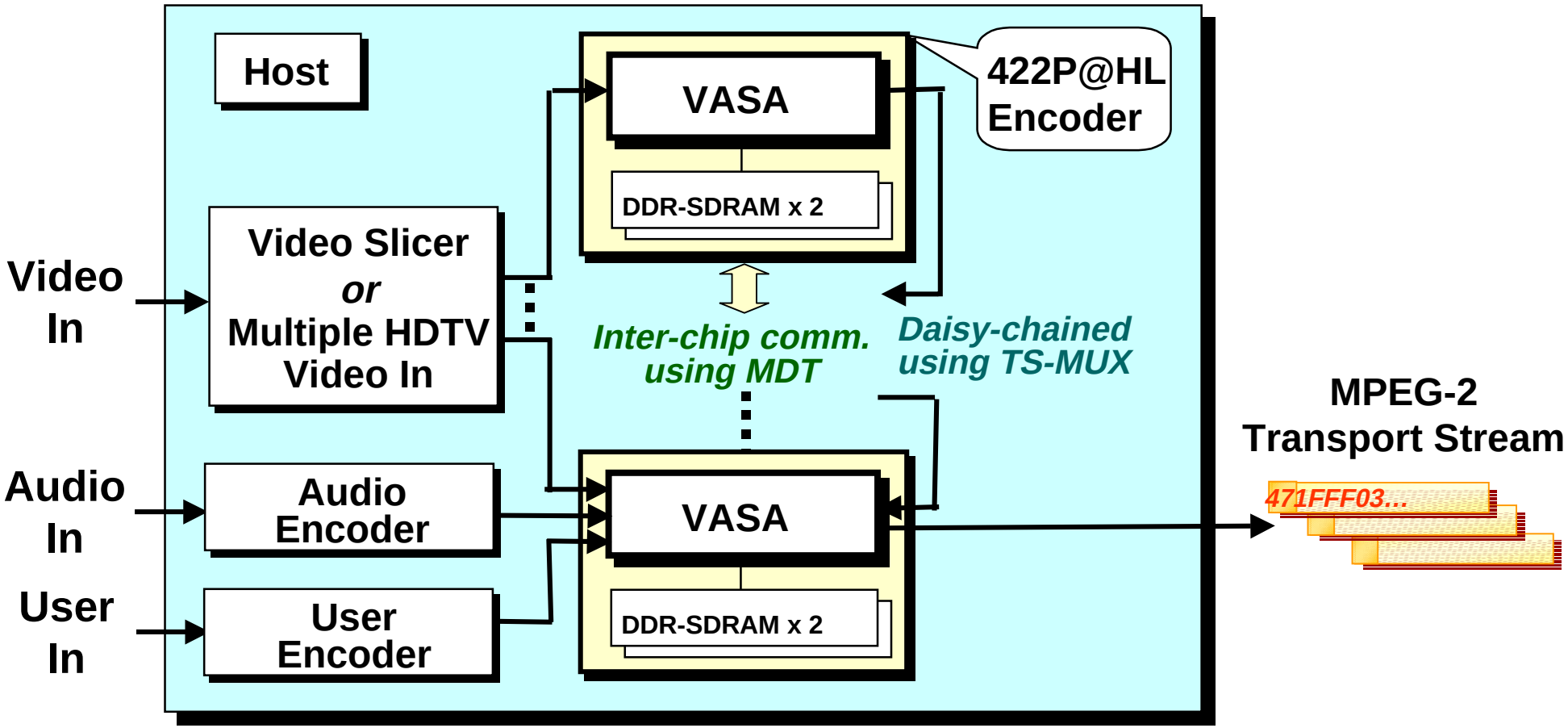
Multi-chip System Configuration



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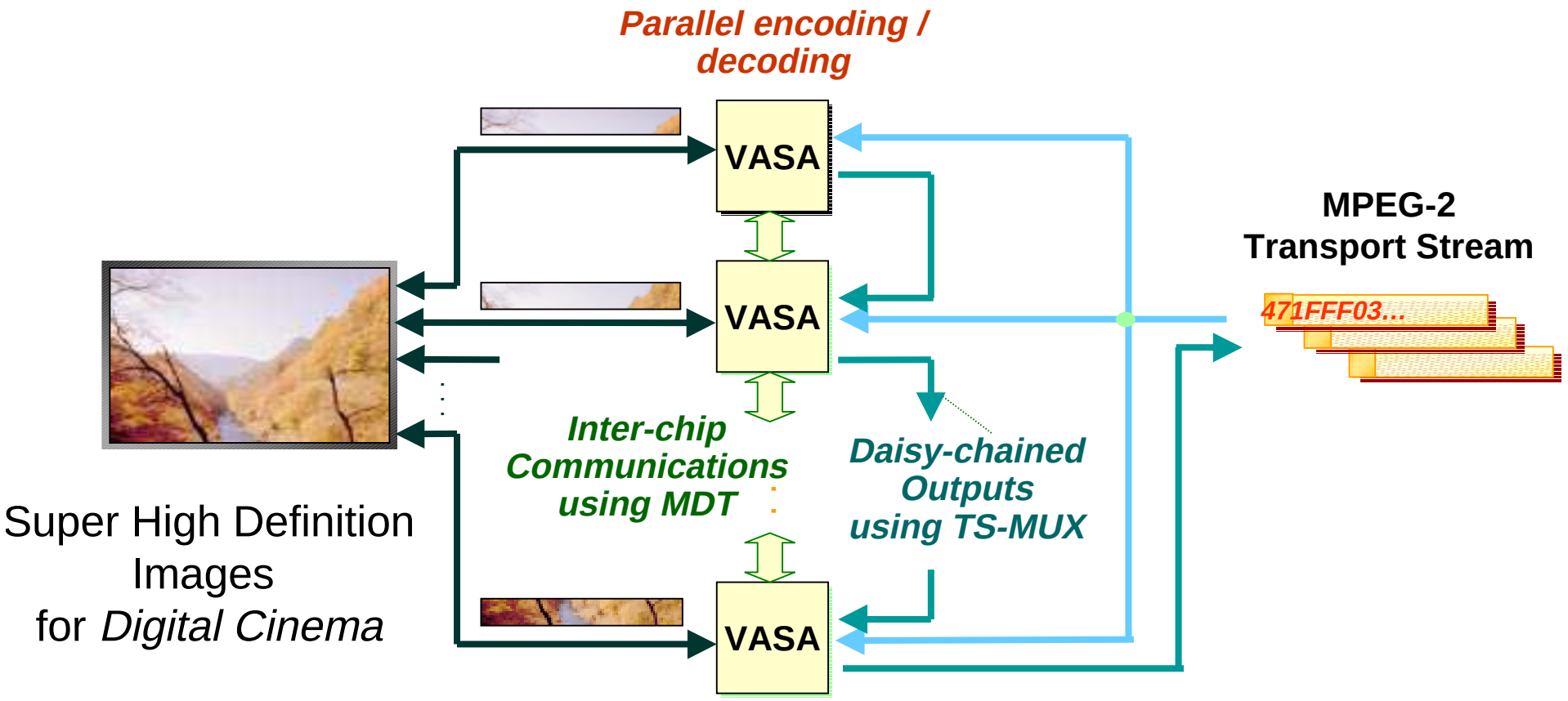
Multi-chip Applications (1)



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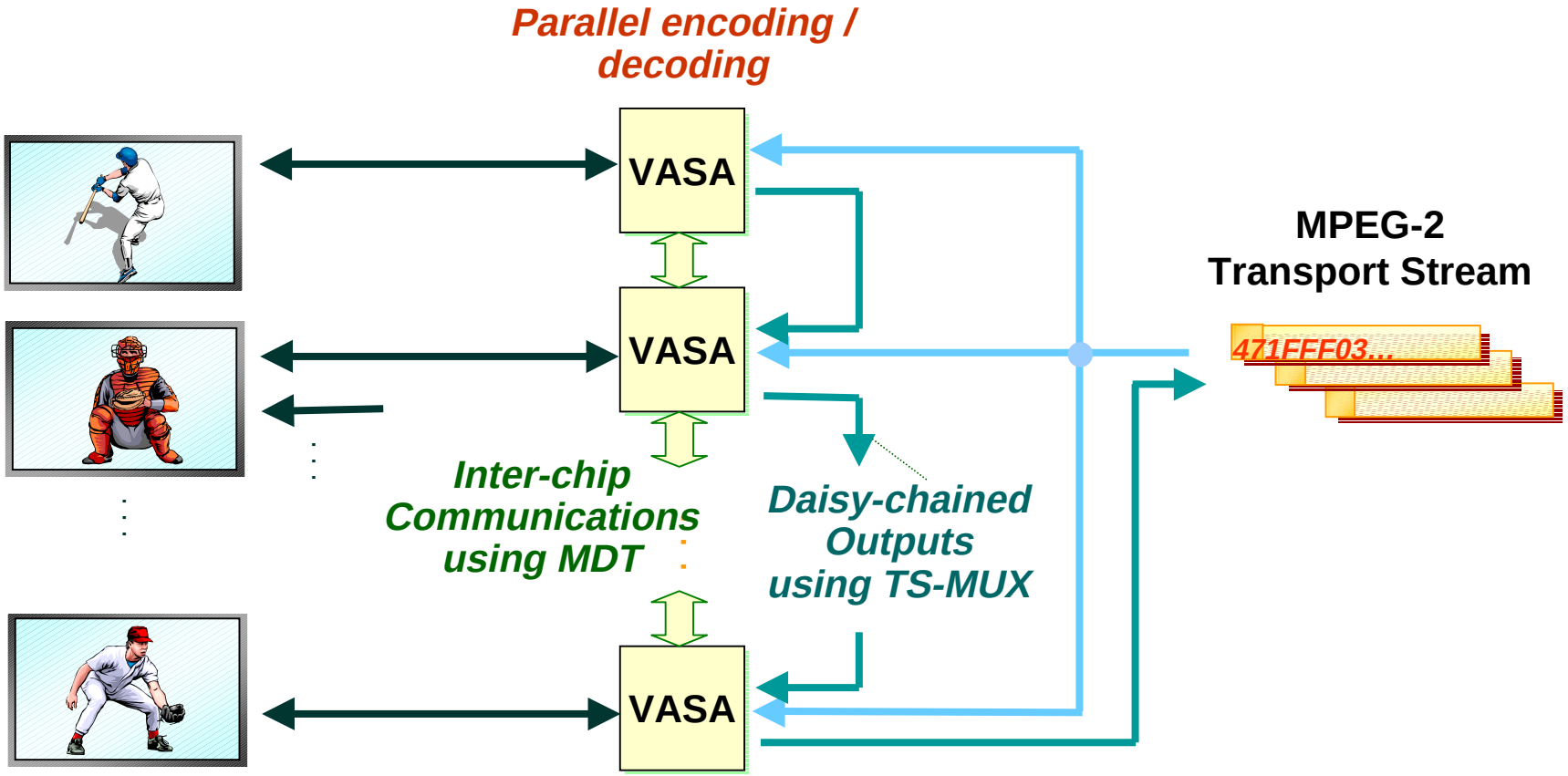
Multi-chip Applications (2)



Multiple HDTV images
for *Multi-view/-angled TV*

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Summary

- Background and Motivation
- VASA Main Architecture
  - Hierarchical Flexible Comm. Architecture
  - Intra-core/-chip & Inter-chip Comm.
- VASA Implementation
  - Chip Specifications
  - Physical & Functional Features
- VASA Software Architecture
- Multi-chip Applications beyond HDTV Level

➡ ***VASA*** is a ***key LSI*** for implementing various professional MPEG-2 applications in near future.

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