Au1X00

Video decode for less than 1W

Agenda

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- Demonstration

- Three main topics:

    - **The Au1100™ Processor (and family)**

    - **Video performance in Au1X00 systems**
        - **System performance issues in embedded systems**
        - **Video performance on Au1X00 systems**

    - **Power dissipation while displaying video**

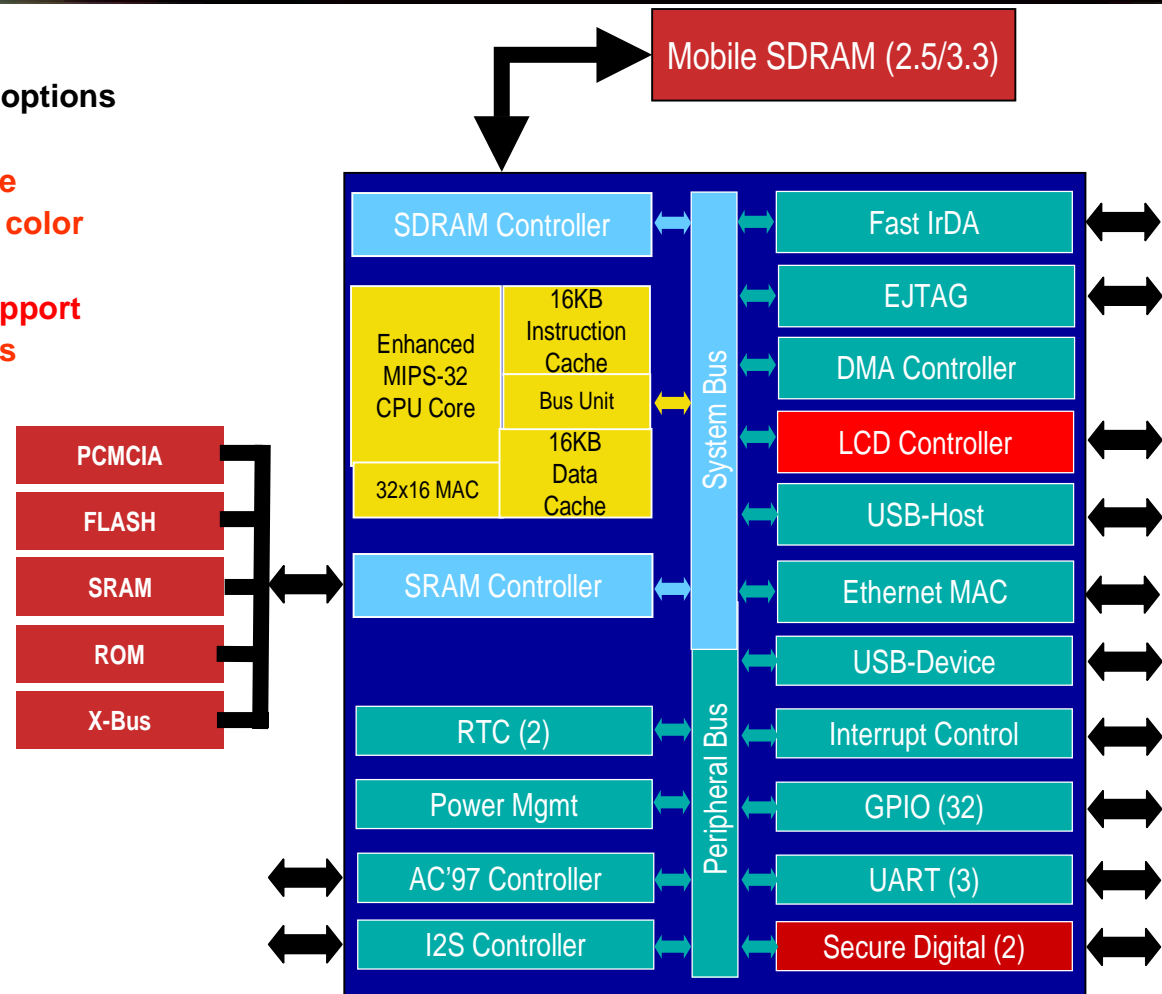- Summary and conclusions

Video demonstration

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- **What you just saw:**
  - MI-2 movie trailer
  - Encoded at:
    - MPEG1 encode
    - 400 x 200 window size
    - 1100 kbps bit rate
    - 24 Frames per Second
  - Playback setup
    - MediaPlayer™ video player
    - WindowsCE™ OS
  - Played on
    - Pb1100 development platform
    - Au1100
      - 0.13um
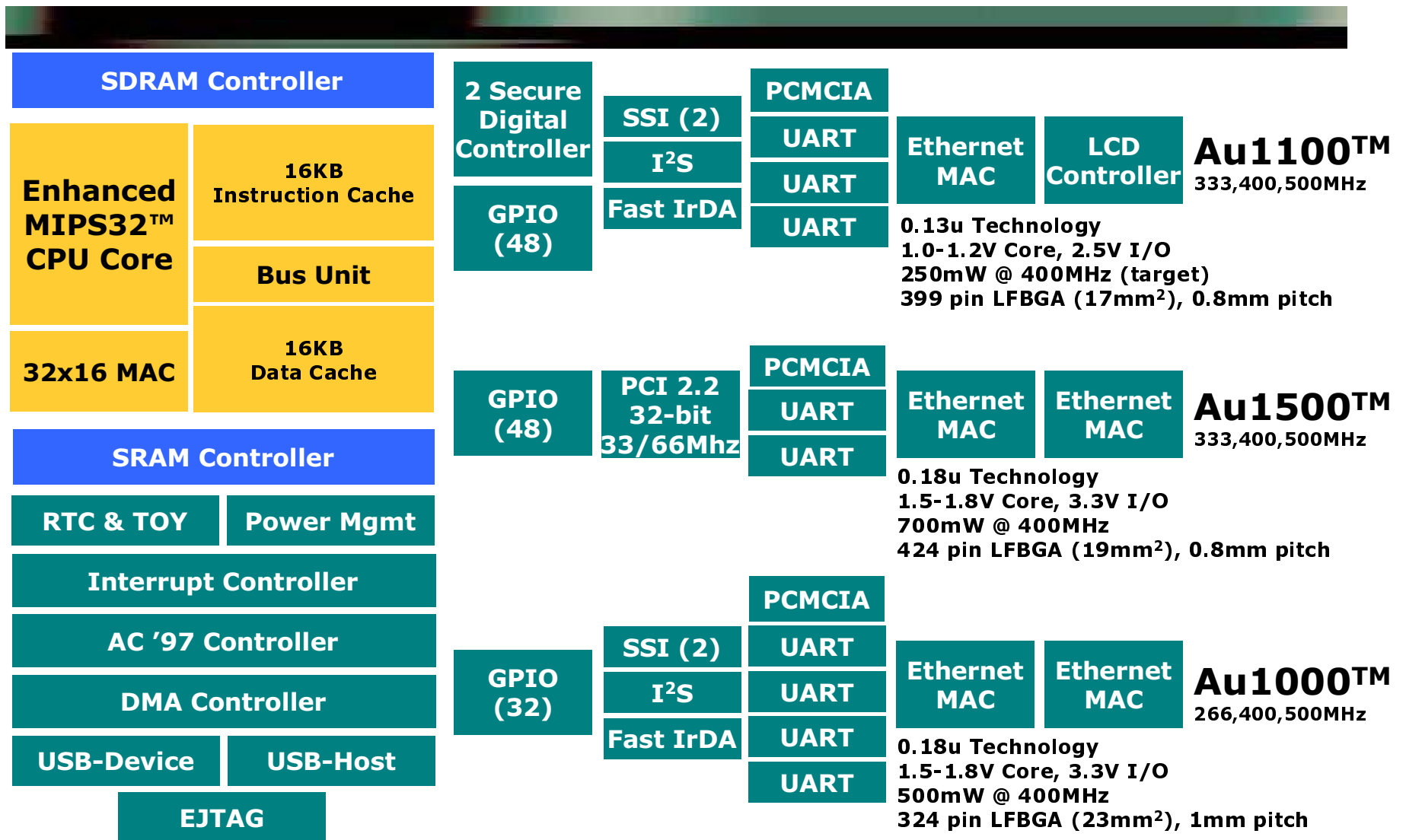   - 396MHz
      - <<500mW power

Au1100™ Processor
The first 0.13um AMD SOC

AMD

- **Alchemy Au1 Core**
  - **333, 400, and 500 MHz core options**
- **LCD Controller**
  - **Unified Memory Architecture**
  - **All panel types, up to 16-bit color**
  - **Hardware rotate (QVGA)**
- **2.5 Volt/3.3Volt Mobile SDRAM Support**
- **2 x Secure Digital / SDIO Interfaces**
- **Ethernet MAC**
- **3 UARTs**
- **USB Host and Device**
- **Fast IrDA**
- **GPIO (TBD)**
- **AC'97**
- **I2S**
- **TSMC 0.13μ Process**
- **Low Power Consumption**
  - **1.0 - 1.2V Core**
  - **3.3 V I/O**
  - **250mW @ 400MHz**
- **Package**
  - **399 Pin PBGA, 17 x 17 mm2**

Mobile SDRAM (2.5/3.3)

SDRAM Controller

Enhanced MIPS-32 CPU Core
16KB Instruction Cache
Bus Unit
32x16 MAC
16KB Data Cache

SRAM Controller

PCMCIA
FLASH
SRAM
ROM
X-Bus

RTC (2)
Power Mgmt
AC'97 Controller
I2S Controller

System Bus
Peripheral Bus

Fast IrDA
EJTAG
DMA Controller
LCD Controller
USB-Host
Ethernet MAC
USB-Device
Interrupt Control
GPIO (32)
UART (3)
Secure Digital (2)

Au1X00 SOC comparison

AMD

SDRAM Controller					

Enhanced MIPS32™ CPU Core

16KB Instruction Cache

Bus Unit

32x16 MAC

16KB Data Cache

SRAM Controller

RTC & TOY | **Power Mgmt**

Interrupt Controller

AC '97 Controller

DMA Controller

USB-Device | **USB-Host**

EJTAG

2 Secure Digital Controller

SSI (2)

I²S

Fast IrDA

GPIO (48)

PCMCIA

UART

UART

UART

Ethernet MAC

LCD Controller

Au1100™
333,400,500MHz

0.13u Technology
1.0-1.2V Core, 2.5V I/O
250mW @ 400MHz (target)
399 pin LFBGA (17mm²), 0.8mm pitch

GPIO (48)

PCI 2.2 32-bit 33/66Mhz

PCMCIA

UART

UART

Ethernet MAC

Ethernet MAC

Au1500™
333,400,500MHz

0.18u Technology
1.5-1.8V Core, 3.3V I/O
700mW @ 400MHz
424 pin LFBGA (19mm²), 0.8mm pitch

GPIO (32)

SSI (2)

I²S

Fast IrDA

PCMCIA

UART

UART

UART

UART

Ethernet MAC

Ethernet MAC

Au1000™
266,400,500MHz

0.18u Technology
1.5-1.8V Core, 3.3V I/O
500mW @ 400MHz
324 pin LFBGA (23mm²), 1mm pitch

System-level Video Performance Issues

AMD

- Computation requirements of video decode (MPEG4/1)

- Memory system bandwidth utilization

- Performance/overhead of networking solution

- Integration/synchronization of audio and video outputs

- Can video decode be done in software on a <1W power budget?

Computational Components of Video Decode

- We studied 2 of the dominant components in MPEG4 video decode
  - Inverse Discrete Cosine Transform: up to 40%
  - Color Space Conversion: up to 25%

- Performance measured by two benchmark tests
  - IDCT loop: 81000 block transforms
  - CSC loop: 81000 YCbCr->RGB 8x8 block conversions
  - Results should be dominated by CPU, not memory system.

Projected Decode Performance

AMD

- Performance measurements/projections
  - Projected frames per second (FPS) are approximate

	CPU Cycles per CSC	CPU Cycles per IDCT	Projected FPS, 320x240, 504MHz
Au1500	~5050	~2675	26

- Benchmark measurements project full frame rate decode

System Performance Issues
Bus/Memory Bandwidth Utilization

AMD

- Bandwidth to/from frame buffer is valuable resource
  - Unified/Split memory architectures have very different performance characteristics

- There may be many consumers of bandwidth
  - Ethernet, video decode, frame buffer updates, audio, GUI overhead, USB mouse/keyboard input
  - Bus arbitration fairness may be an issue for satisfying real-time requirements of video display
    - The AuSB protocol supports shifting bandwidth allocation towards high-priority consumers.

Au1X00 Video Solution Bandwidths

- The effective bandwidth to the frame buffer varies widely depending on the video solution.

- Au1000™ Processor:
  - Glueless interface to inexpensive, low-power Epson controllers
    - 16-bit, 25-50MHz interface

- Au1500™ Processor:
  - Any PCI-based graphics solution
  - Example: ATI Xpert 98
    - 33MHz, 32-bit PCI interface

- Au1100™ Processor:
  - Integrated LCD controller
  - Full speed read/write access to SDRAM based frame buffer

Video Display System Bus Bandwidth Requirements

AMD

- For video decode, bandwidth usage will be dependent on the frame buffer update rate.
  - For example: at 30FPS, 16-bit color the bus bandwidth required is:

	FB write (MB/s)
QCIF (176x144)	1.5
SIF (320x240)	4.6
CIF (352x288)	6.1

- The complete decode operation will use 1.5-3X this much memory bandwidth depending on the details of the encoding scheme used.

- Available Au1X000 FB bandwidth:
  - Au1000™: good for lower end of the performance range
  - Au1500™ and Au1100™: cover full spectrum of decode performance

Memory System Impact

AMD

- Memory system dependence
  - The CPU-dominated benchmarks show a second-order dependence on the memory system.

	CPU Cycles per CSC	CPU Cycles per IDCT
Au1500, 396MHz, PCI graphics	~5050	~2675
Au1100, 396MHz, QVGA panel	~5500	~2850
Au1100, 396MHz, VGA panel	~5975	~3150

Video Display System Bus Bandwidth

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- With a UMA display controller like the Au1100, a dominant bandwidth consumer is screen refresh.
  - Screen refresh accesses frame buffer at full SDRAM rate

	Refresh BW (MB/s)	% of AuSB BW w/ 100MHz SDRAM @ typical access rate
QVGA (320x240)	11.7	5.6
VGA (640x480)	46.9	22.3
SVGA (800x600)	73.2	34.8
XGA (1024x768)	120.0	57.0

Power Management

AMD

- The Au1X00 systems are very capable of supporting quality video decode solutions – what about power?

- The keys to power dissipation
  - Managing power in both Active and Idle processor states
  - Leveraging technological developments
  - High frequency operation allows more time spent in Idle

Au1X00: Managing Power

AMD

- Au1X00 family is designed for low-power operation
  - Custom circuit design allows high-speed operation at low voltage
  - Very aggressive use of clock gating

- At the system level the Au1X00 solutions allow:
  - Multiple frequency scaling options
    - Support for static, semi-static and dynamic frequency changes.
  - Dynamic Voltage scaling
    - Power supply can track the operating frequency:
      - 500MHz/1.8V, 400MHz/1.4V, <333MHz/1.2V

- Typical Au1X00 Active:Idle power ratio: 3-4X

Technology Enhancements

AMD

- Power savings from moving to 0.13um and Mobile SDRAM
  - Core nominal operating voltage
    - 1.4V -> 1.0V reduces core power by ~2X

  - Mobile SDRAM
    - 3.3V -> 2.5V reduces I/O power by ~1.75X
    - The new SDRAMs also have additional power saving modes

Au1X00: Idle Time

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- Active:Idle ratios while playing video clips

System	Video clip encoding	% idle	Chip power
Au1500, ATI PCI card	Low complexity	85-90	<300mW
Au1500, EPSON controller	Low complexity	45-50	500mW
Au1500, ATI PCI card	High complexity movie trailer	30-35	600mW

- High performance design reduces system power

Summary

AMD

- Good video performance does not require high power

- Demonstrated full frame rate video decode at <0.5W

- The Au1X00 family allows tuning system performance and power to meet a range of applications.

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