# A MIMD Multi Threaded Processor

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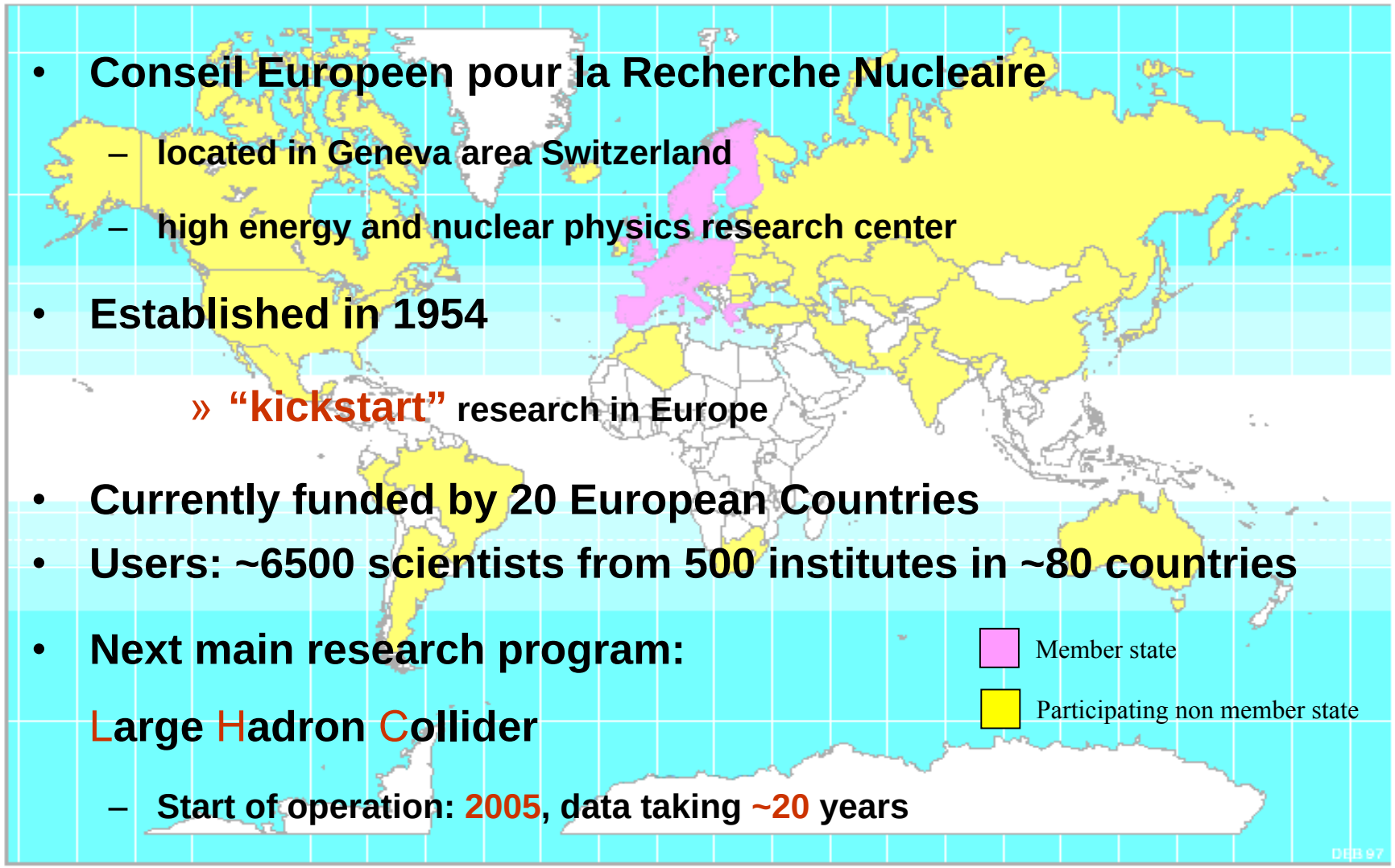
## Outline

- Introduction
- Application for the MIMD processor
- Electronics environment
- The MIMD processor architecture
- Summary

# High Energy Physics

- **Study of fundamental constituents of matter and forces between them**
  - » **quarks, electrons, neutrinos, photon, $Z^0$, $W^{\pm}$, etc.**
  - **– Higher and higher energies are required to delve deeper and deeper into matter**
- **i.e. larger, more powerful, more expensive**
  - **– No longer affordable by individual countries**

# CERN




- Conseil Europeen pour la Recherche Nucleaire
  - located in Geneva area Switzerland
  - high energy and nuclear physics research center
- Established in 1954
  - » "kickstart" research in Europe
- Currently funded by 20 European Countries
- Users: ~6500 scientists from 500 institutes in ~80 countries
- Next main research program:

  Large Hadron Collider
  - Start of operation: 2005, data taking ~20 years

# Large Hadron Collider & The Alps

4 Interaction points

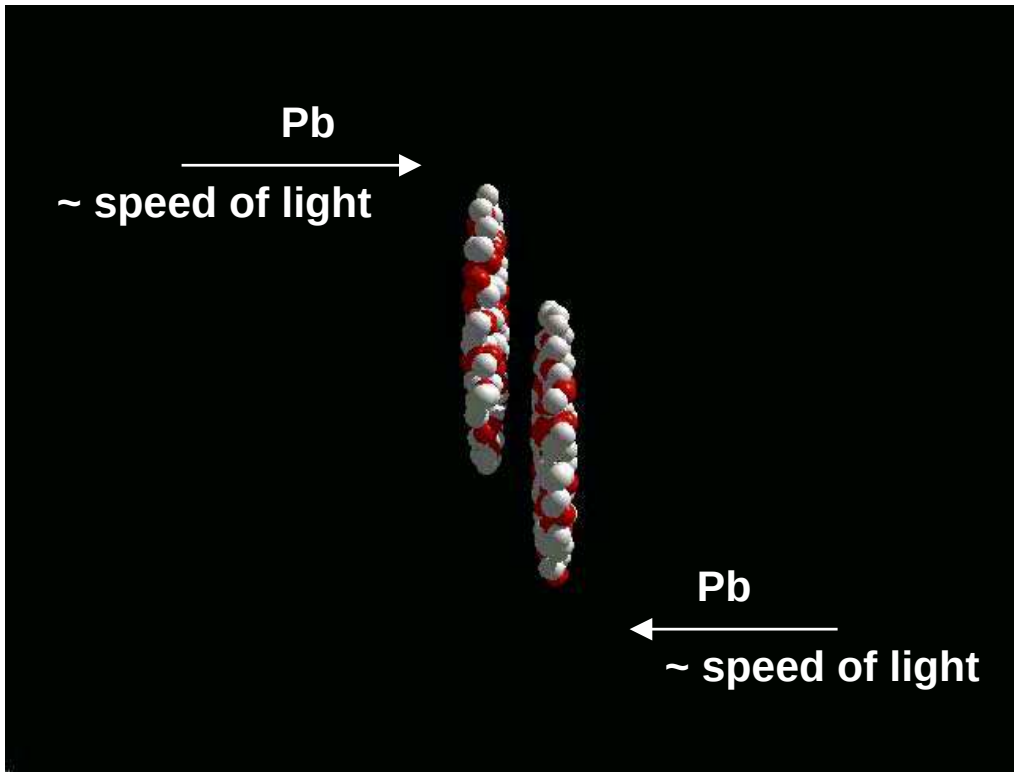



~100m deep

Superconducting accelerator
7 TeV p→←p
5.5 TeV Pb→←Pb

27km circumference

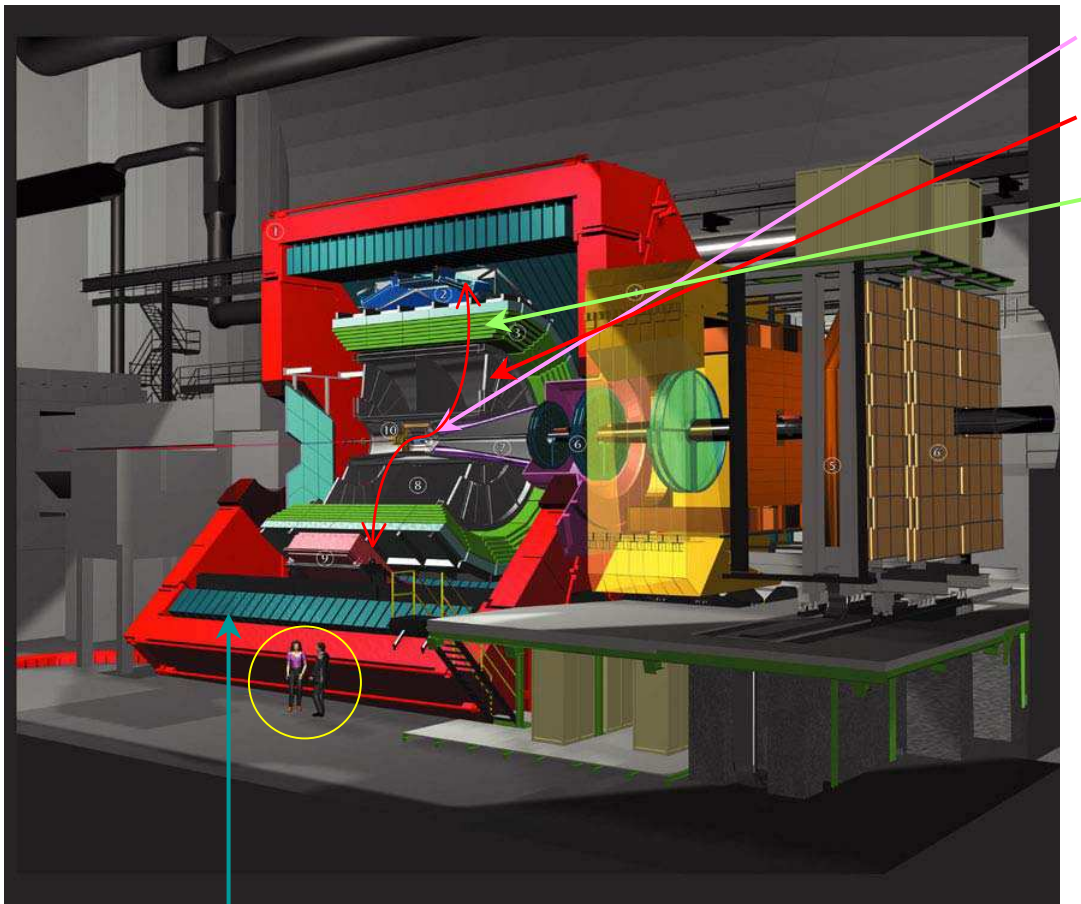
# Nucleons In Collision




- 8000 collisions per second
- Each interaction generating >24 000 particles in acceptance of detector
- Task: Find within one specific particle pair within 6 µs out of 16 000 charged particles
- 6 µs to:
  - digitize 1.2 million data channels @ 10 MHz/10 Bit
  - process 29 Mbytes
  - form global decision

**Main goal is to create the Quark-Gluon Plasma,**
**A state of matter existing during the first few microseconds after the big bang**

# A Particle Detector named ALICE

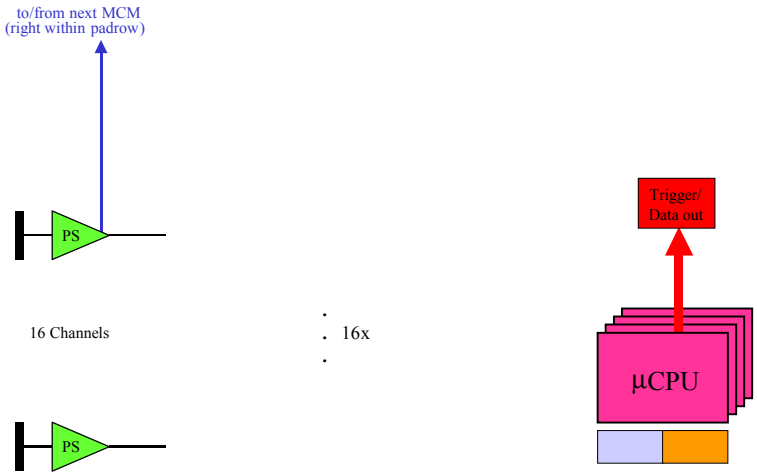


- ITS: 2.62 million channels (1 Bit)
- TPC: 570 000 channels (10 Bit)
- TRD: 1.2 million channels (10 Bit)
  - 1,425 million ADCs
  - Digitization rate: 10 MHz/10 Bit
  - Peak data rate: 17,8 TB/sec
  - 75 000 MIMD processors
  - Computing time of 6 µs
  - Target clock rate: 120 MHz

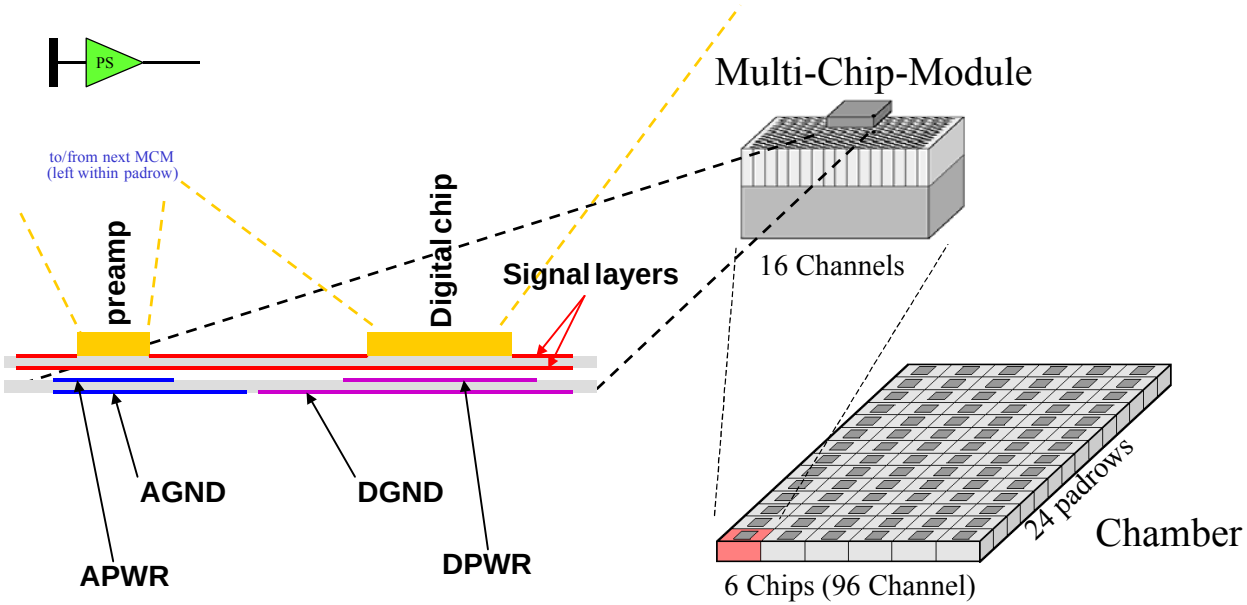
Measures particle trajectories, momentum and provides particle identification

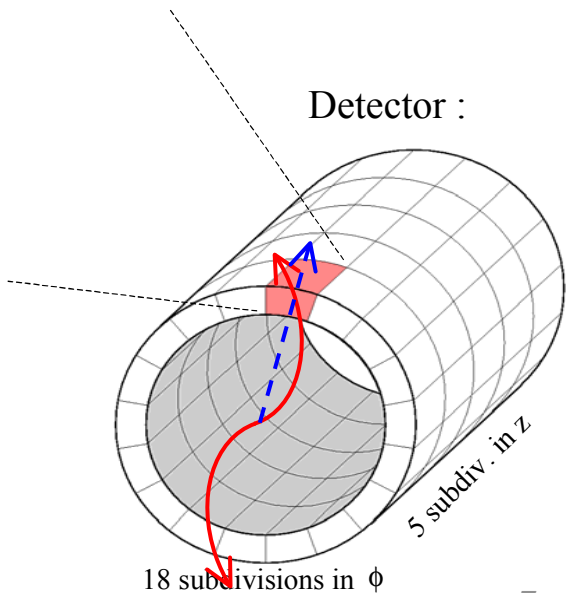
Magnet (0,4 Tesla)

# TRD Electronics Overview

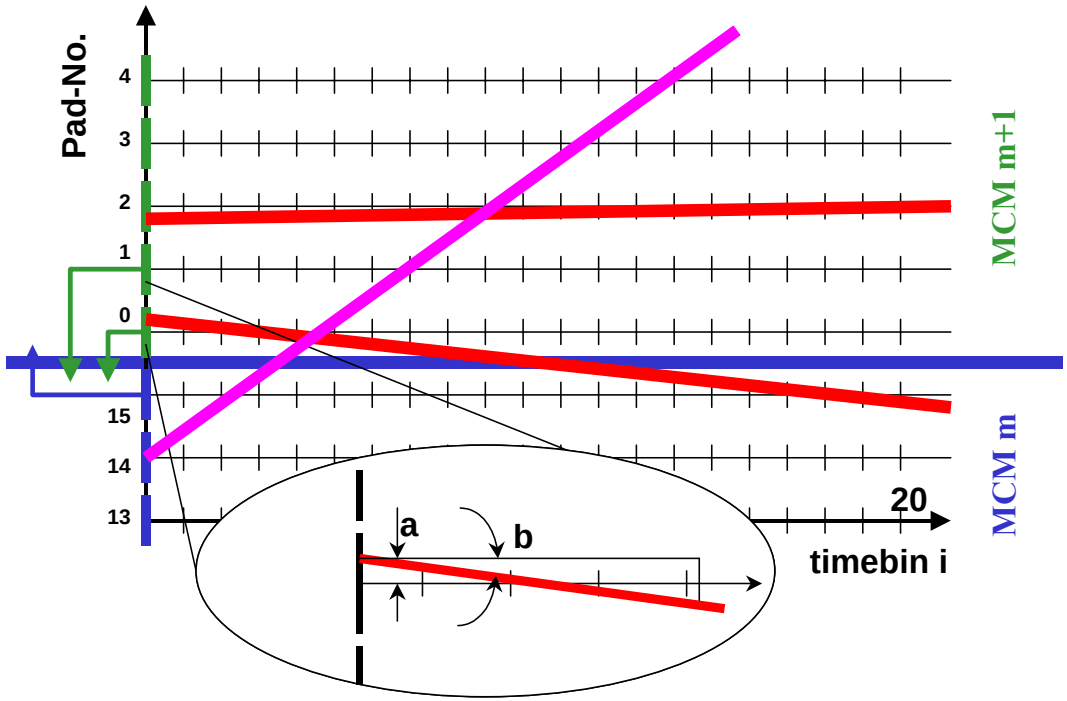



- 1.2 million analog channels @ 10 MHz
- 16 channels per module
- 75000 sources → 1 trigger bit
- track segment processing on chamber
- maximum latency 6µs
- ~20 space points per tracklet
- 4-6 tracklets (layers) per track



# Tracklet Fit Concept




**During Drift Time:**

N = hitcount

y

$^2$ = position$^2$ sum

**After Drift Time:**

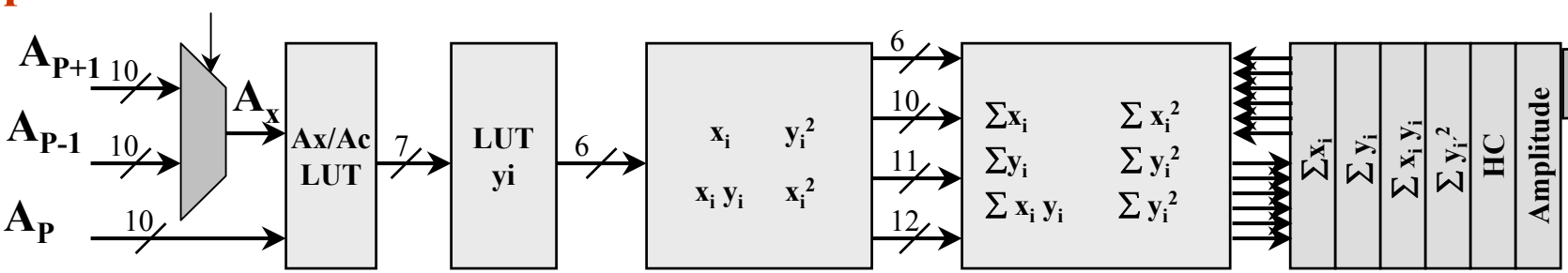
a = intercept $a = \frac{\sum x_i^2 \sum y_i - \sum x_i \sum x_i y_i}{N \sum x_i^2 - \left(\sum x_i\right)^2}$

b = slope $b = \frac{N \sum x_i y_i - \sum x_i \sum y_i}{N \sum x_i^2 - \left(\sum x_i\right)^2}$

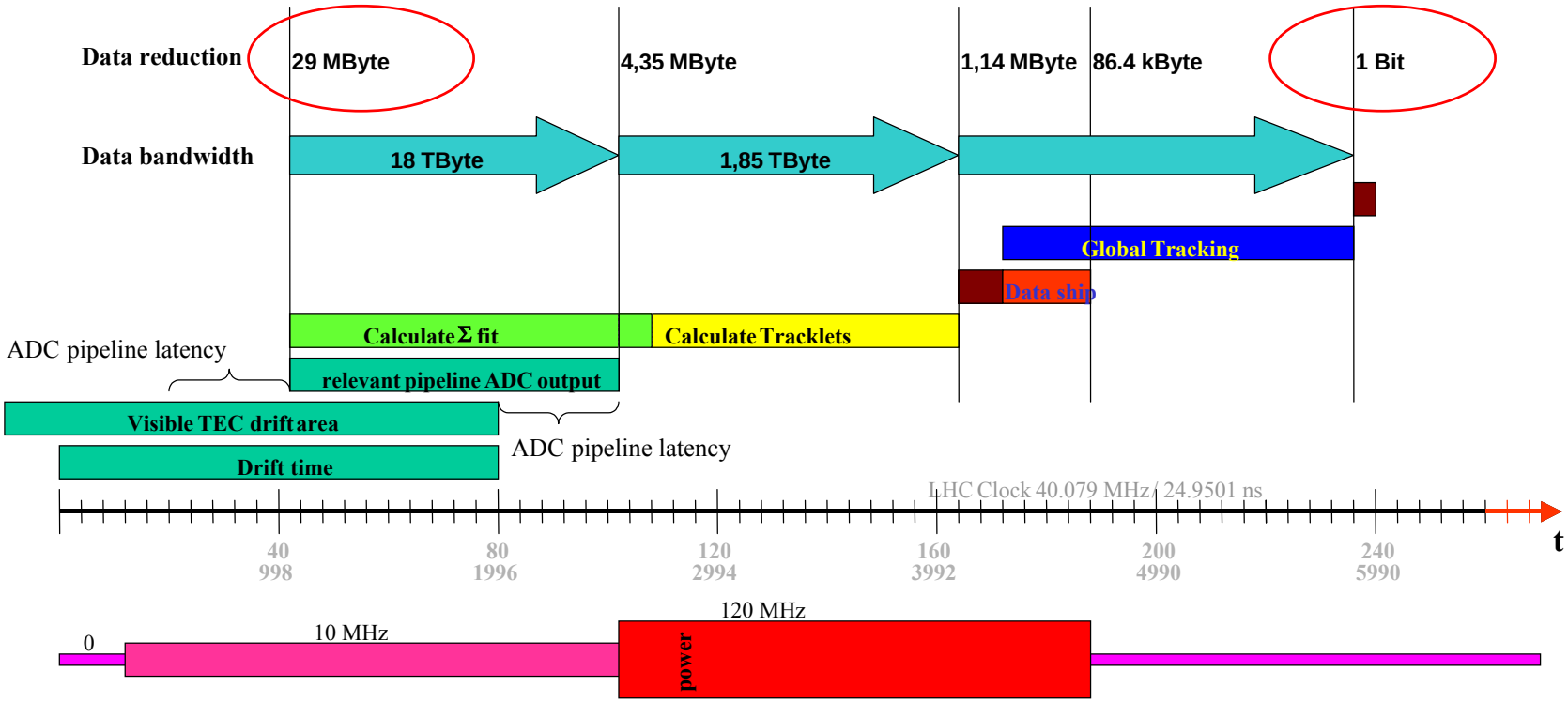
$\chi^2$ = track quality

merge track segments in padrow

**Pipelined Calculation :**

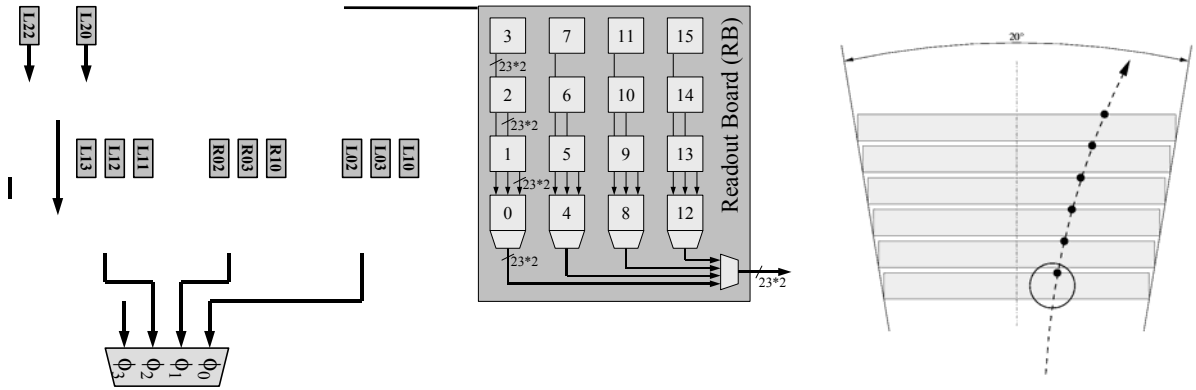


# TRD Trigger Timing and Data Flow

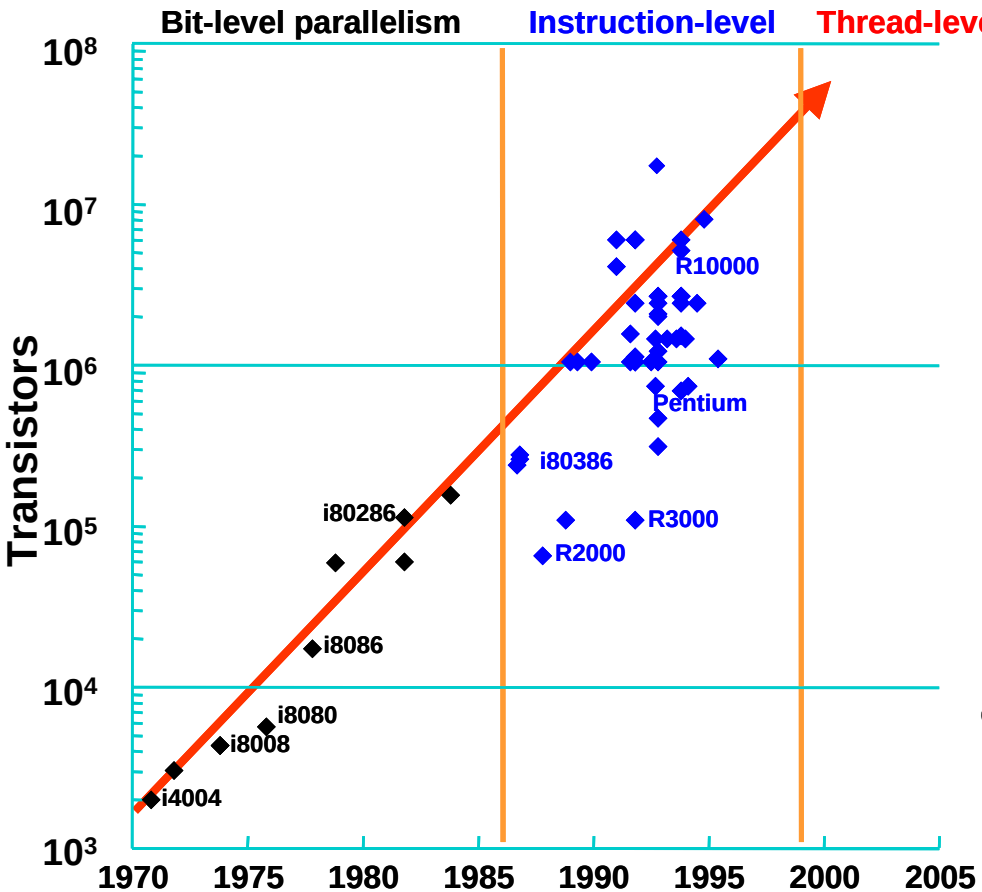


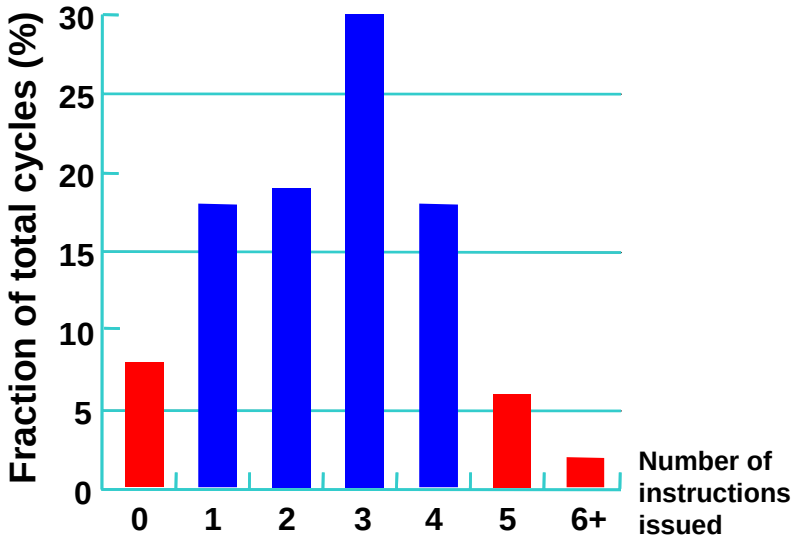

- Highly I/O bound: 17.8 TB/sec
- Very tight time budget: 1.8 + 1.5 µs

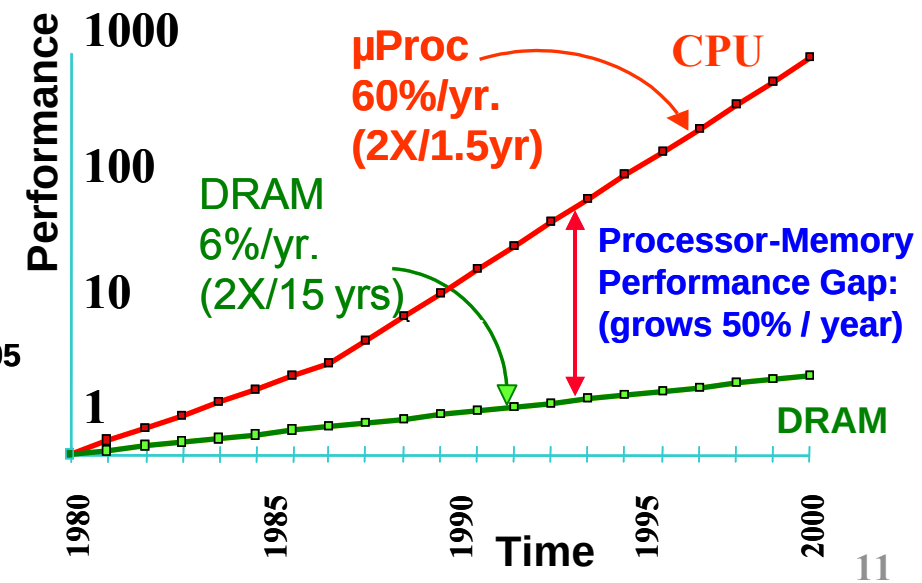
# Next Step: Compute and Combine



# Computer Architecture Trends



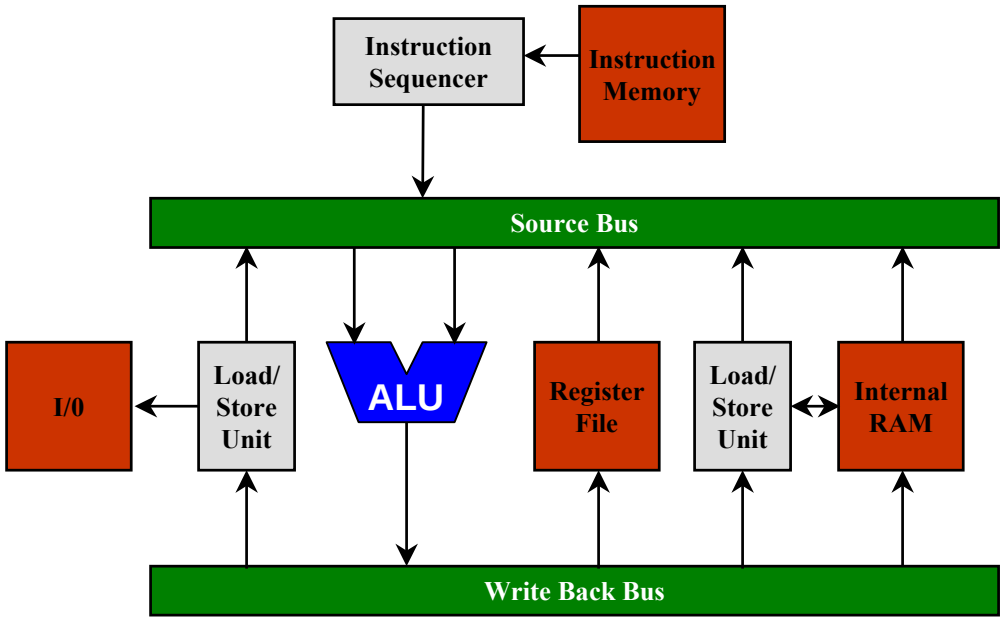



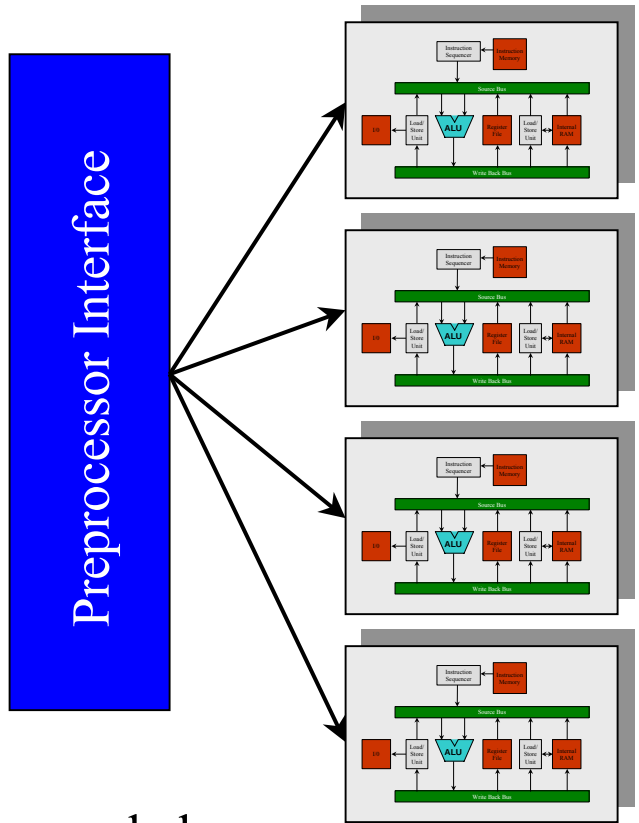



# Why MIMD with Shared Memory?

- 1.5 µs computing time @ 120 MHz ⇒ 180 clock cycles
- ~120 clock cycles required to finish one task
- Four tasks have to be done ⇒ ~ 480 cycles needed
- The processor must execute up to four tasks on different data objects
- Arithmetic operations should be executed in one clock cycle
- Data has to be shared without overhead ⇒
  - Quad Ported SRAM (QPM)
  - Global Register File (GRF)
- Four tasks ⇒ Four CPUs
- Same code ⇒ Quad port instruction memory saves chip area
- MIMD

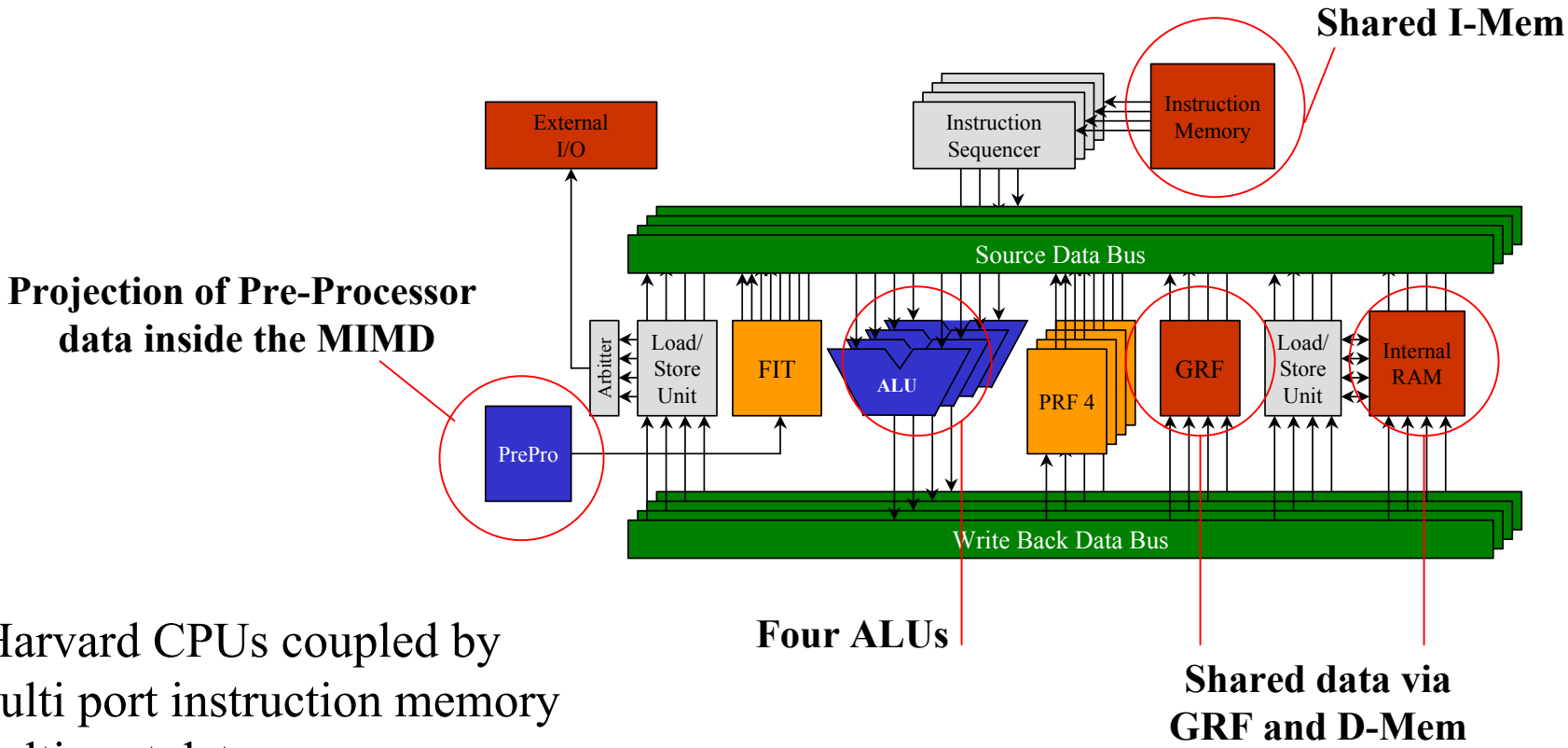
# Generic Processor Architecture




- To execute up to four tasks in real time, four CPUs are needed
- Independent CPUs can't share data or program

# MIMD Architecture



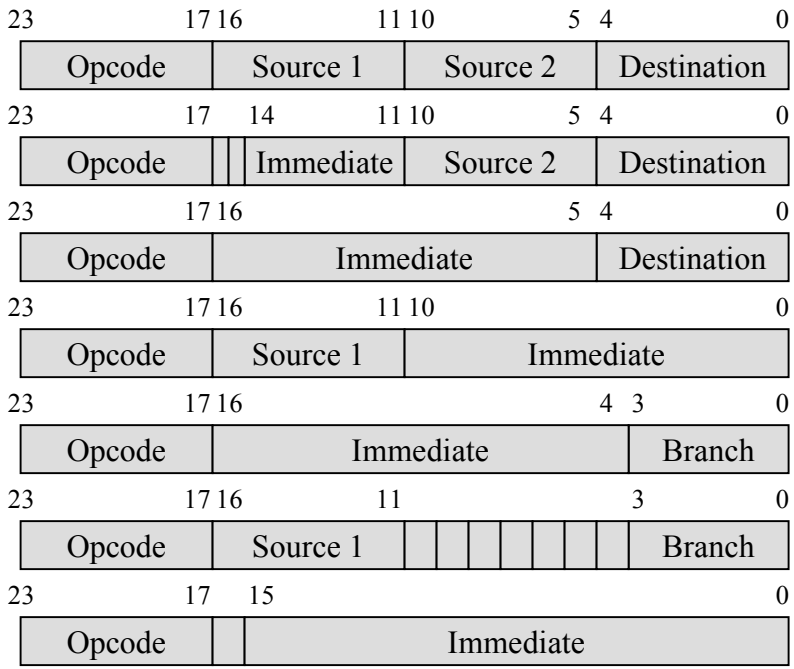

- Four Harvard CPUs coupled by
  - multi port instruction memory
  - multi port data memory
  - Global Register File (GRF)
- Register based interface to Pre-Processor
- Two stage pipeline (fetch/decode, execute/write back)
- **Architecture can be adopted to any general purpose processor**

# Some Features

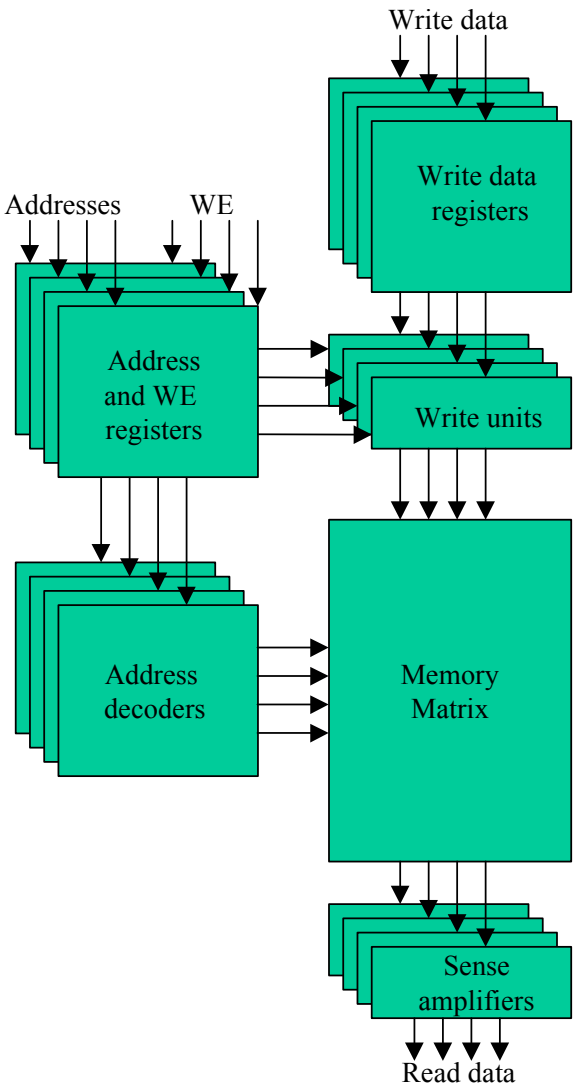
- 16 Bit data word
- 16 private registers per node
- 16 global registers common to all nodes
- 24 Kbytes quad port

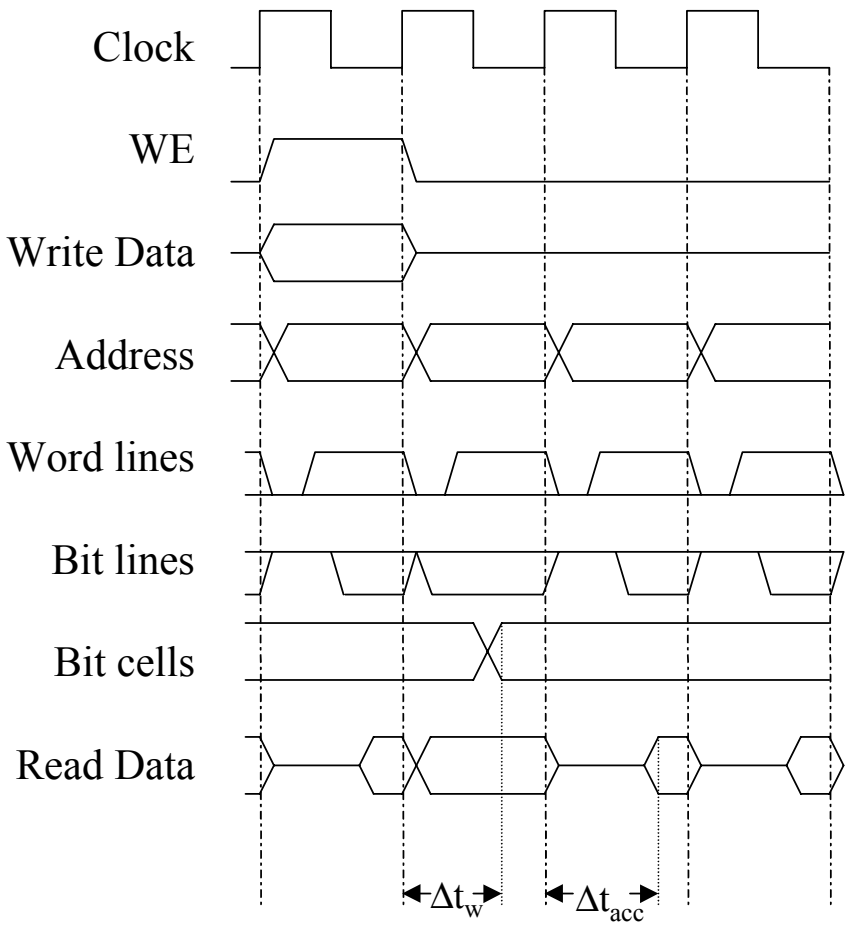
# Instruction Set and Format

- 24 Bit fixed length instruction word
- 70 instructions in total
  - 22 ALU instructions
  - 26 branch instructions
  - 3 instructions for synchronization
  - 14 Load/Store instructions
  - 4 instructions to handle interrupts



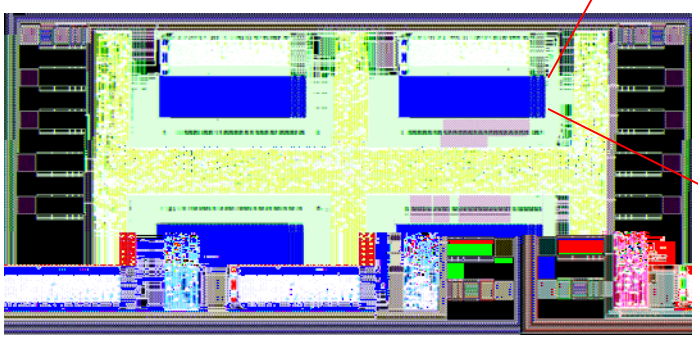
# Quad Port Memory

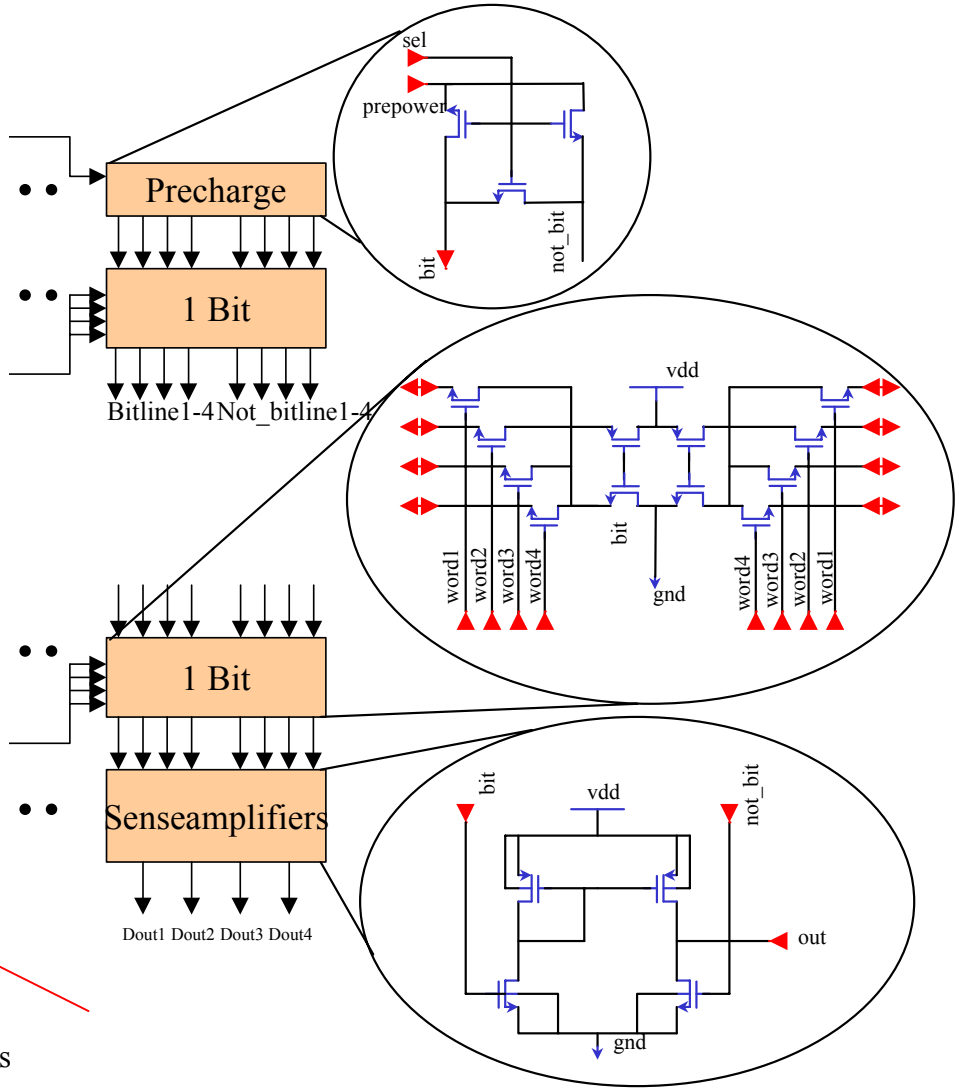


# A Closer Look Inside the MPM

- **Full custom design used for quad port 16 bit data memory and 24 bit instruction memory**
- **Delivers/receives data to/from 4 CPUs simultaneously**
- **Max. access time is about 2 ns (0.18 µm)**
- **Needed access time 6 ns**
- **Organized in blocks of 64 lines**
- **Line width is parametrizable**

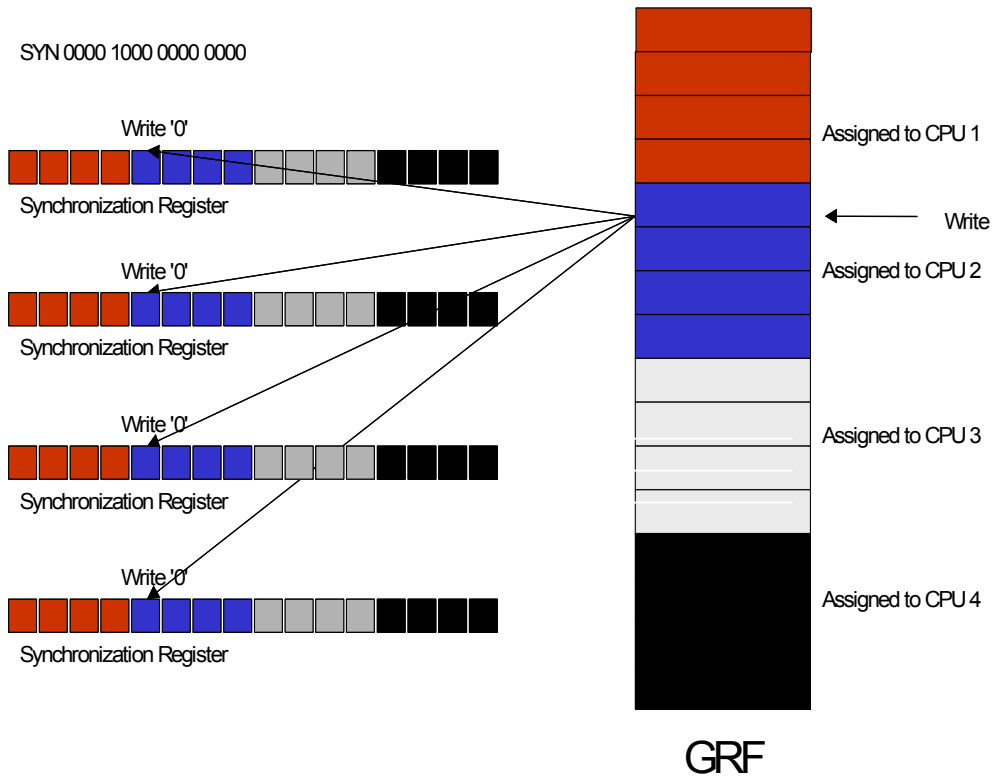




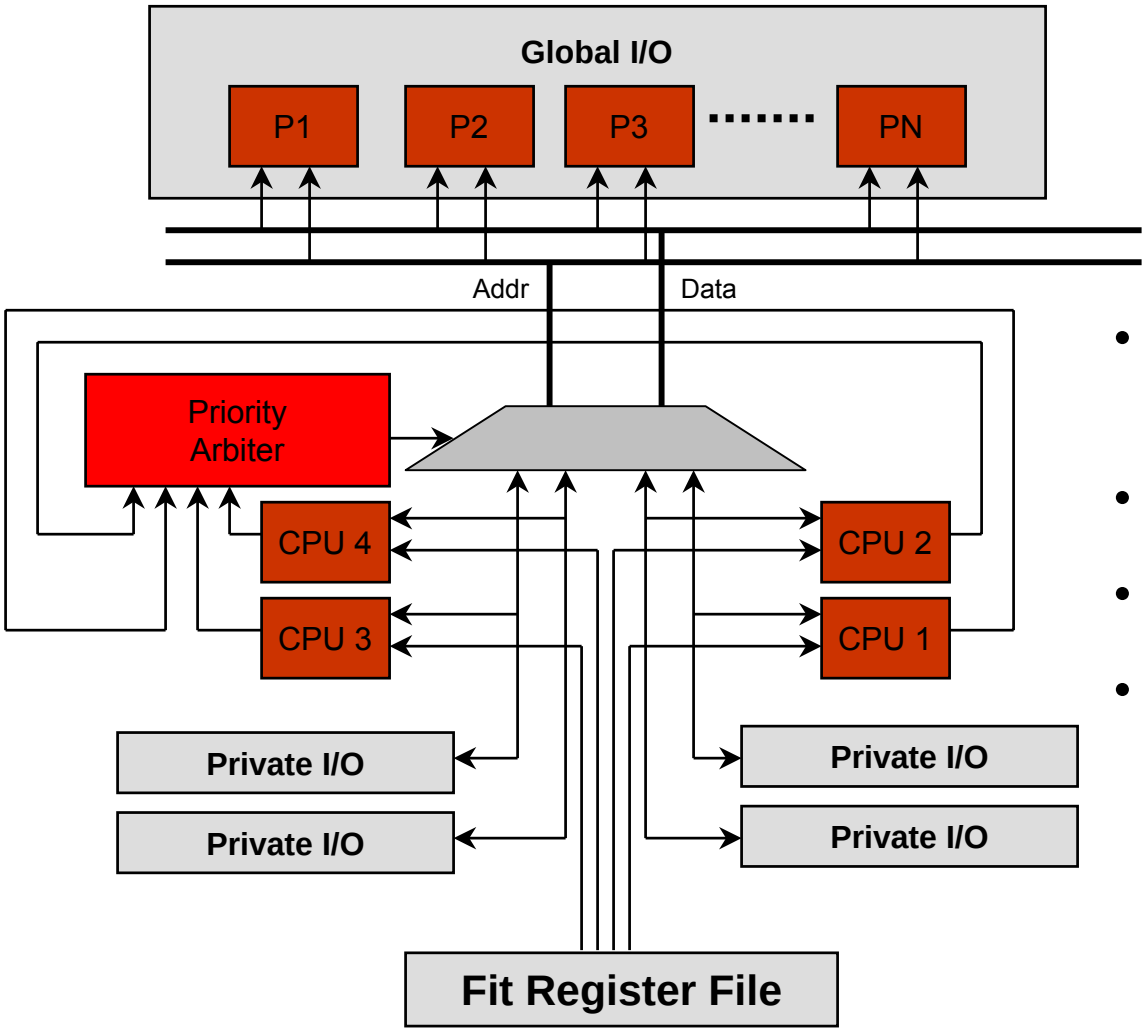

Four blocks of the MPM with additional test logic in 0.35 µm process

# Synchronization

- Three instructions for synchronization
  - **SEM** sets the synchronization mask
  - **SYN** suspend the PC
  - **SYT** copies the synchronization register
- Implementation of flexible synchronization patterns
- Synchronization implemented as a side effect of access to the GRF



# Data I/O




- Direct input from preprocessor via multi ported registers
- Private I/O to external links
- System bus for peripheries
- Arbiter to select a CPU

# Summary

- High Energy Physics presents very interesting challenges in the computer science (high throughput, low latency, low overhead, massively parallel processing)
- Use of Multi Ported Memories (MPM) enables integration of multiple generic processor cores as MIMD unit
- MPM as global register file allows zero overhead, asynchronous multi processor communication (semaphores, locks, etc.)
- MPM operating as buffer memory provides scalable, independent access to shared data structures
- MPM operating as buffered crossbar switch allows tight integration of I/O for network and I/O processors
- For further information contact www.ti.uni-hd.de

**US/PCT Patend Pending: 6,067,595**