The Network Processor Revolution

Fast Pattern Matching and Routing at OC-48

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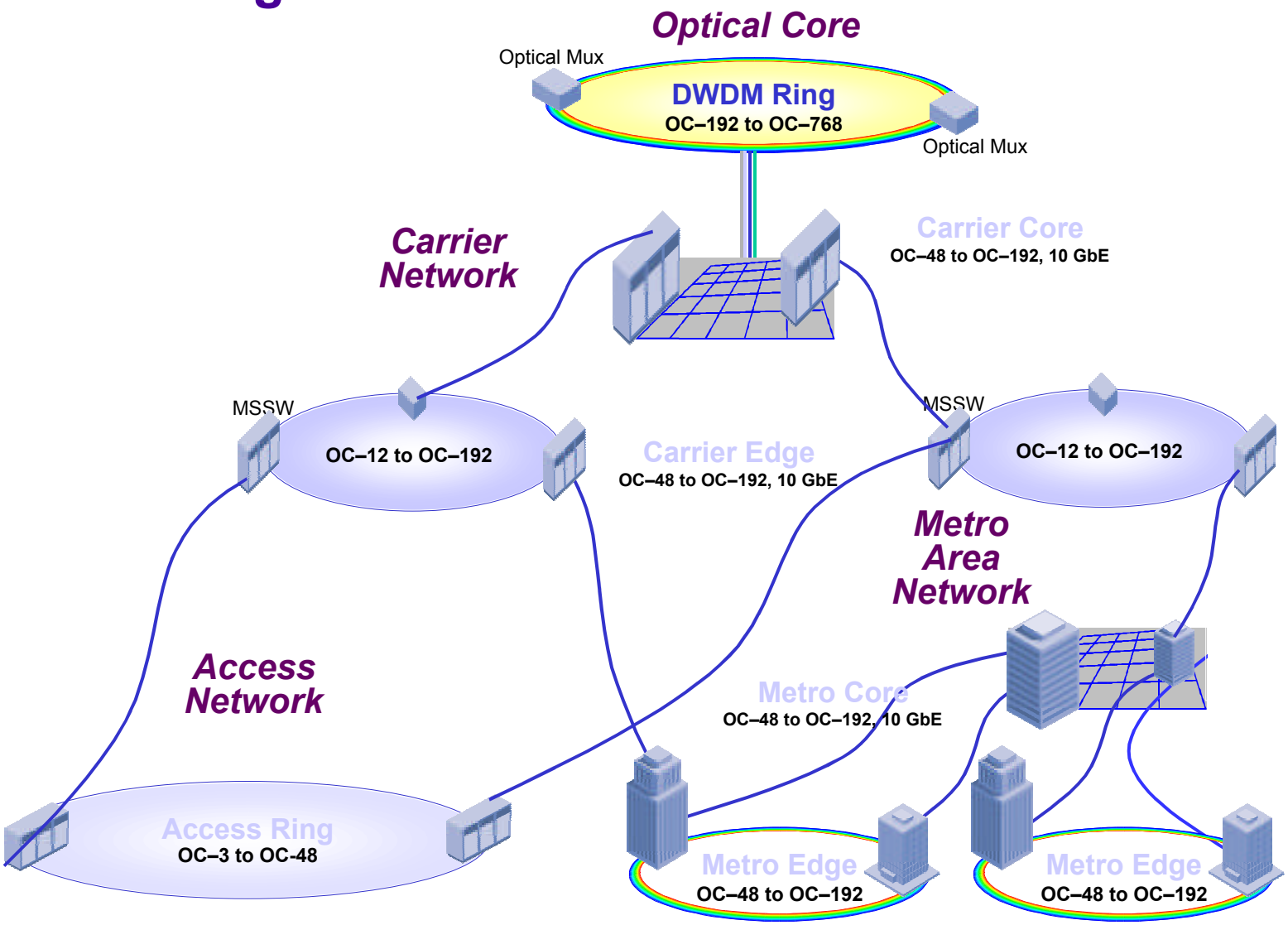
Market Segments



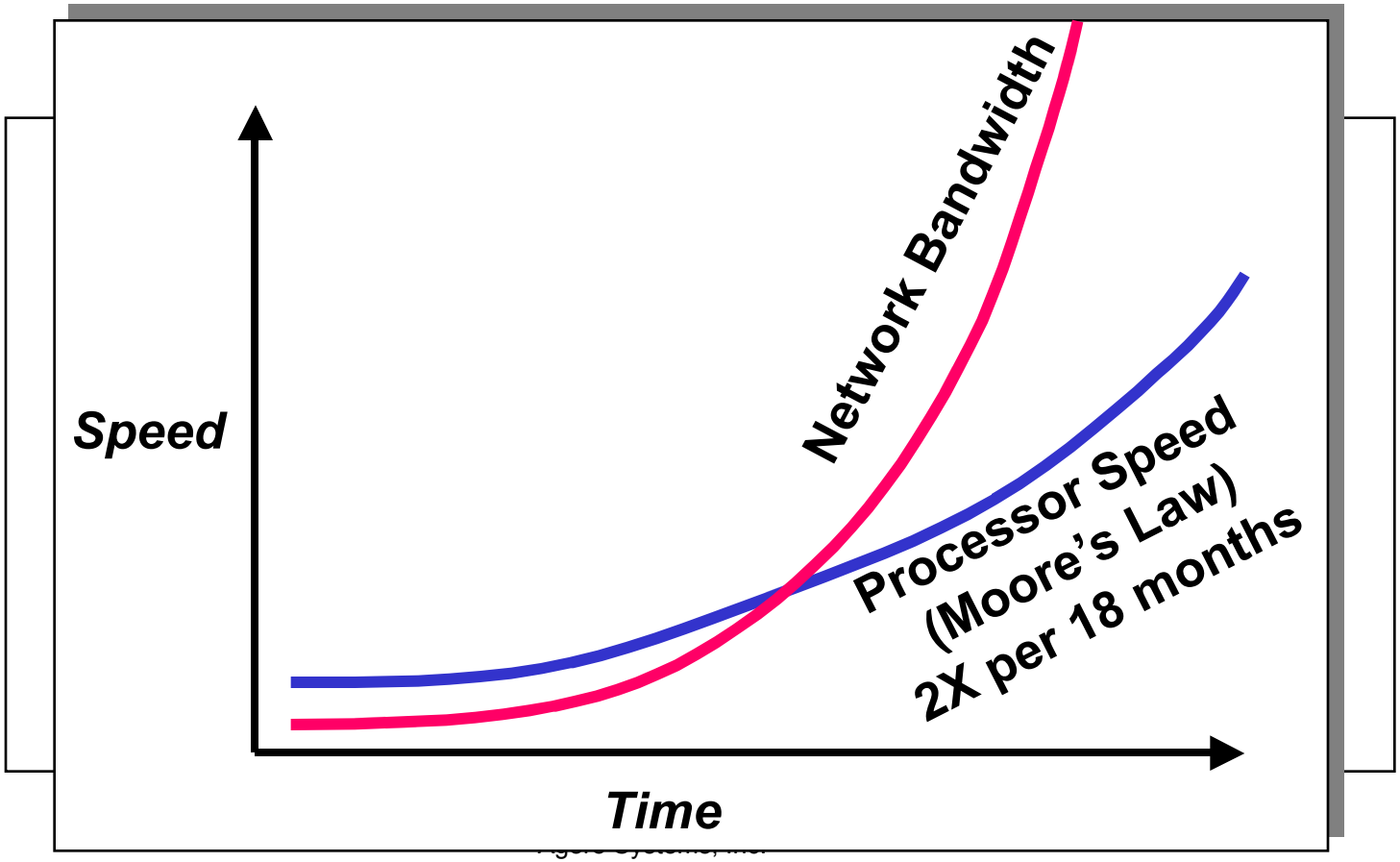
Agere's Approach

- Family of Chips for Network Devices
- New "Data-Flow" Approach
- High-level Software Programming

What are the old approaches?

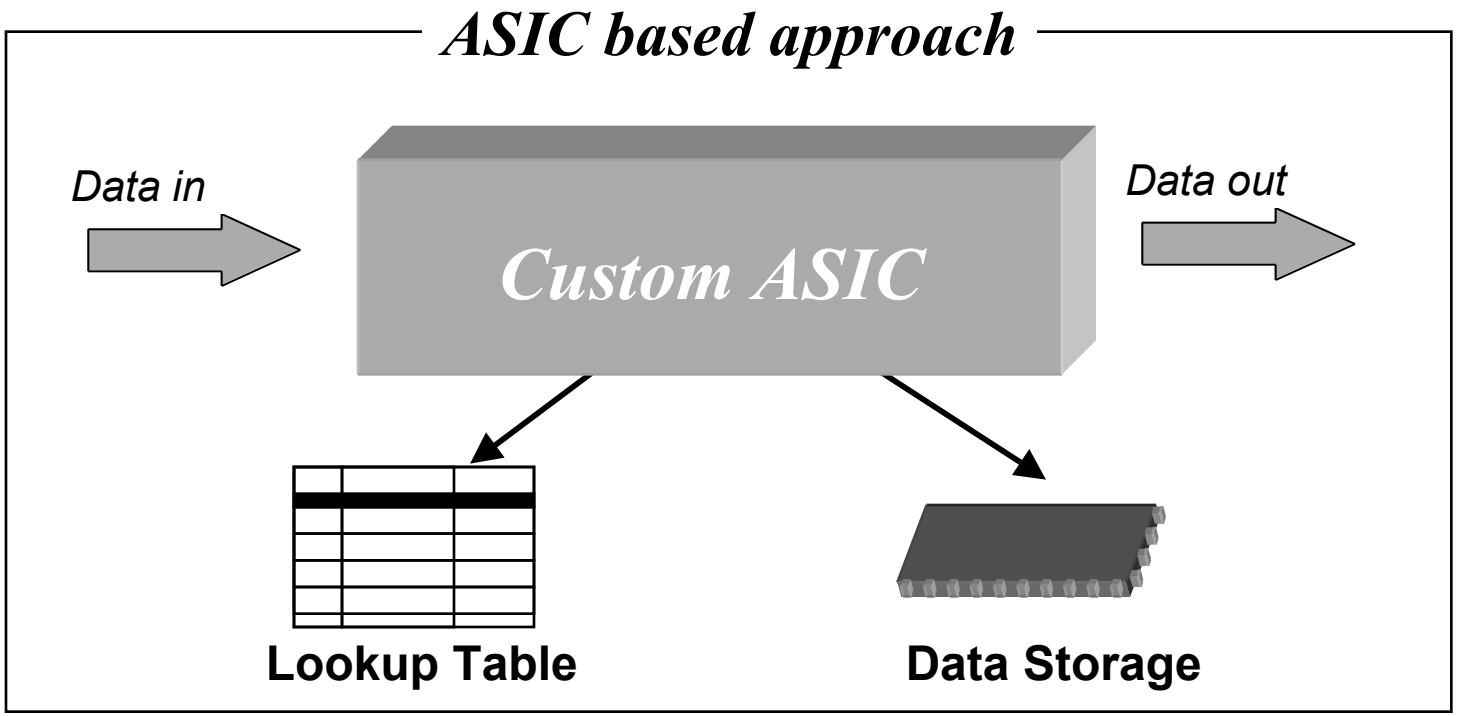
Old Approach

- Worked well for awhile
- Higher speeds, more functionality needed
- Started falling behind dramatically



Old Approach #2

- **Develop custom ASIC to perform wirespeed routing/queuing**
  - High development costs
  - Long time to market
  - No flexibility (e.g. IPv6 = forklift upgrades, Diffserv = forklift upgrade)

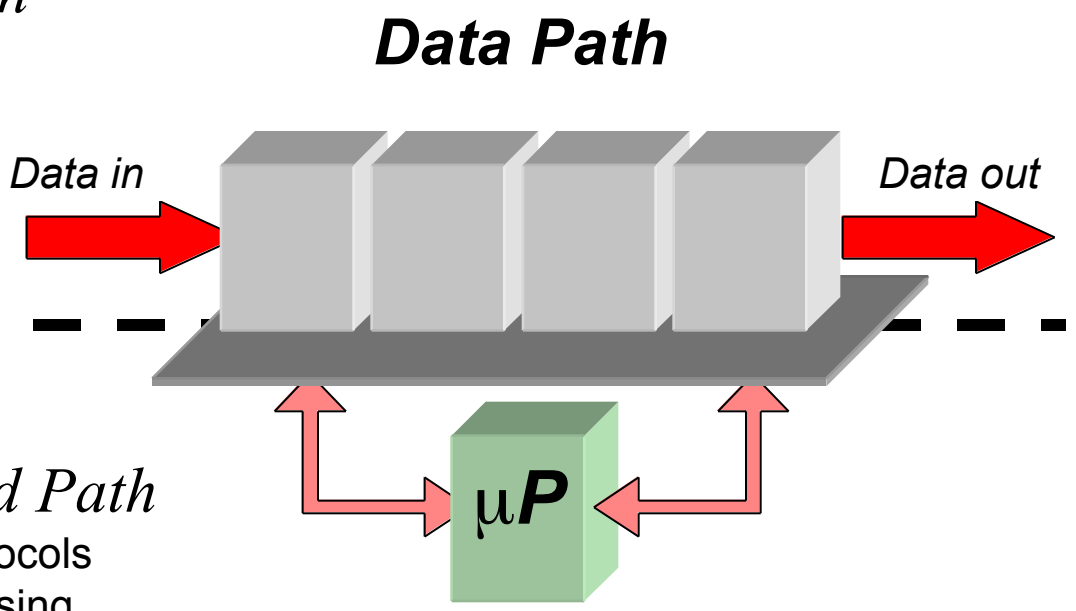


Agere's Approach

- **Highly pipelined chip-set for fast "Data Path"**

Wire-speed Path

- Forwarding
- Shaping
- Queuing
- SAR
- Monitoring, etc.

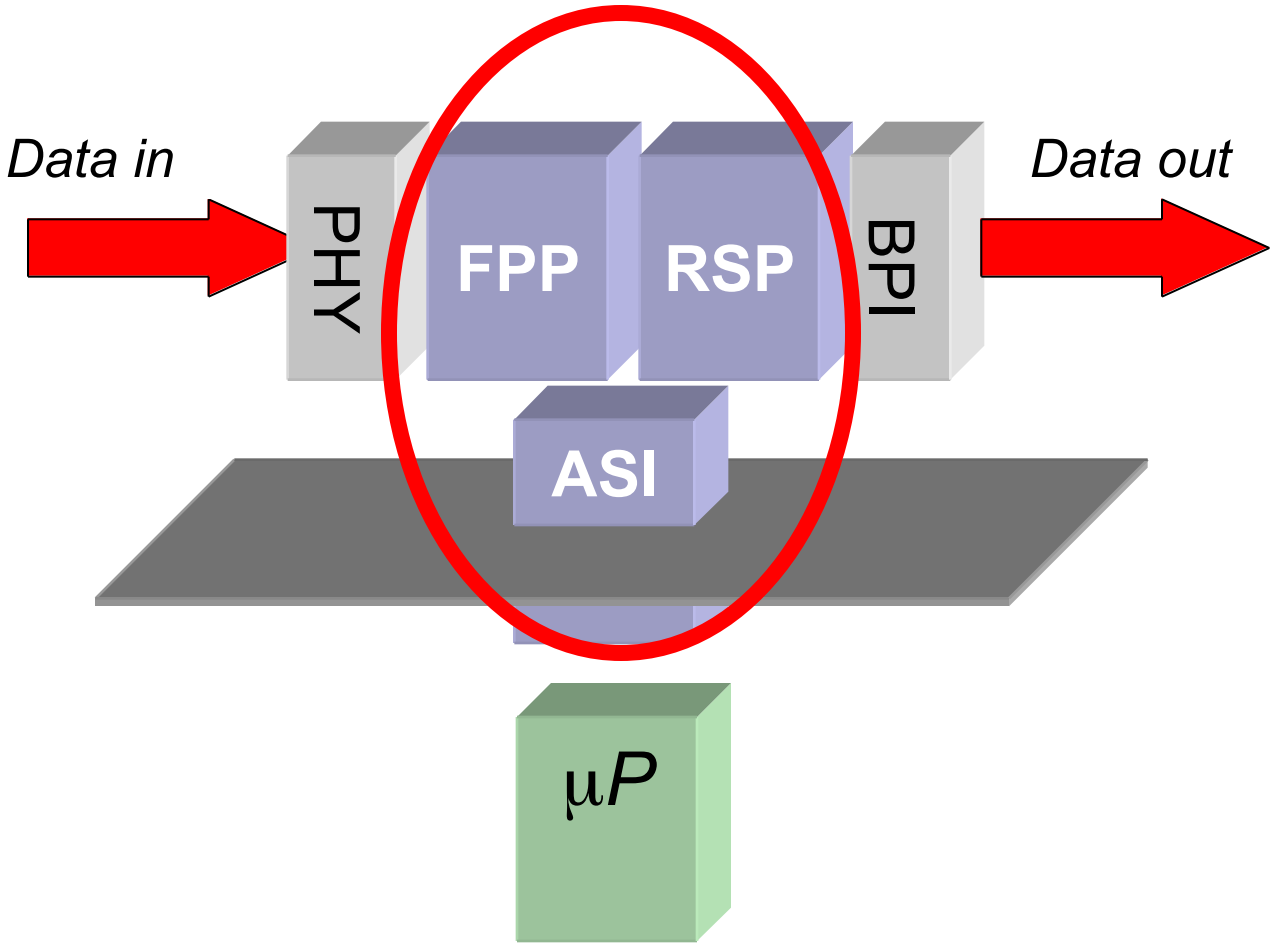


Slow-speed Path

- Routing protocols
- Error processing
- Statistics reporting
- Configuration, etc.

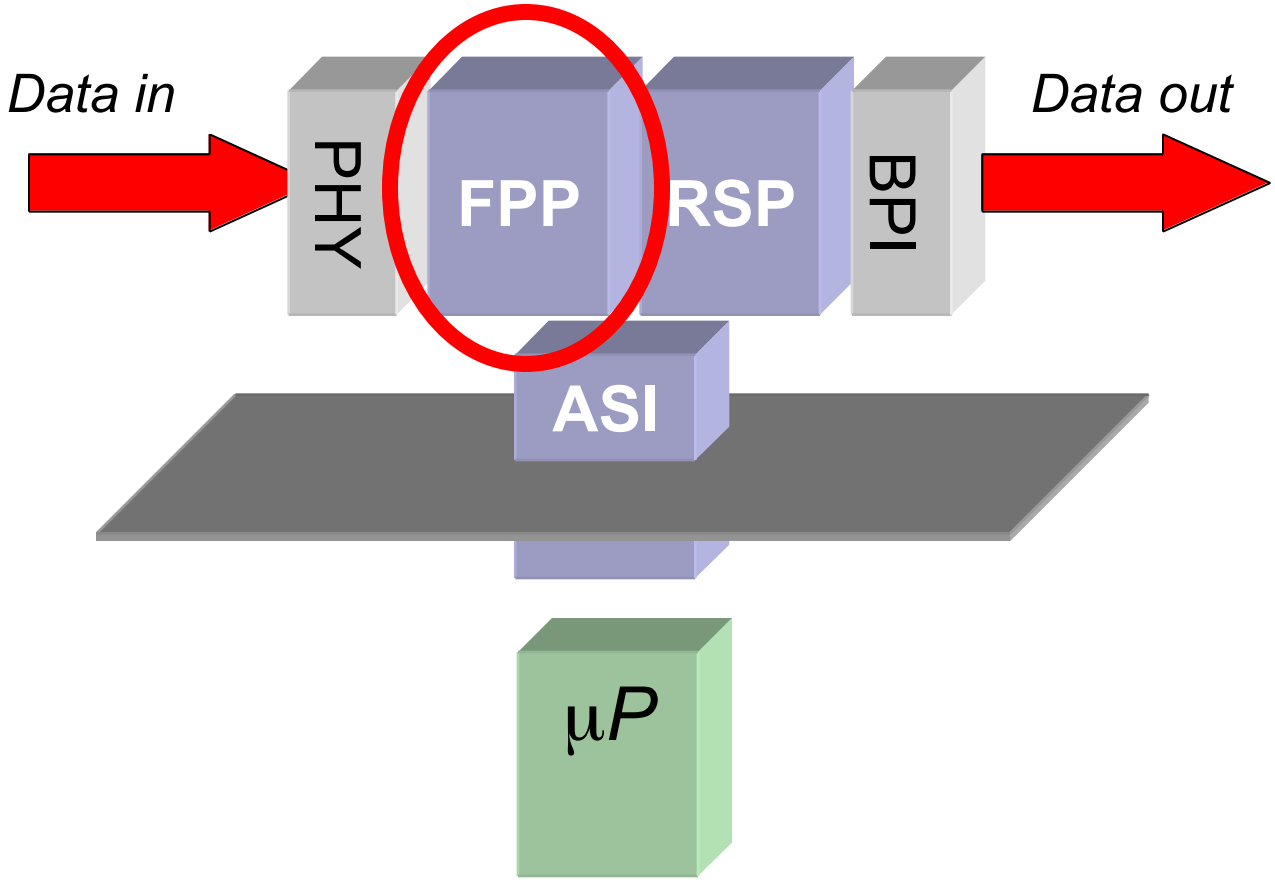
Agere's Approach

- Agere chip-set forms the wire-speed path



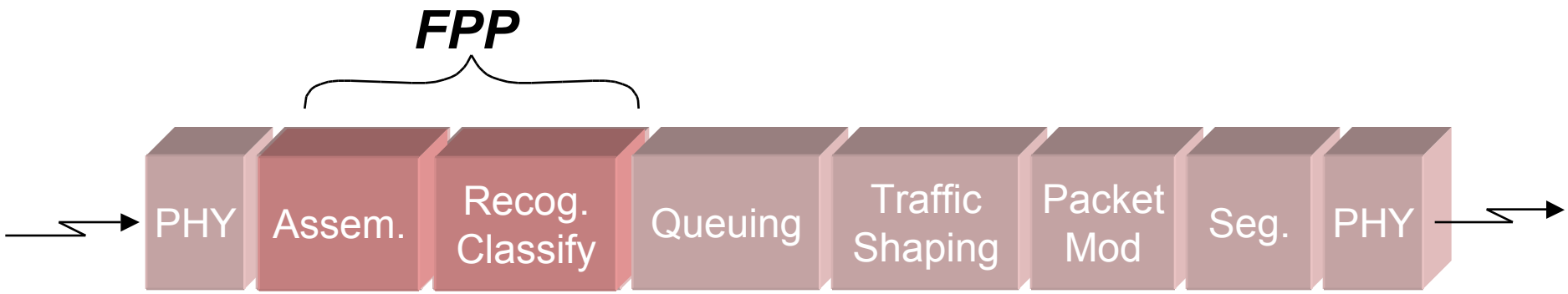
System Overview

- Fast Pattern Processor (FPP)



System Overview - FPP

- Recognition/Classification/Filtering
- Functional Processing
- Assembly (if necessary)



System Overview - FPP

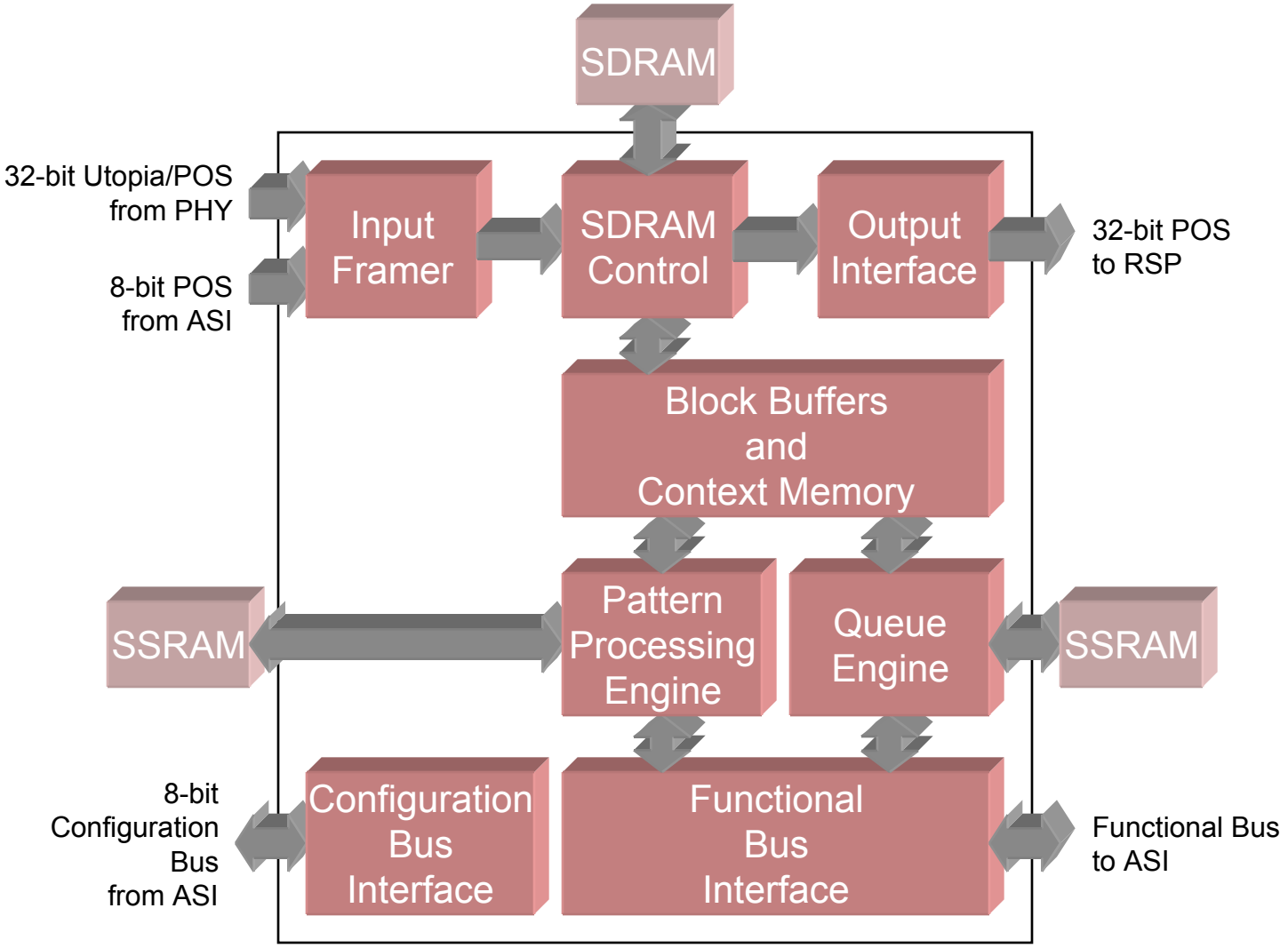
Features

- Programmable classification up to Layer 7
- Functional Programming Language
- Highly pipelined multi-threaded processing of PDUs
- ATM re-assembly at OC-48c rates
- Table lookup with millions of entries & variable entry lengths
- Configurable UTOPIA/POS interfaces

Benefits

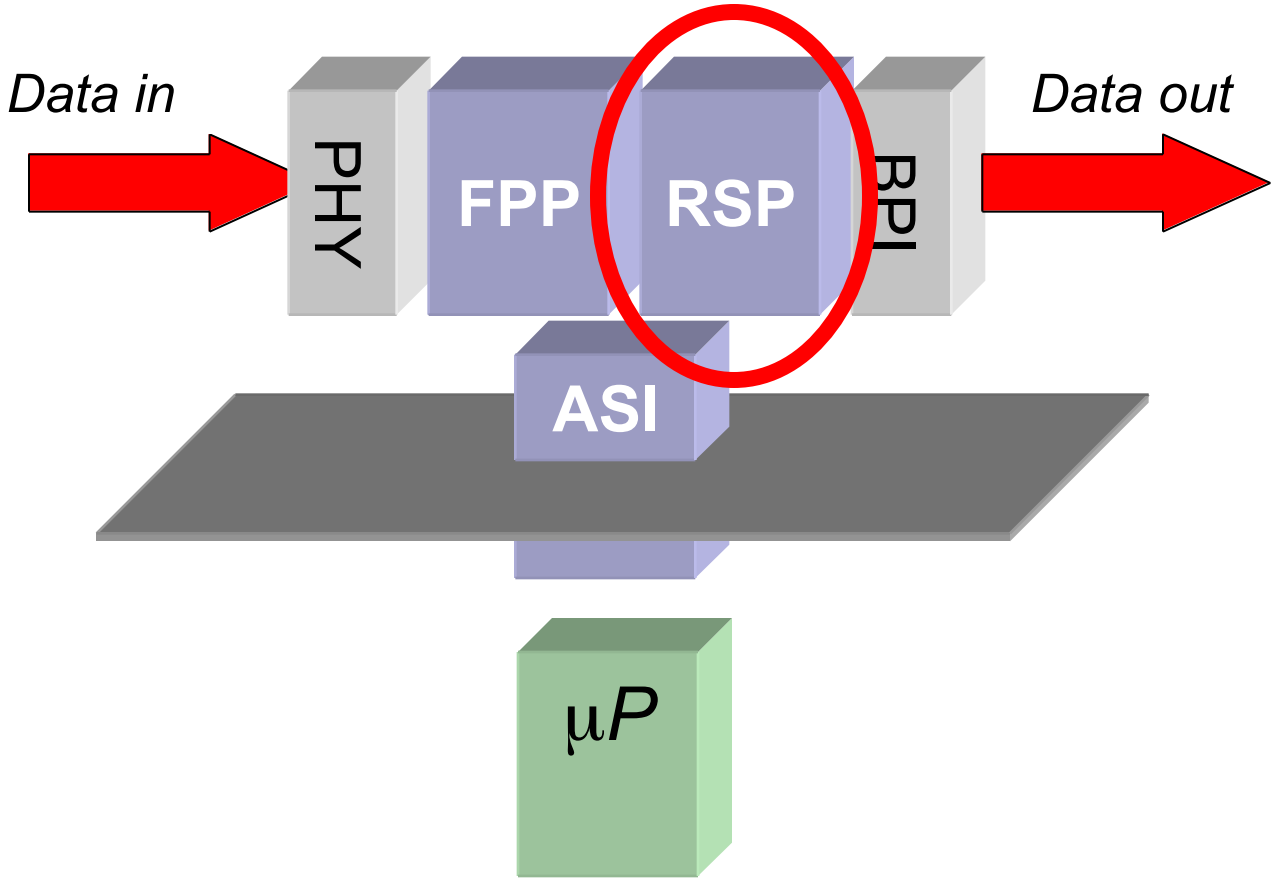
- Time to market, ease of upgrade
- Reduces development time, code maintenance
- High performance scalable architecture
- Eliminates external SAR
- Eliminates need for external CAMs; deterministic performance regardless of table size
- Simplifies design and reduces development cost

System Overview - FPP



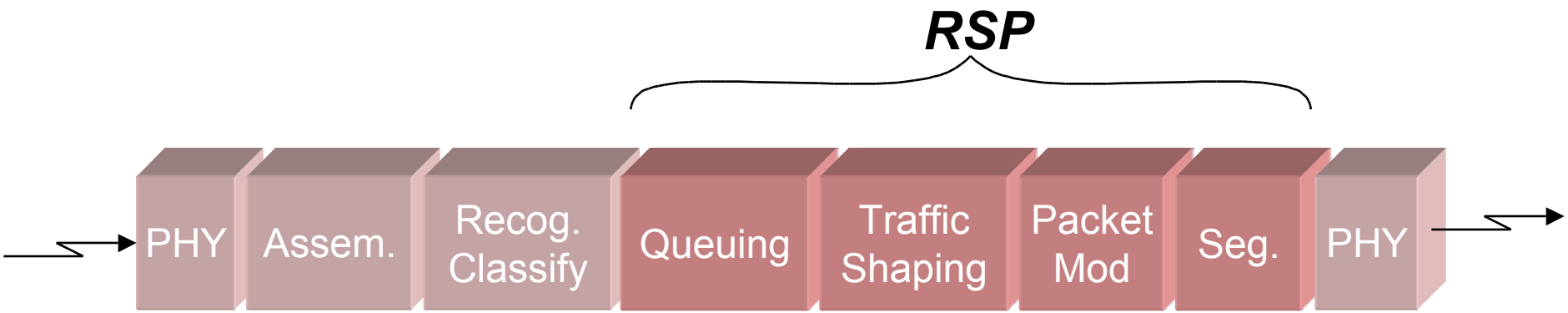
System Overview

- Routing Switch Processor (RSP)



System Overview - RSP

- **Transmit queuing**
- **Traffic Management and Shaping**
  - Quality of Service (QoS), Class of Service (CoS)
- **Packet Modification**
  - Including Segmentation



System Overview - RSP

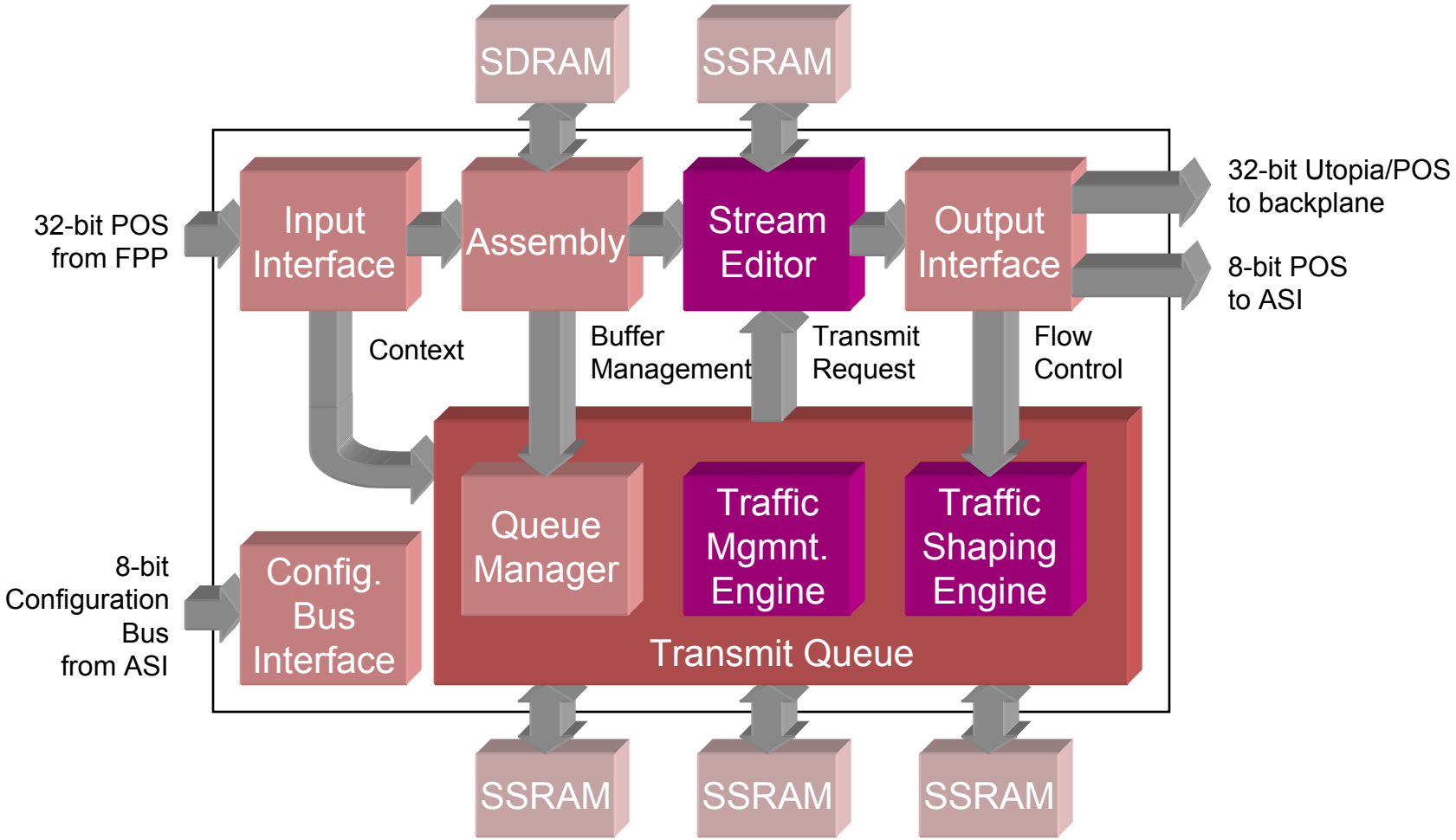
Features

- **64K queues**
  - programmable shaping (such as VBR, UBR, CBR)
  - programmable discard policies
  - programmable QoS/CoS
  - 16 levels of priority
- **Programmable packet modifications**
- **Support for Multicast**
- **Highly pipelined processing of PDUs**
- **OC-48c bandwidth**
- **Generates required checksums/CRC**

Benefits

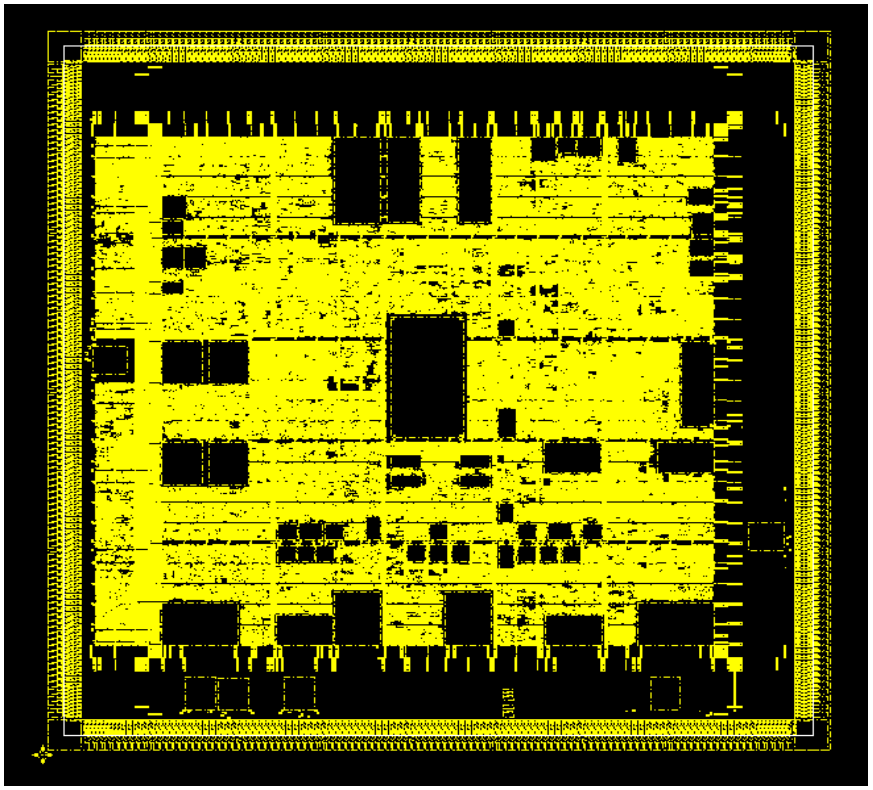
- **Large number of connections**
  - OEM Differentiation
  - Enables new policy based management system
- **Support for emerging apps**
- **Consistent software model across all programmable features**
- **High performance architecture**
- **Smart processing at very high bandwidths**

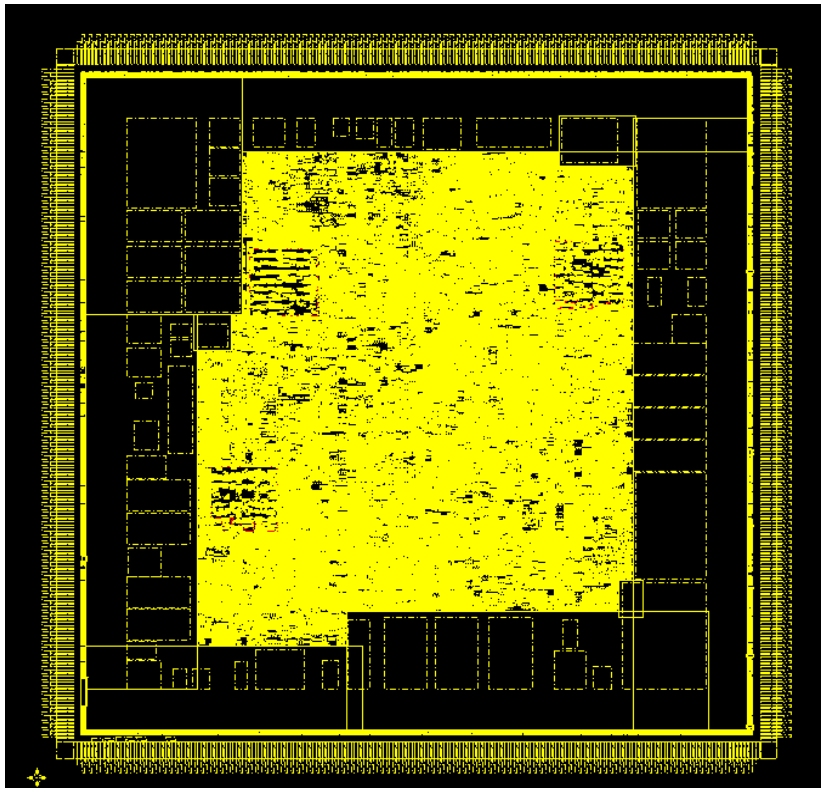
System Overview - RSP



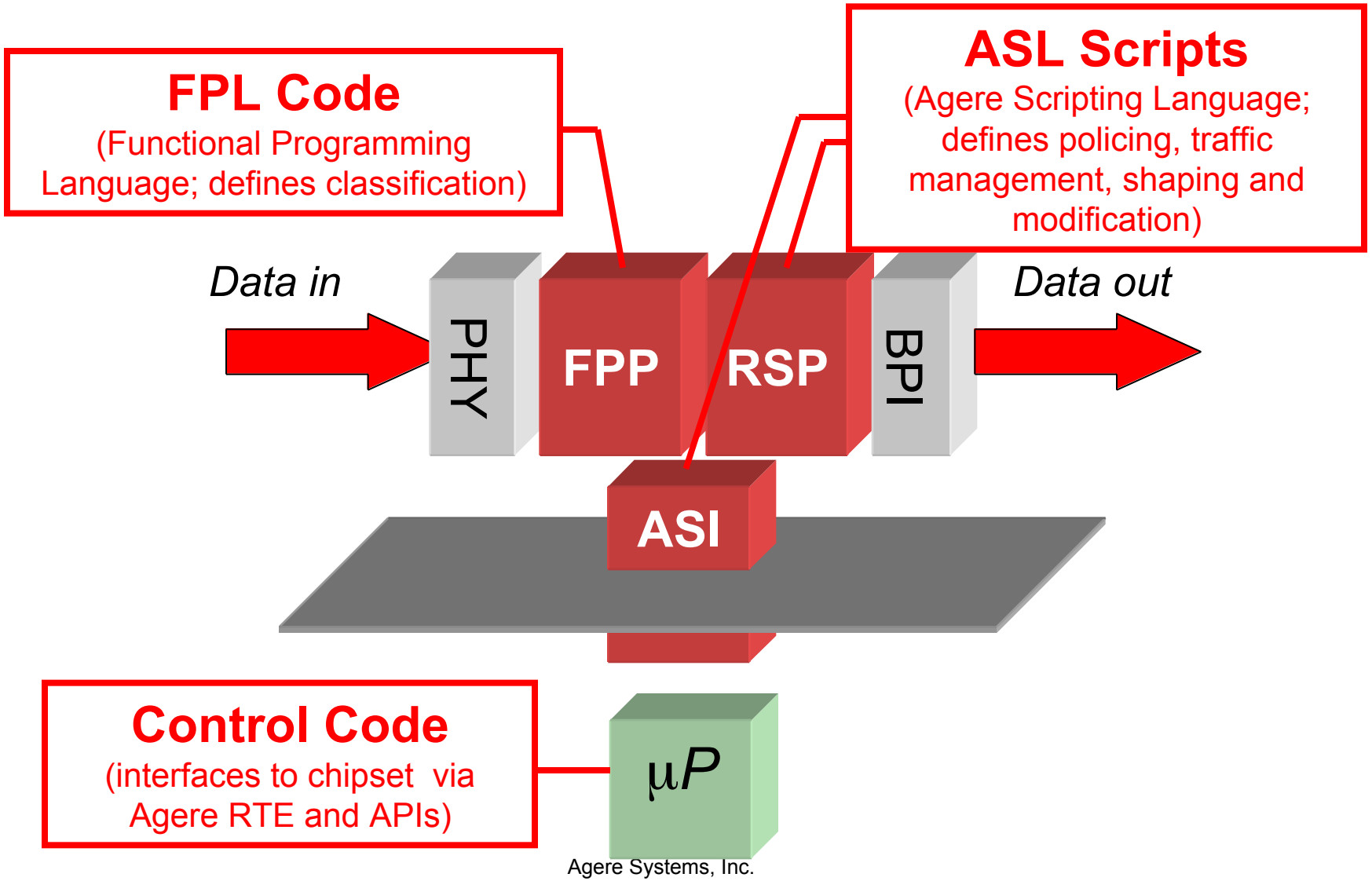
Chip Details (Payload Plus Chipset)

- TSMC 0.18um technology
- 26.4 million transistors
- 1.33 million RAM bits
- Measured Power Consumption: 6.2W





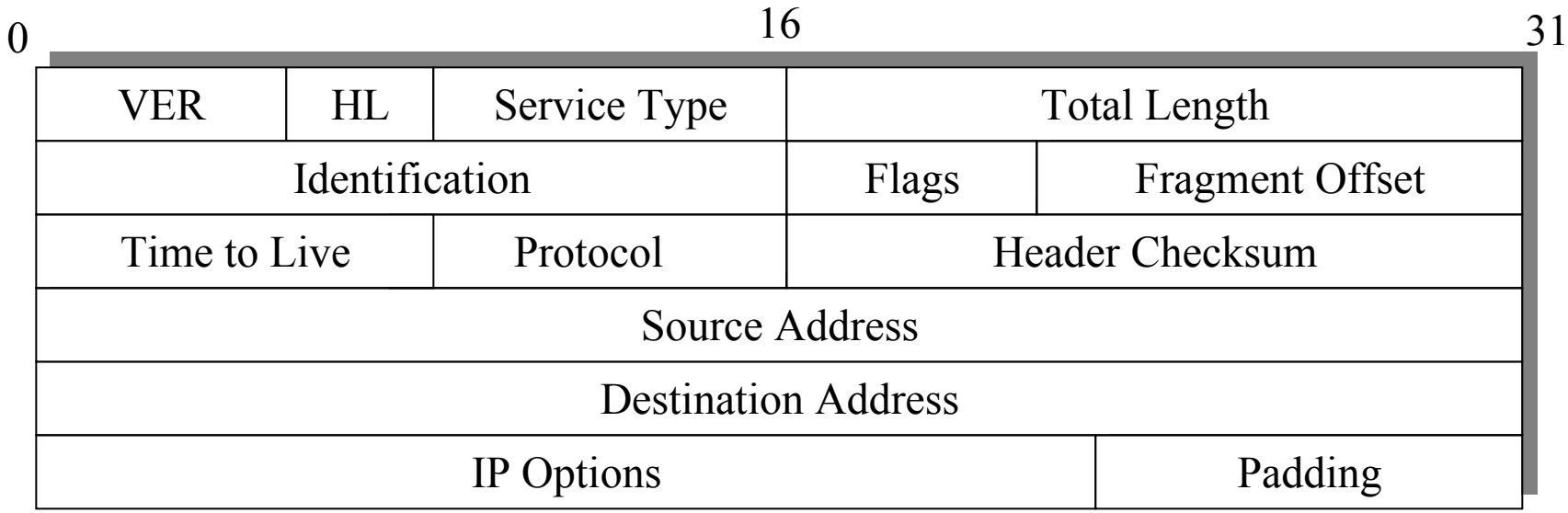
Software Landscape



Functional Programming Language (FPL)

- **FPL is a high-level language expressly designed for high-speed protocol processing**
  - Fast pattern matching of the data stream
  - Easy-to-understand statement semantics
  - Dynamic updating of FPL programs in the FPP
  - A complete software development tool set

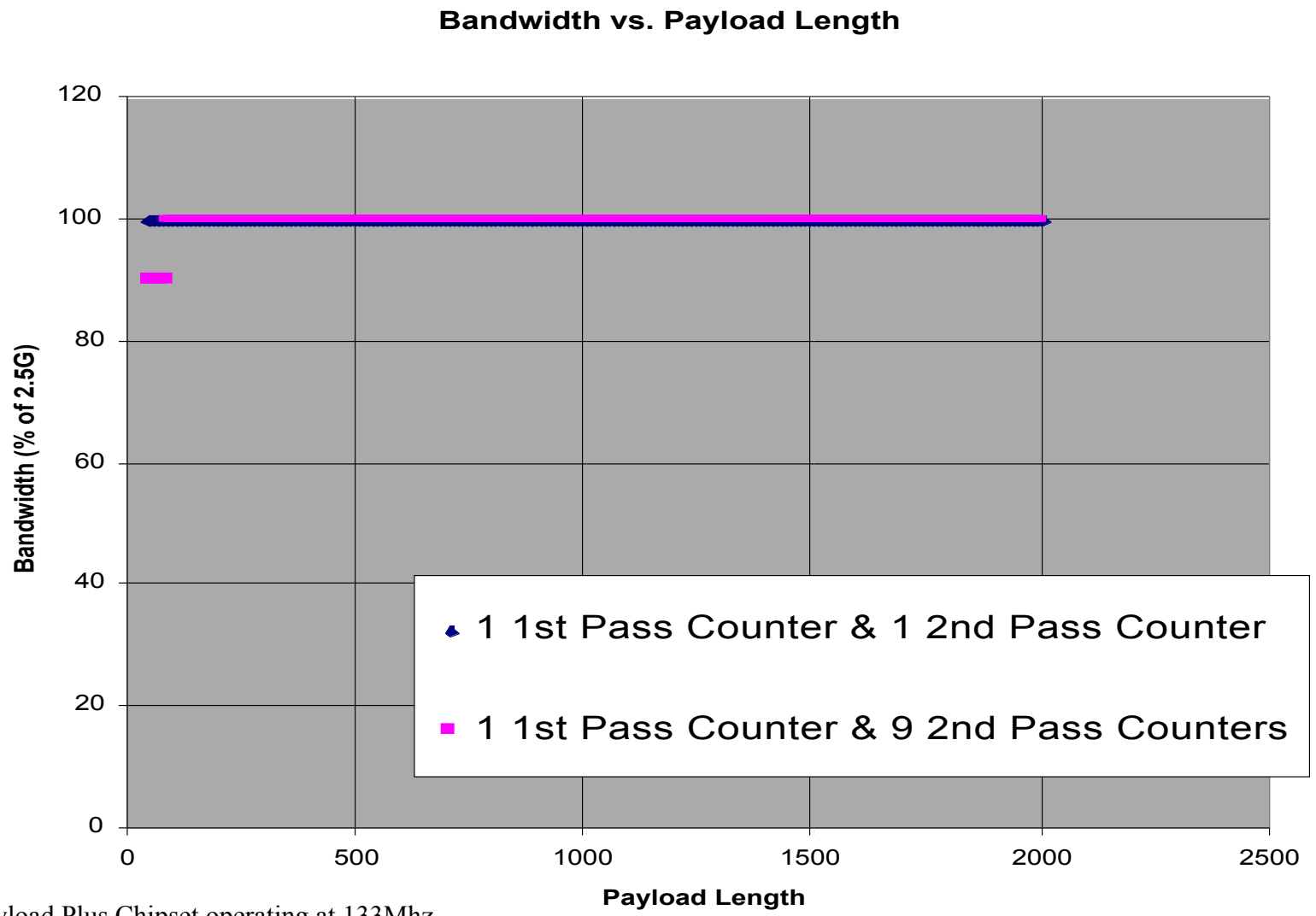
FPL IP Processing Example




```
IP: IPv4_header fskip(36) dest=route fTransmit(dest);
```

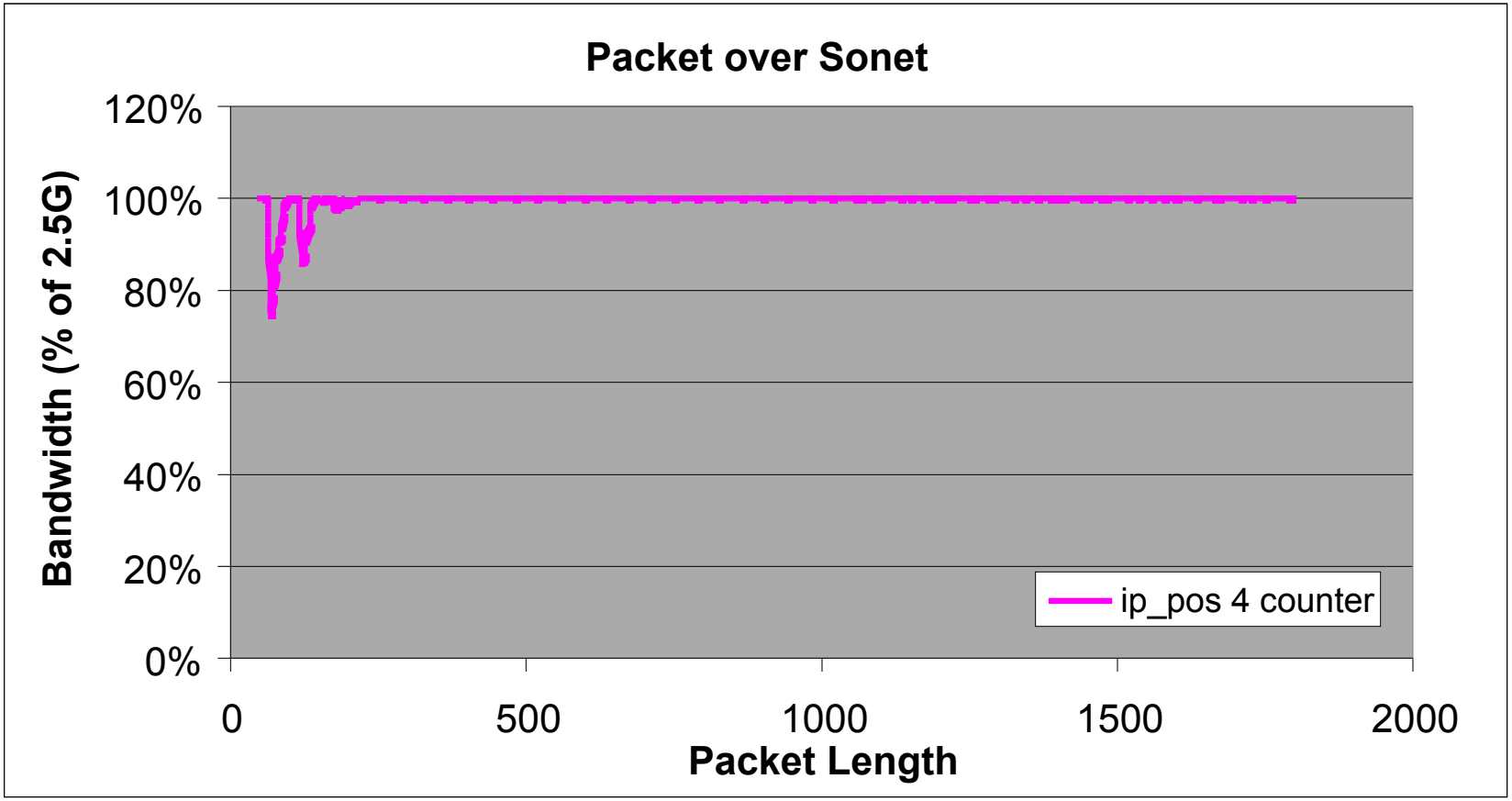
```
route:  10.20.15.12   freturn(FILTER)
route:  10.20.15.*    freturn(LOCAL)
route:  10.20.*.*     freturn(GATEWAY)
```

Performance: IPv4 4-tuple (ATM)



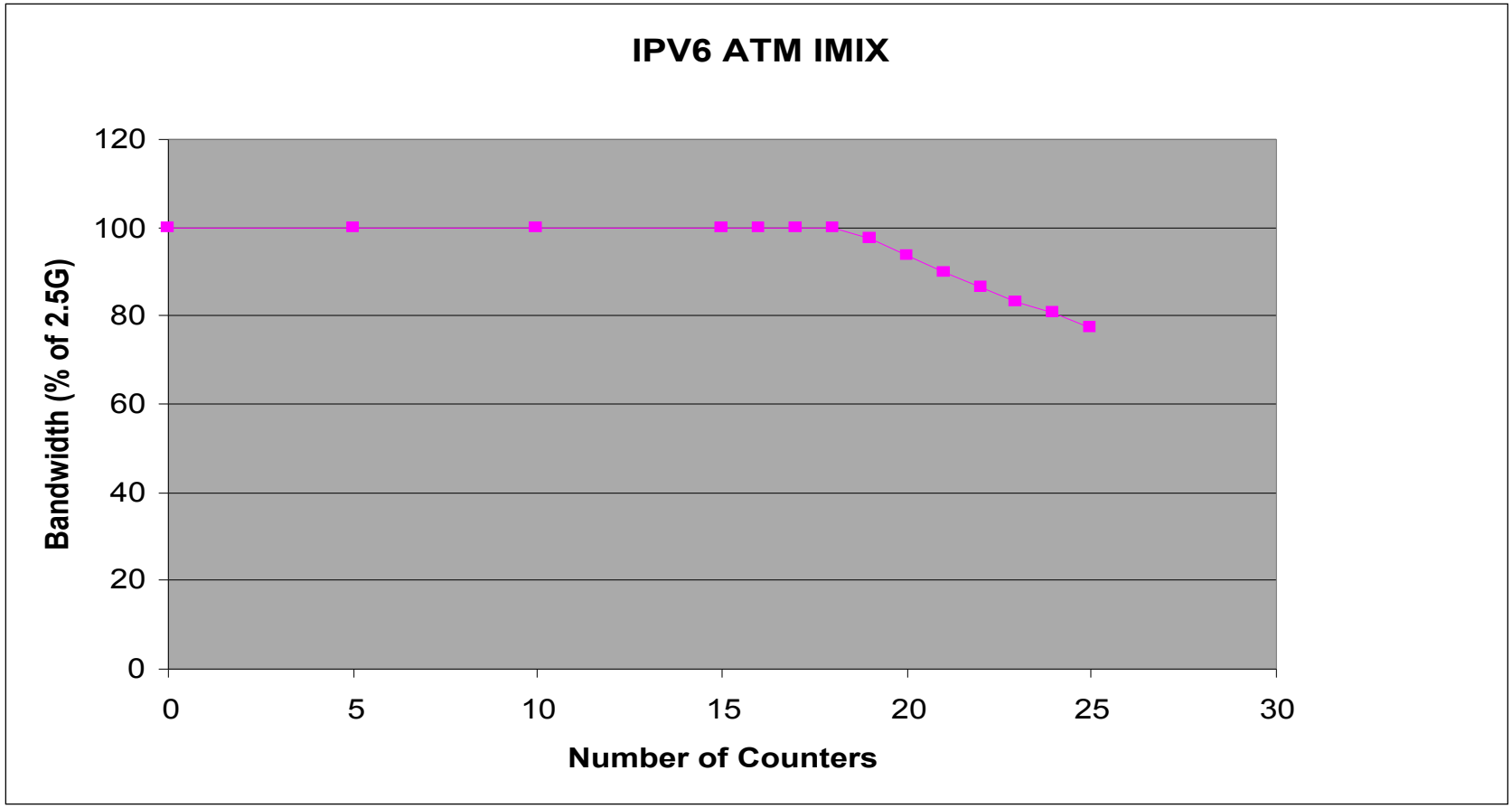
Payload Plus Chipset operating at 133Mhz
IP over ATM over SONET

Performance: IPv4 4-tuple (POS)



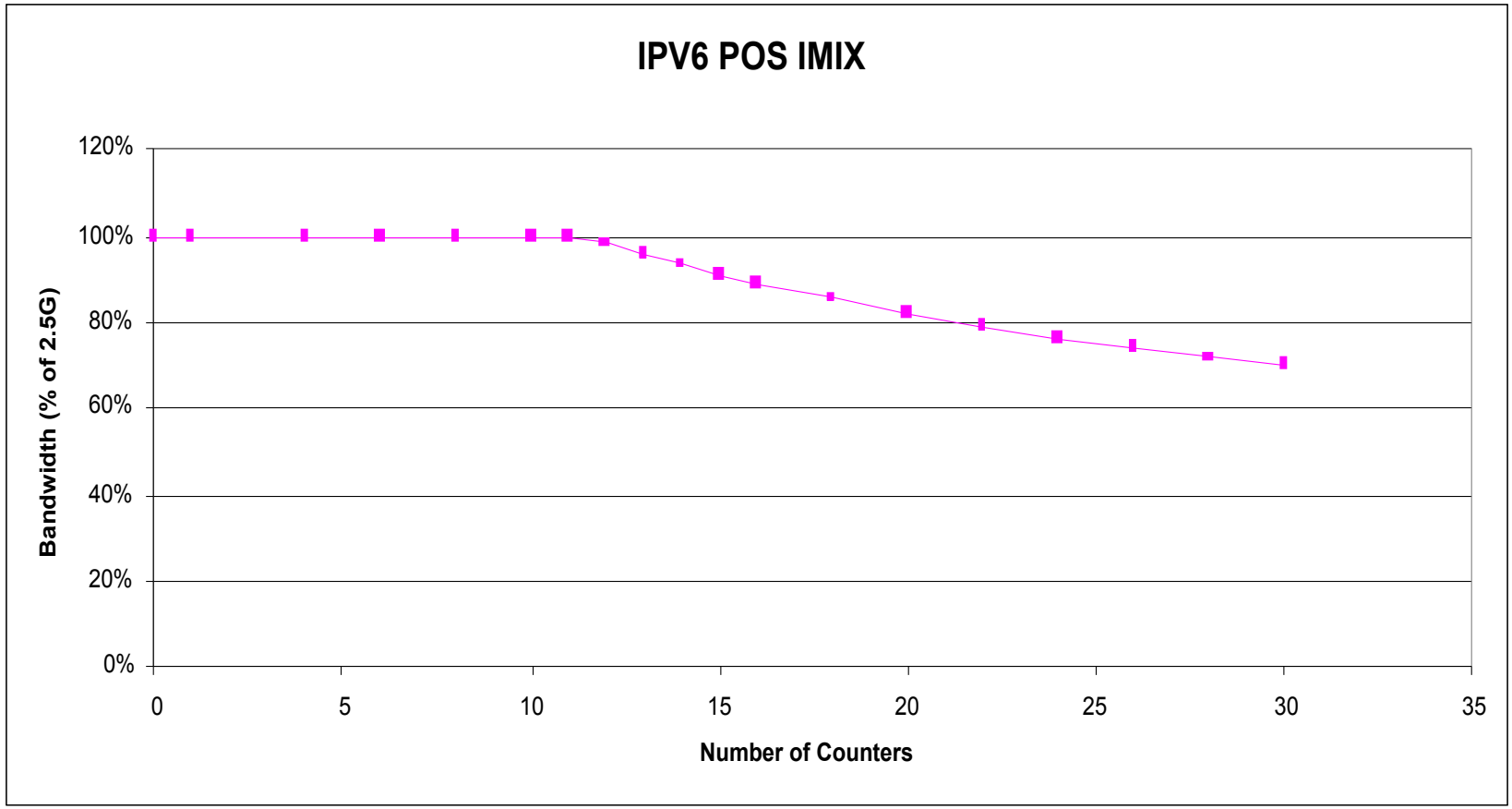
Payload Plus Chipset operating at 150Mhz
IP over PPP over SONET

Performance: IPv6 forwarding (ATM)



Payload Plus Chipset operating at 133Mhz
IMIX = 55% 64byte, 5% 72byte, 17% 596byte, 23% 1520byte

Performance: IPv6 forwarding (POS)



Payload Plus Chipset operating at 133Mhz
IMIX = 55% 64byte, 5% 72byte, 17% 596byte, 23% 1520byte

PayloadPlus™ Summary

- **Value Add Elements**
  - Classification
  - Statistics Gathering
  - Buffer Management
  - Traffic Shaping
  - Data Modifications
- **Hardware Overhead**
  - Linked List Maintenance
  - Queue Maintenance
  - Parallel Processing
  - Pipeline Processing

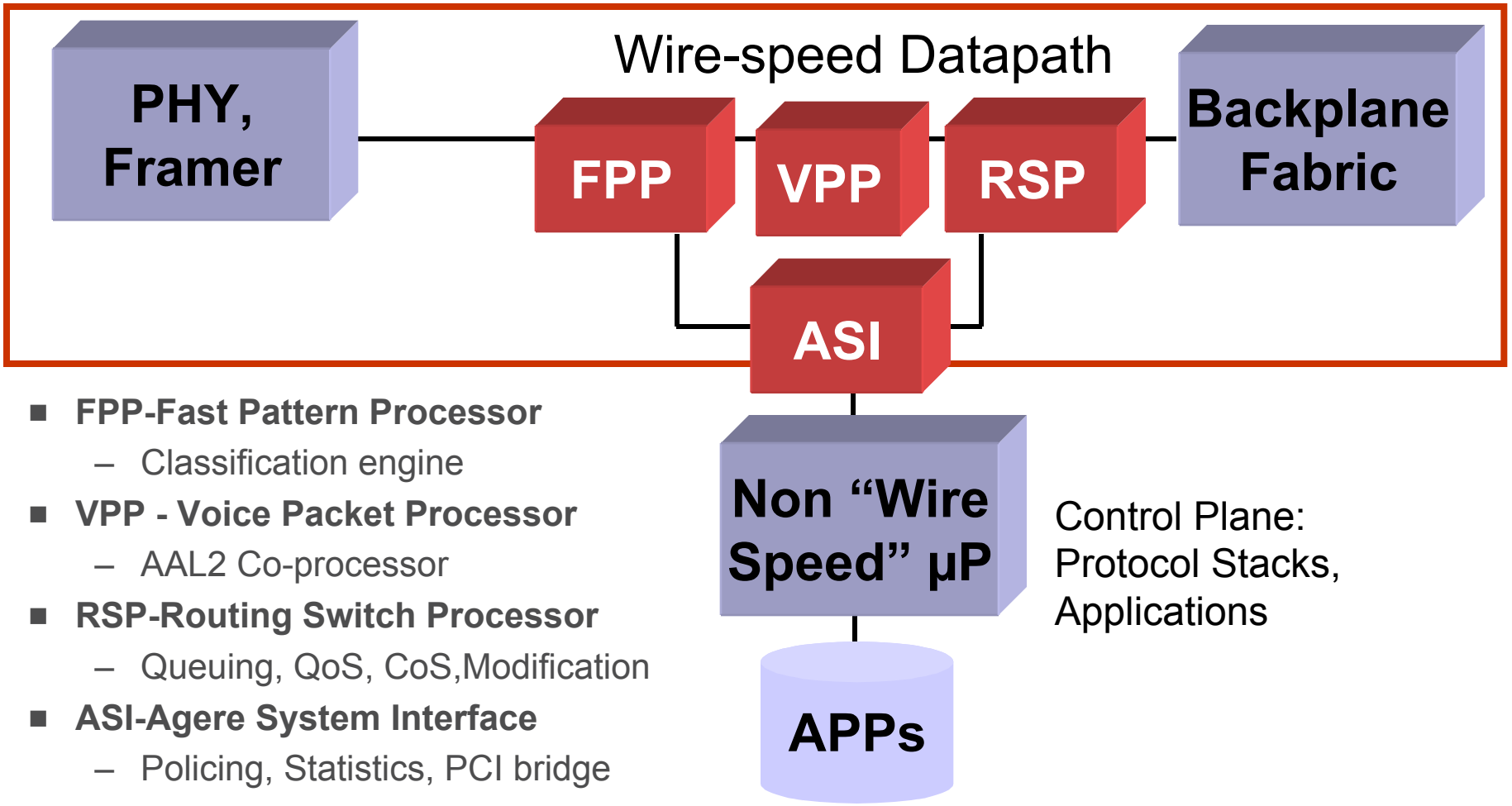
OC-48c Classification, Scheduling, Statistics
133Mhz, 6.2W

agere systems

Backup Slides

Building Blocks for Wire-Speed Datapath

IP, POS, ATM and Frame Relay at OC-48c Rates



- **FPP-Fast Pattern Processor**
  - Classification engine
- **VPP - Voice Packet Processor**
  - AAL2 Co-processor
- **RSP-Routing Switch Processor**
  - Queuing, QoS, CoS,Modification
- **ASI-Agere System Interface**
  - Policing, Statistics, PCI bridge

FPL is to Communication Apps what SQL is to Relational Databases

	FPL	C
Focus	Communications	Generic
Hides parallelism	✓	
Real-time capable	✓	✓
Good for routing/switching	✓	
Good for spreadsheets		✓
Wide variety of prog. styles		✓

System Overview - Applications

- **Building-blocks approach allows flexibility**
  - Many different applications possible
  - Mix-and-match chips for desired functionality