The ARM10 Family of Advanced Microprocessor Cores

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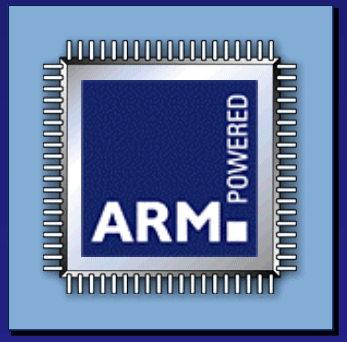
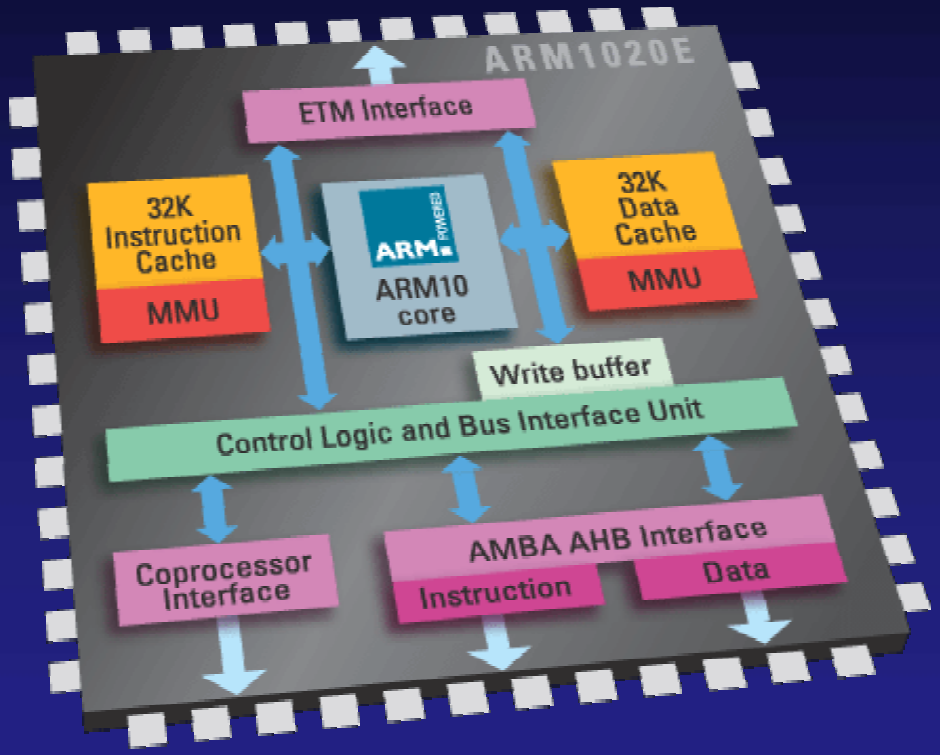


Agenda

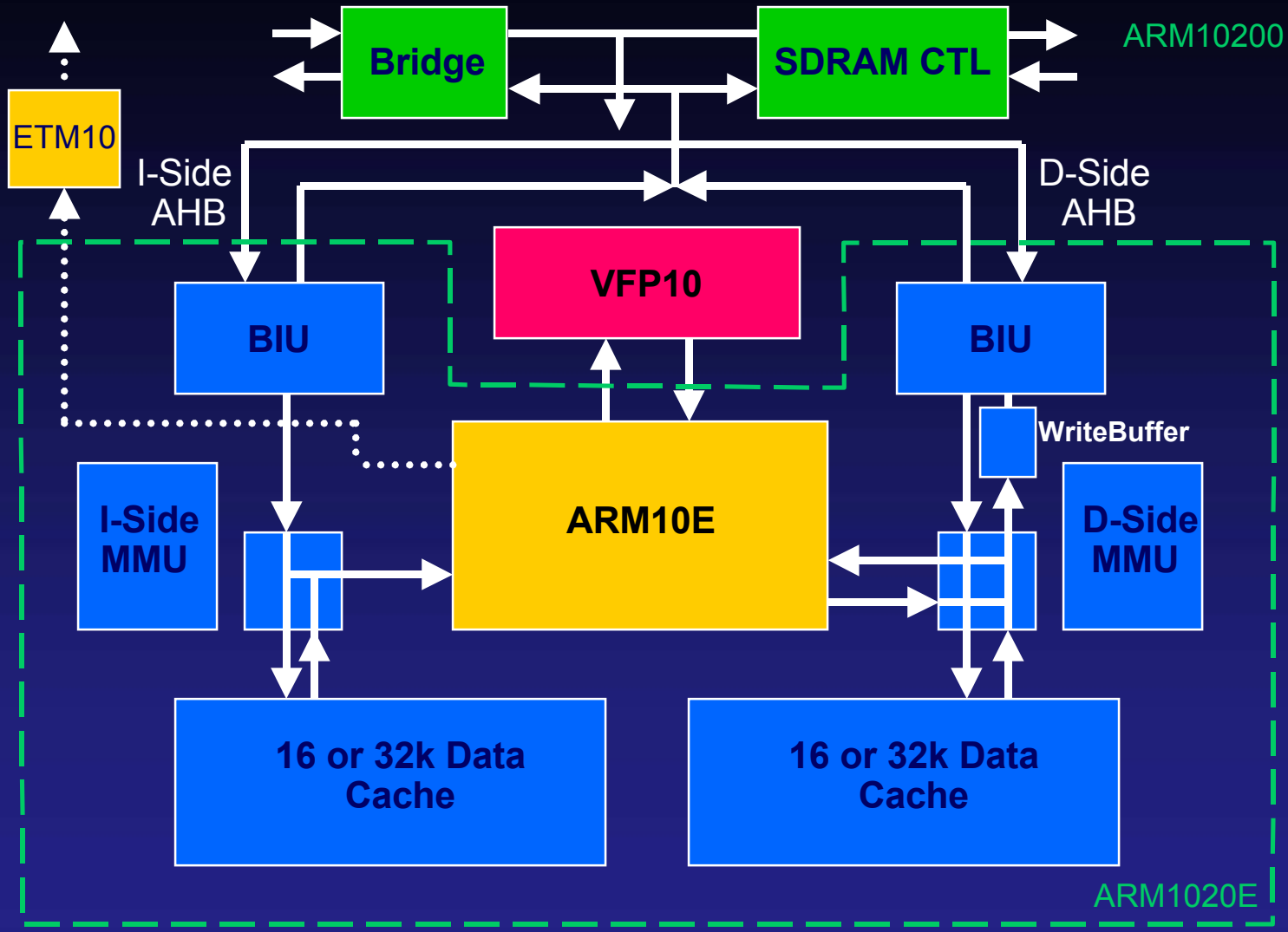


- Design overview
- Microarchitecture
  - ARM10
    - Memory System
    - Interrupt response
3. Power
   - Dynamic power
   - Power down modes
4. VFP10
- ETM10
- Summary

ARM1020E Overview

- Max frequency: 400MHz
  - 0.9*V*, worst case
  - TSMC 0.13um LV
- MIPS/MHz: 1.25
  - 500 MIPS @ 400MHz
  - Dhrystone 2.1
- Active power consumption: 0.51mA/MIPS
  - Room Temp / Typical / 1.1V
  - Average when running Dhrystone 2.1
- Area
  - ARM1022E (2x16KB): 6.9mm^2
  - ARM1020E (2x32KB): 10.3mm^2

ARM10200 System Overview



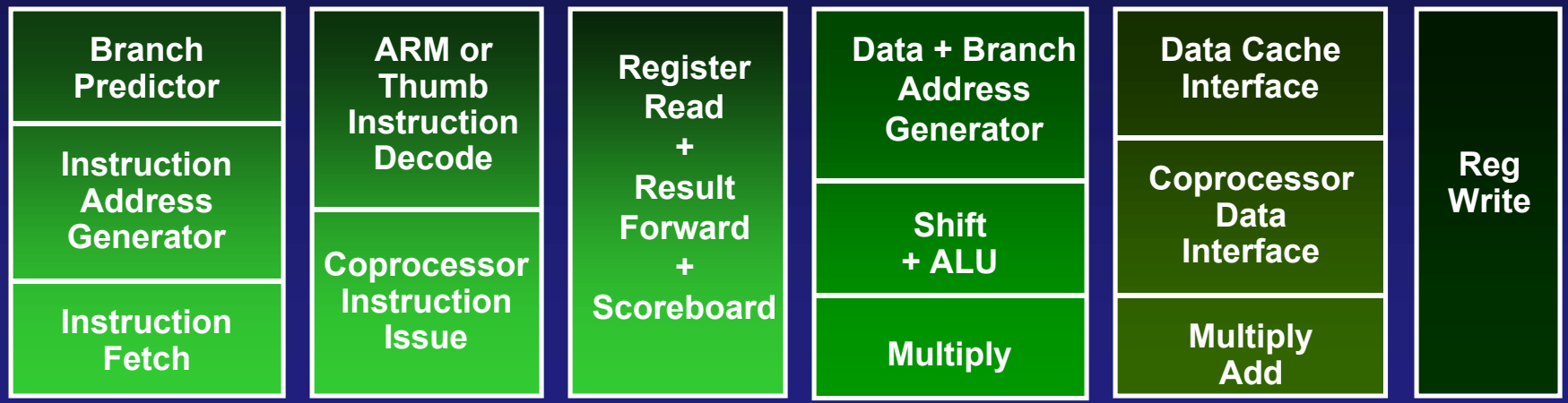
ARM10E Microarchitecture

- 64-bit instruction and data interfaces
- Static branch prediction with branch folding
- Parallel load/store pipeline
  - Dedicated machine for LDM/STM execution; all but the first cycle of these instructions are hidden if no dependencies are encountered
- Parallel execution of multi-cycle coprocessor operations
- Multiply 16 bits per cycle
  - 1-3 cycle throughput and 2-4 cycle latency
  - No data-dependent MUL cycle counts

ARM7 Pipeline versus ARM10

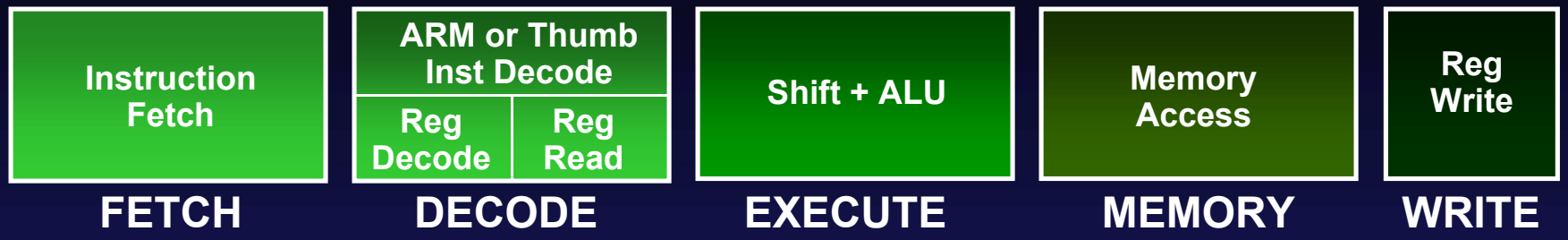
ARM7TDMI

ARM10

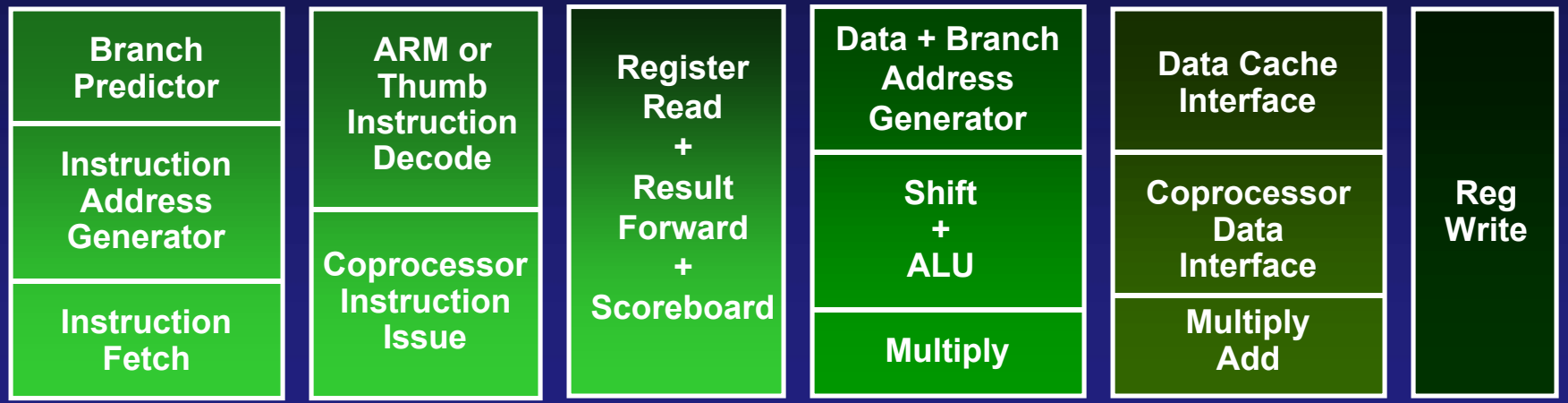


ARM9 Pipeline versus ARM10

ARM9TDMI



ARM10



ARM1020E Memory System

- Instruction & Data Caches
  - 32Kbyte Instruction and Data caches
  - Virtually addressed, 64-way set-associative, 32-byte lines, 64-bit R/W
  - Configurable for Write Through or Write Back operation
  - Lockable by line (1/64 of the cache)
- MMUs
  - Two fully associative (I and D) 64-entry TLBs
  - Lockable by entry
  - Support for software loadable TLBs
- Write Buffer
  - Eight 64-bit entries, plus 32-byte cache line castout buffer
- AHB Bus Interface
  - 64-bit wide data transfers, split transactions
  - Multi-layer AHB support (separate I and D-side system interfaces)

ARM1020E Memory System

Performance features:

- Critical word first
- Non-blocking data cache
- Hit-under-miss (H-U-M)
- Data cache streaming (forwarding) from linefills
- Data cache store merging into linefills

ARM1020E Interrupts

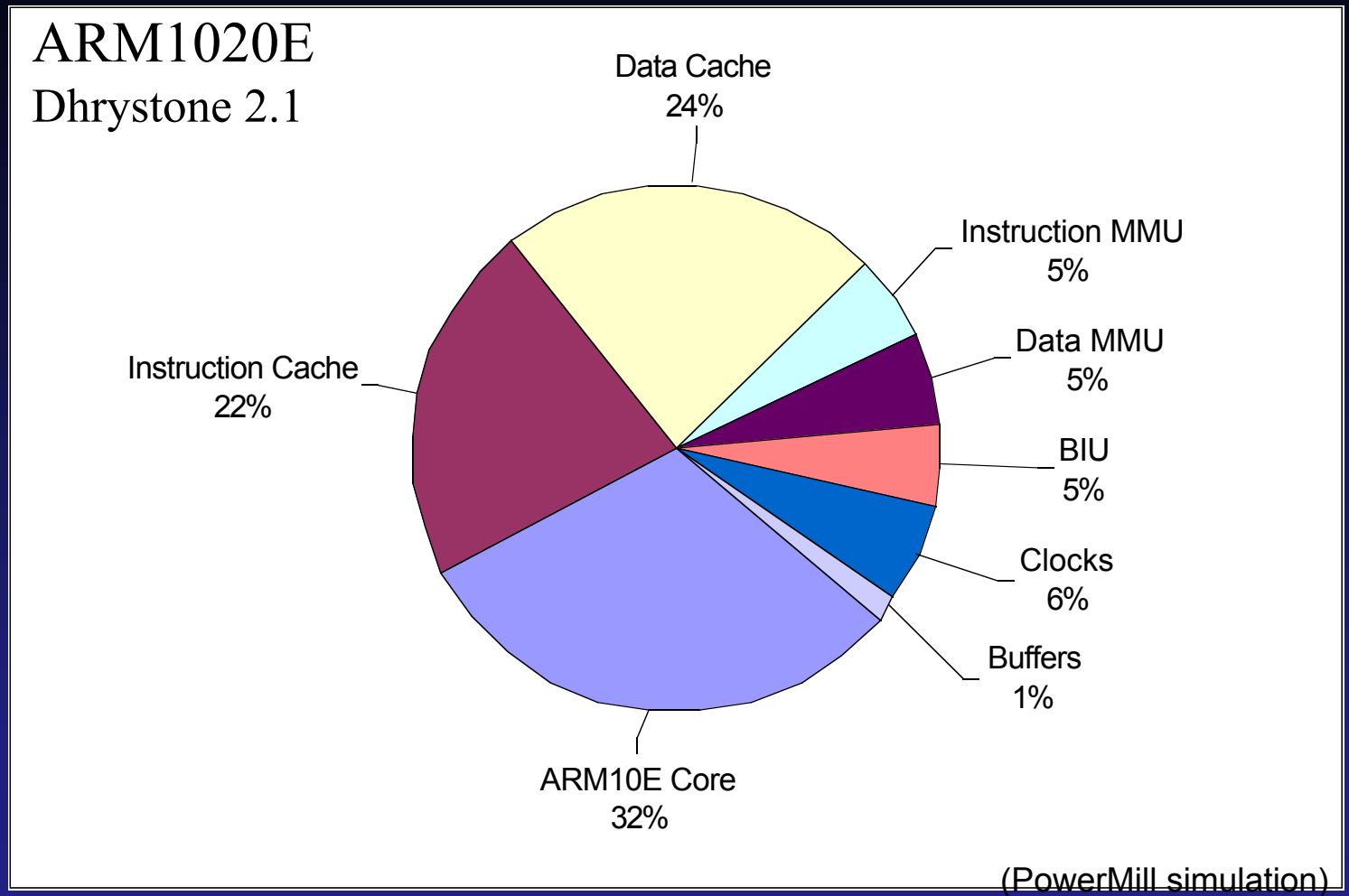
- Interrupts taken in Execute stage
- Fast interrupt mode:
  - First load miss stops further memory ops but not other instructions
  - Limit write buffer depth
- Recommended measures for fast interrupt response:
  - Lock handler code into Caches and TLB
  - Set data cache to write-though (no cast outs)
  - Limit LDM length to 9 registers (spans only 2 cache lines)

ARM1020E Interrupts

- Worst case Interrupt response time to enter handler (G:H Clock 1:1)
  - Worst case of outstanding memory operations (LDM just started)
  - 3 table walks needed (unless TLB locked down)
  - Write buffer full, bus not granted by default

CYCLES (approx)	Fast Interrupt mode	Max Regs in LDM	Write through D cache	TLB locked down
171		16		
148	✓	16		
129	✓	9		
63	✓	16	✓	✓
48	✓	9	✓	✓

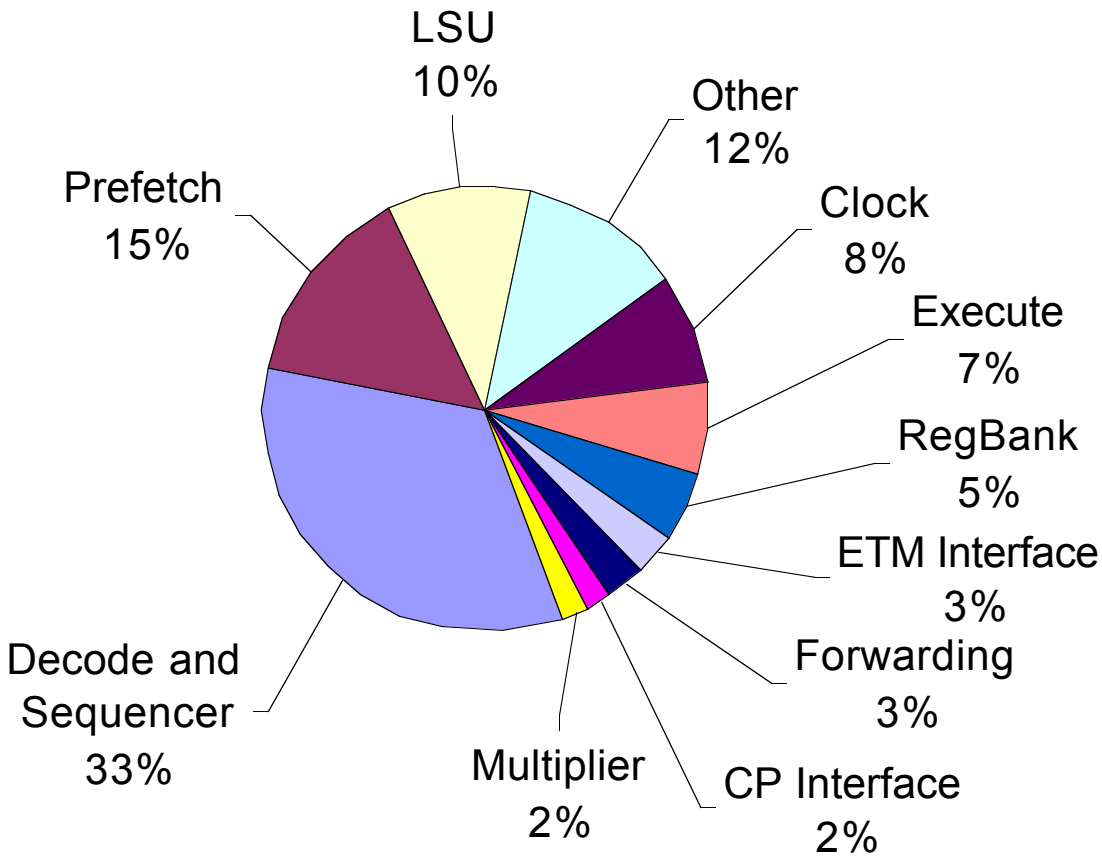
ARM1020E Dynamic Power



ARM10E Dynamic Power

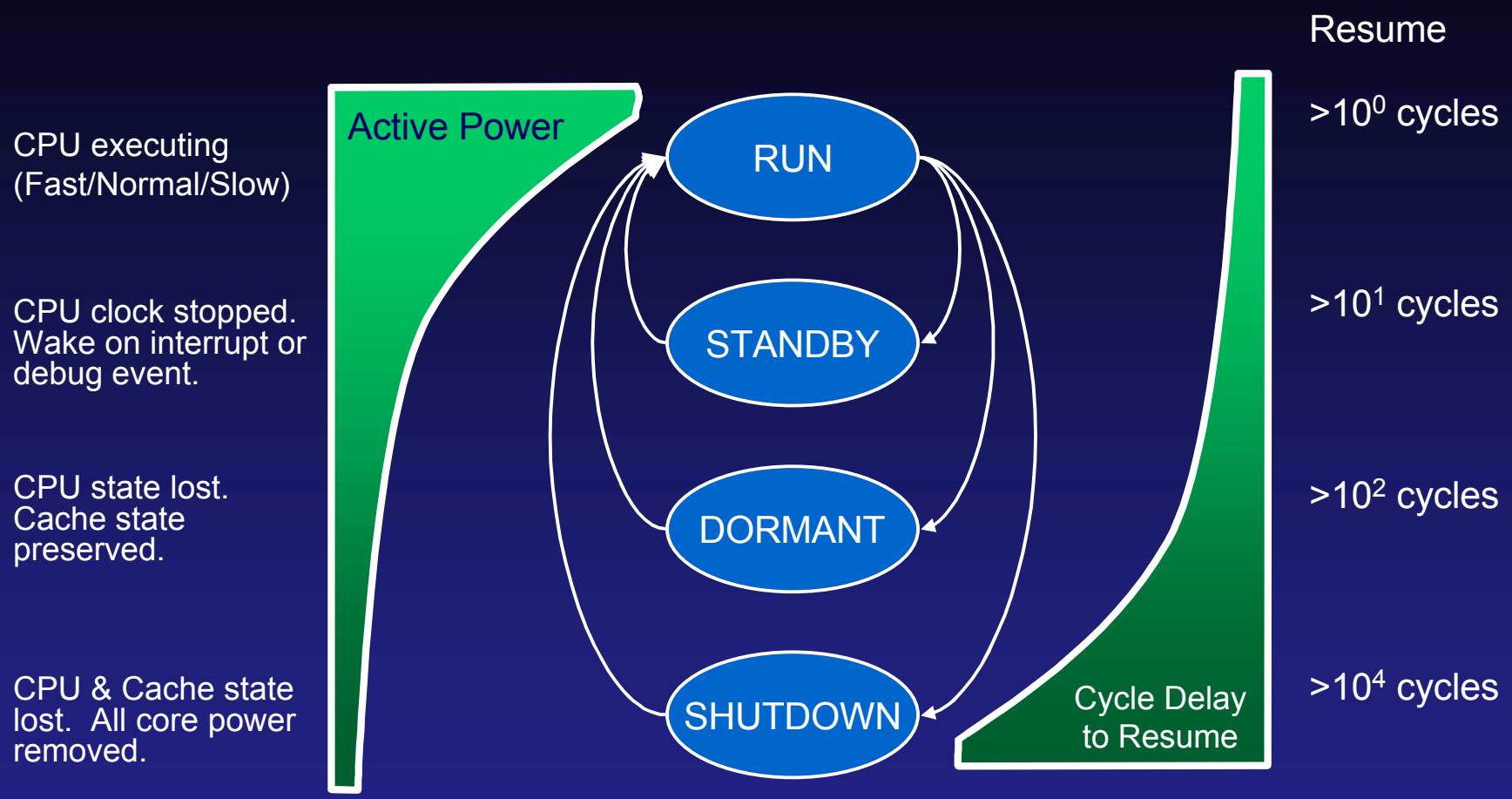
ARM10E Core

Dhrystone 2.1

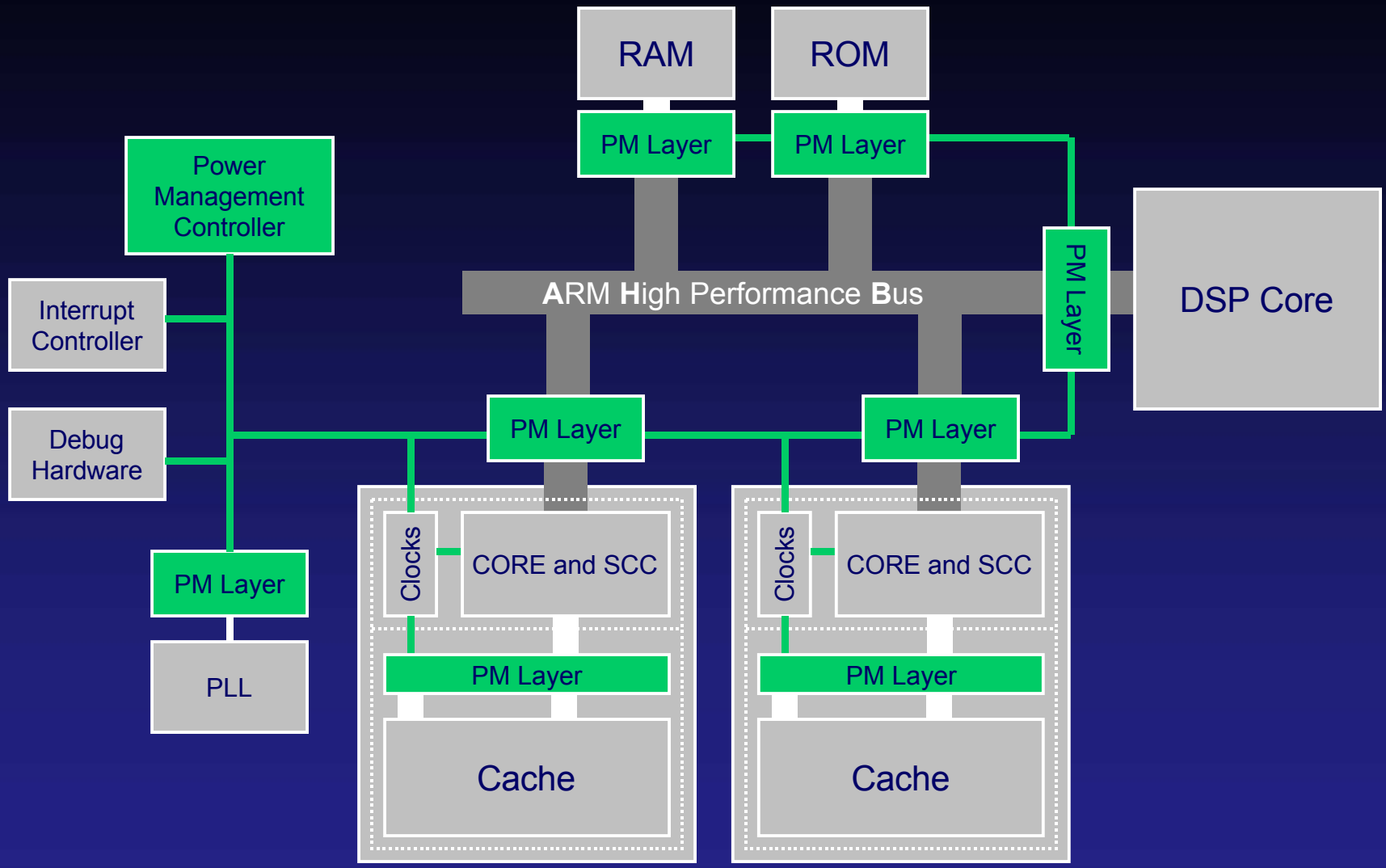


(PowerMill simulation)

Power Down


Resume
CPU executing (Fast/Normal/Slow)
Active Power
RUN
>10^0 cycles
CPU clock stopped. Wake on interrupt or debug event.
STANDBY
>10^1 cycles
CPU state lost. Cache state preserved.
DORMANT
>10^2 cycles
CPU & Cache state lost. All core power removed.
SHUTDOWN
>10^4 cycles
Cycle Delay to Resume

Power Down


RAM
ROM
PM Layer
PM Layer
Power Management Controller
Interrupt Controller
Debug Hardware
ARM High Performance Bus
PM Layer
DSP Core
PM Layer
PM Layer
PM Layer
PLL
Clocks
CORE and SCC
PM Layer
Cache
Clocks
CORE and SCC
PM Layer
Cache

VFP10

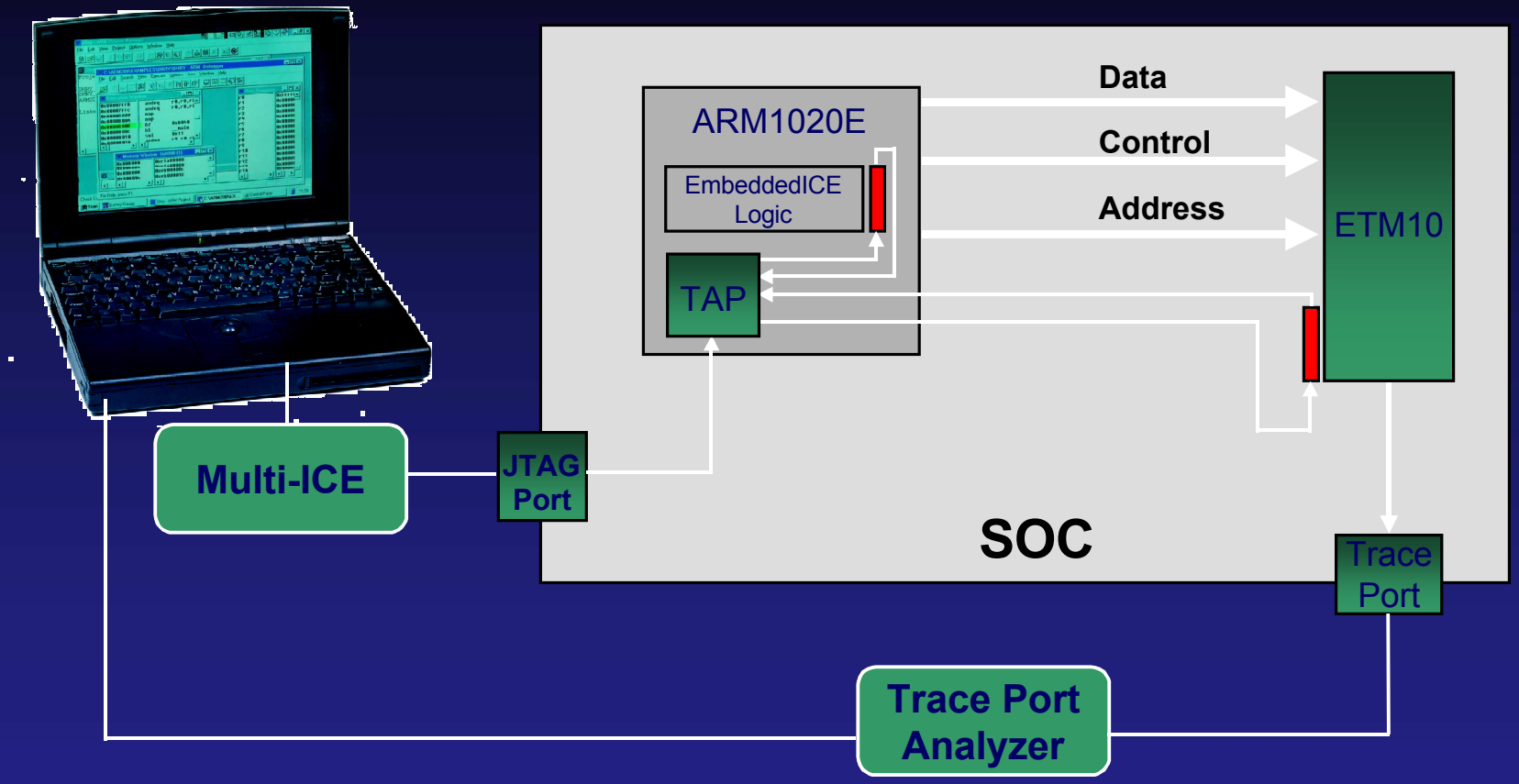
- Full IEEE 754 compliant (with SW support)
- Performance:
  - 236 MFLOPS Linpack (SAxPY) @ 400MHz
  - 400M FIR Taps (800 Peak MFLOPS) @ 400MHz
- Functions supported in hardware
  - Multiply, add, multiply-add, subtract, multiply-subtract, negate, negate multiply, negate multiply-add, negate multiply-subtract, absolute value, compare, convert, divide and square root, conversions
- Most IEEE 754 exceptions handled in hardware
- RunFast mode
  - No trapping enabled (Denormals flush to +0)
  - NaN fractions not propagated (not typical)

VFP10

- 7 Stage pipeline
  - Fetch - Issue - Decode - Execute (E 1) - E 2 - E 3 - E 4/WB
- 32 Single precision / 16 Double precision registers
- High performance short vector operations
  - Register banks operate as hardware circular queues and can be addressed as short vectors (up to 8 values)
- Separate divide/square root unit
  - Supports load/store, and arithmetic operation in parallel with divide/square root operation
- Separate load/store unit
  - Load/store operations may be done in parallel with data processing operations
  - 64-bit unidirectional data interfaces
- Area: ~1.6mm^2 in 0.13um

ETM10

Embedded Trace Macrocell



ETM10

- Full real-time instruction and data tracing
- Monitors the core's *internal* buses
- Zero performance overhead
  - Supports high frequency trace with demux-port
- Configurable synthesis for optimum:
  - area
  - features
  - pin count
- Programmed non-intrusively through JTAG

ARM1020E Family Summary

ARM1020E:

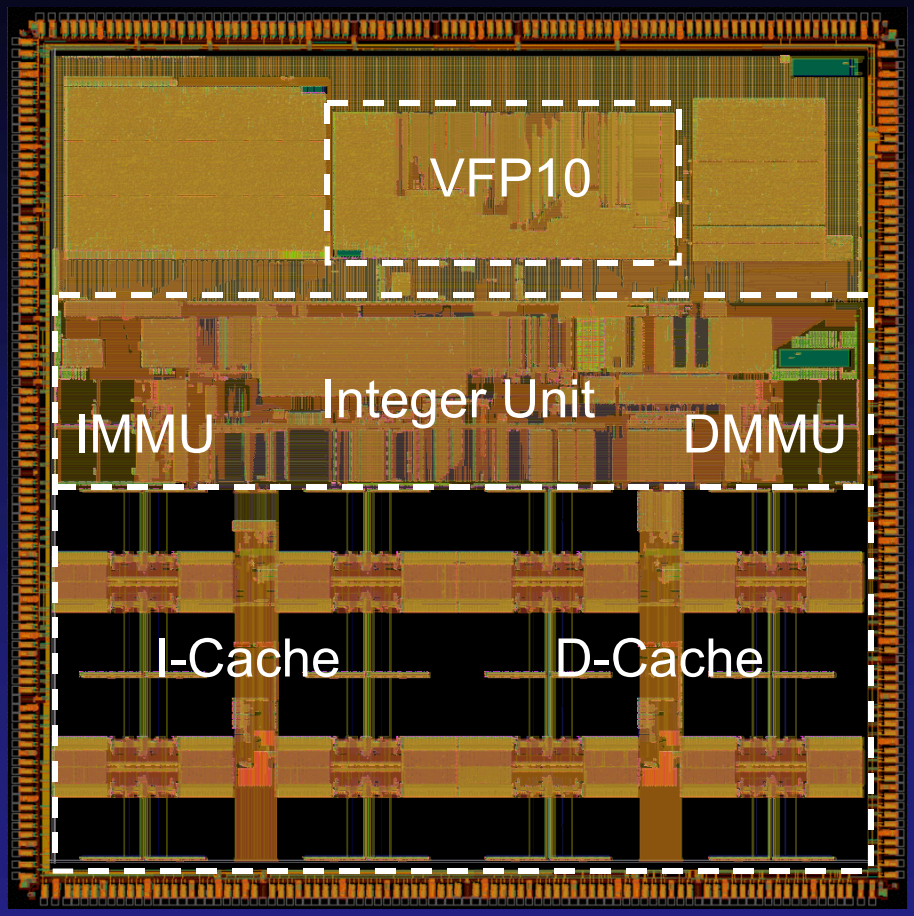
- 500 DMIPS @400 MHz
- 0.51 mA/MIPS
- 10.3mm^2 / 6.9mm^2

VFP10:

- 236 MFLOPS @400MHz
- IEEE 754 Compatible

ETM10:

- Full speed, real time embedded trace



(ARM10200r1)