HOT CHIPS 13 Advance Program

HOT Chips 13

A Symposium on High-Performance Chips – August 19-21, 2001
Memorial Auditorium, Stanford University, Palo Alto, CA

Sunday, August 19, 2001

8:30-12:00 **Morning Tutorial** **Chair: Jan Rabaey**

Jan Rabaey *(U.C. Berkeley)*

Silicon Platforms for the Next-Generation Wireless Systems

Progress in wireless information systems, as envisioned by the 3rd generation and beyond, puts tremendous pressure on underlying implementation technologies. It is commonly observed that the complexity of wireless systems outpaces the technology evolution predicted by Moore's law. As a result, the implementation of future wireless systems requires re-thinking implementation architectures and their relation to the applications.

Wireless infrastructure and mobile components pose a contradictory set of implementation requirements:

- Reducing the cost in a multi-standard, evolutionary and adaptive environment requires flexible and evolvable solutions, which are often translated into software-programmable architectural implementations
- Extremely high performance and energy-efficiency is needed for state-of-the art wireless algorithms and networks.

The latter requirement is more easily satisfied by semi-custom solutions, but these tend to lack the required flexibility. As a result, the architectural community has explored a variety of novel architectures and implementation approaches, such as VLIW and reconfigurable processors, and processors with accelerators .

This tutorial will discuss: opportunities offered by the progress in semiconductor technologys, an exploration of the needs of future wireless systems, an overview of the different solutions, and clear metrics in how to evaluate and compare the options. Actual values for metrics such as flexibility, cost, performance and energy-efficiency will be offered with the aid of some real benchmark examples.

12:00-1:30 **Lunch**

1:30-5:00 **Afternoon Tutorial** **Chair: Alan Smith**

Rob A. Rutenbar, *(Carnegie Mellon/Neolinear)*

Ramesh Harjani, *(Univ. of Minnesota)*

Design at the Leading Edge of Mixed-Signal ICs

Most modern System-on-Chip (SoC) designs are mixed-signal designs. This should come as no surprise: a few million gates worth of fast digital computation on a chip is much more useful if it can communicate with the external world, and the world is a continuous-valued analog place. Since analog circuits exploit rather than avoid the low-level physics of the fabrication process, they remain painful to design, to validate, and to reuse. Classical "hand-crafted" analog design (one transistor at a time) is incompatible with our desire to integrate more analog on chip, and to design each chip quickly. This tutorial will survey progress in two areas: how we design these chips, and what we can design into these chips.

The first half will explain design methodology for high-end analog, including a beginners overview of why analog is not like digital design: why it's weird, where it's weird, how designers cope. We focus on recent developments in the quest for practical analog intellectual property (IP). Currently, if you want a CPU core for your SoC, you can buy one. However, if you want a customized wireless front-end for your SoC, you'll need to build one yourself. This is a huge roadblock to any vision of "assemble-able" systems with reusable pieces. We describe emerging industrial approaches, including the appearance of commercial analog synthesis tools.

The second half of the session will focus on wireless IC design. Advanced CMOS and SiGe processes are making sophisticated single-chip radio frequency (RF) designs a reality. But the style of such designs changes radically as we move from separate discrete components to a single SoC. We focus on the architecture of wireless transceivers, what the analog components do, and what new capabilities are possible in tomorrow's designs. We also outline circuit-level problems remaining in the quest for a single "universal" wireless front-end.

This tutorial is intended for both the digitally-inclined (who wonder why analog folks are always so cranky), and the analog-inclined (who think digital folks have life way too easy).

5:00-6:00 **Wine and Cheese Reception**

The HOT Chips 13 symposium is sponsored by the Technical Committee on Microprocessors and Microcomputers of the IEEE Computer Society

IEEE COMPUTER SOCIETY

Visit our Web Pages for Registration and Conference Details

http://www.hot.org **http://www.hotchips.org**

Monday, August 20, 2001

8:45- 9:00 **Welcome, Opening Remarks**
General Chair: Lily Jow
Program Co-Chairs: John Kubiatowicz, Andy Wolfe

9:00-10:30 **Session 1: Microprocessors I**
Session Chair: Chuck Moore

- **R18000™, The latest SGI™ Superscalar Microprocessor,** Kenneth Yeager, Mahdi Seddighnezhad, *Silicon Graphics*
- **The ARM10 family of Advanced Embedded Microprocessor Cores,** Stephen Hill, *ARM, Inc.*
- **Power4 System Design for High Reliability,** Douglas Bossen, Joel Tendler, Kevin Reick, *IBM*

10:30-11:00 **Break**

11:00- 12:30 **Session 2: Embedded Solutions**
Session Chair: Andrew Wolfe

- **Rapid Application Optimization Using Configurable Processor Extensions,** Michael Carchia, Albert Wang, *Tensilica*
- **SH-5: A First 64-bit SuperH Core with Multimedia Extension,** Fumio Arakawa, *Hitachi Ltd.*
- **Gekko: A PowerPC compatible processor supporting high-performance 3D graphics,** Peter Sandon, Jay Heaslip, George Rohrbaugh, Bruce Singer, Tim Von Reyn, *IBM*

12:30- 1:40 **Lunch**

1:40- 2:40 **Keynote: Atiq Raza,** *Raza Foundries*
Silicon for a 10 Gigabit-per-second connected world

2:40- 3:00 **Break**

3:00- 4:30 **Session 3: Integrated Communications & Networking**
Session Chair: Forest Baskett

- **A Mobile Station Modem Chip for WCDMA,** David Hansquine, *Qualcomm*
- **nFlex: A Broadband Wireless Communications Processor,** Sanjay Vishin, Srinivas Lingam, *nBand Communications*
- **Mellanox InfiniBridge: An InfiniBand Switch and 10Gbs Channel Adapter,** Chris Eddington, *Mellanox Technologies*

4:30- 5:00 **Break**

5:00- 6:30 **Session 4: High Speed Communications**
Session Chair: Jan Rabaey

- **A 2.5Tb/s switch core with LCS interface,** Nick McKeown, Costas Calamvokis, Shang-tse Chuang, *PMC-Sierra*
- **A 5 GB/s Adaptively Equalized Multilevel Transceiver Enabling Multi-terabit Backplane Connectivity,** Jim Gorecki, Paul Nahi, *Accelerant Networks*
- **A Single-Chip Terabit Switch,** Fred Heaton, Bill Dally, Wayne Dettloff, John Eyles, Trey Greer, John Poulton, Teva Store, Steve Tell, *Velio Communications*

6:30- 7:45 **Dinner**

7:45- 9:00 **Panel: My network processor is better than your network processor!**
Panel Moderator: Linley Gwennap, The Linley Group
Panellists:

Anthony Gallo	Silicon Access
Andy Gottlieb	AMCC
David Kramer	Agere
Ravi Sabhikhi	IBM
TBA	

Tuesday, August 21, 2001

8:30- 10:30 **Session 5: Network Switch Technology**
Session Chair: John Wawrzynek

- **Payload+: Fast Pattern Matching & Routing for OC-48,** David Kramer, Roger Bailey, David Brown, Sean Mcgee, Jim Greene, Robert Corley, David Sonnier, *Agere Systems*
- **Fabr-IC: Single-Chip Gigabit Ethernet Switch w/ Integrated Memory,** Dave Brown, Chris Holmes, *MOSAID*
- **Ultra high performance network memory,** David Sherman, *Alpine Microsystems*
- **Tyrant: A High Performance Storage over IP Switch Engine,** Stuart Oberman, R. Mullendore, K. Malik, A. Mehta, K. Schakel, M. Ogrinc, D. Mrazek, *Nishan Systems*

10:30-11:00 **Break**

11:00-12:30 **Session 6: *Storage***
Session Chair: Howard Sachs

- **1.8-inch Super Small Slim HDD,** Yasuichi Hashimoto, *Toshiba*
- **Microdrive: High Capacity Storage for the Handheld Revolution,** Thomas Albrecht, *IBM*
- **DataPlay, a New Technology for Information Distribution,** David Davies, *DataPlay Inc.*

12:30- 1:40 **Lunch**

1:40- 2:40 **Keynote: Mark Dean,** *IBM Fellow, VP of Systems Research*
Trends Impacting Computing Systems Design and the IT Industry

2:40- 3:00 **Break**

3:00- 4:30 **Session 7: Chip Multiprocessors**
Session Chair: John Kubiatowicz

- **53 GOPS Programmable Vision Processor For Processing, Coding-Decoding and Synthesizing of Images,** Ulrich Ramacher, W. Raab, N. Bruels, U. Hachmann, C. Sauer, A. Schackow, J. Gliese, J. Harnisch, M. Richter, E. Sicheneder, *Infineon*
- **A MIMD-based Multi Threaded Processor,** Falk Lesser, J. de Cuveland, V. Lindenstruth, C. Reichling, R. Schneider, M.W. Schulz, *Kirchoff Institute for Physics*
- **The Raw Processor: A Composeable 32-Bit Fabric for Embedded and General Purpose Computing,** Michael Taylor, J. Kim, J. Miller, F. Ghodrat, B. Greenwald, P. Johnson, W. Lee, A. Ma, N. Schnidman, D. Wentzlaff, M. Frank, S. Amarasinghe, A. Agarwal, *MIT*

4:30- 5:00 **Break**

5:00- 6:30 **Session 8: Microprocessors II**
Session Chair: John Shen

- **Itanium Processor Performance Insights from the IMPACT Compiler,** John Sias, M. Merten, E. Nystrom, R. Barnes, J. Matarazzo, C. Shanno Wen-mei Hu, *Univ. of Illinois*
- **The Intel® 870 Family of Enterprise Chipsets,** Faye Briggs, M. Cekleov, K. Creta, M. Khare, A. Kumar, S. Kulick, L. Looi, C. Natarajan, L. Rankin, *Intel*
- **The Pentium® 4 Processor,** Doug Carmean, Mike Upton, Glenn Hinton, Dave Sager, Darrell Boggs, Patrice Roussel, *Intel*

6:30 -6:45 **Closing Remarks, Awards**

Visit our Web Pages for Registration and Conference Details
http://www.hot.org **http://www.hotchips.org**

HOT Chips Conference Registration Form

Web registration is preferred! You can register on our secure web server via:
http://www.hotchips.org

On or before August 6th, you can also register by faxing this form to: **+1 (509) 479-1966** or by mailing it to: **Hot Chips Registration P.O. Box 1981 Los Altos, CA 94023, USA**
Confirmation of registration will be sent by e-mail.

Registrations received after August 6, 2001 may not be acknowledged and may require on site registration.

We are sorry that we cannot accept phone registrations.

Forms must be received before or on July 29, 2001 for advanced rates to apply.

Refund requests must reach us on or before August 6th, and are subject to a $50 refund fee.

Students are required to show valid picture ID cards.

For answers to questions about registration, contact us by email at:
hotchips2001@hotmail.com

For other information, contact us by email at: **info@hotchips.org**

Conference registration includes:

- Attendance
- One copy of notes
- Monday and Tuesday luncheons
- Coffee breaks
- Sunday afternoon wine and cheese reception
- Monday HOT Chips evening dinner and Panel
- Monday and Tuesday Parking

Tutorial registration includes:

- Attendance for both Morning and Afternoon tutorials
- One copy of notes
- Sunday Luncheon
- Coffee breaks
- Sunday afternoon wine and cheese reception

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Membership ☐ IEEE/CS ☐ ACM ☐ Non-member ☐ Student* (* ID required)

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If I cancel my registration after Aug. 6, 2001, I agree to pay the entire bill.

Fees: Please CIRCLE Appropriate Fees

	Advance (on/before 7/29)			Late (after 7/29)		
	Tutorials	Conf. only	Both	Tutorials	Conf. only	Both
Member	$ 75	$200	$275	$150	$330	$480
Non-Member	$ 75	$275	$350	$150	$410	$560
Student Member	$ 75	$ 75	$150	$150	$100	$250

HOT CHIPS 13

Special Event: Tour of Computer Museum History Center Collection at Nasa Ames- Weds Aug. 22, 10am-1pm.

Bus transportation and snack included. **Attendance is limited, preregistration required** **Valid ID will be required to enter NASA.** **Email: machus@aol.com for details and schedule.**	**$25**

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Advance Program

HOT CHIPS 13

August 19-21, 2001

Memorial Auditorium - Stanford University

***For housing information, visit our web page:* http://www.hotchips.org**

Location:
Hot Chips and Hot Interconnects will be held in Memorial Auditorium on the Stanford University campus, Palo Alto, California approximately 24 miles from San Francisco airport, and 15 miles from San Jose airport.

Directions, Maps:
From San Francisco: take Highway 101 south. ***From San Jose***: take Highway 101 north.
Exit 101 at Embarcadero Rd. (west) and drive 3 miles until you enter Stanford campus on Galvez St.
Keep to the left on Galvez, then turn right at Campus Drive. Parking is between Galvez and Palm Dr.
Walk along Galvez to the end, then turn right for Memorial Auditorium, opposite Hoover Tower.

Mass transit information is available at **http://www.transitinfo.org/**

Maps of Stanford campus and surroundings are at **http://www.stanford.edu/home/visitors/maps.html**

Weather: Mid-August is typically in the 80s (F) and sunny during the day.
Nights are much cooler; a light jacket or sweater is appropriate.

Housing:
Hotel information for the area is available at **http://www.stanford.edu/dept/hds/scs/individuals/hotelmotel.html**
The Sheraton, Westin, and Stanford Terrace Inn are the closest hotels to campus. Reservations well in advance are advised.
On campus housing is available in student residences and can be arranged by contacting the Stanford Summer Conference Office at **(650)725-1429** or **summerhousing@conferences.stanford.edu** .
Rates are $45 per night for single occupancy and $31.75 per night per person for shared occupancy.