The Itanium™ Processor Cartridge

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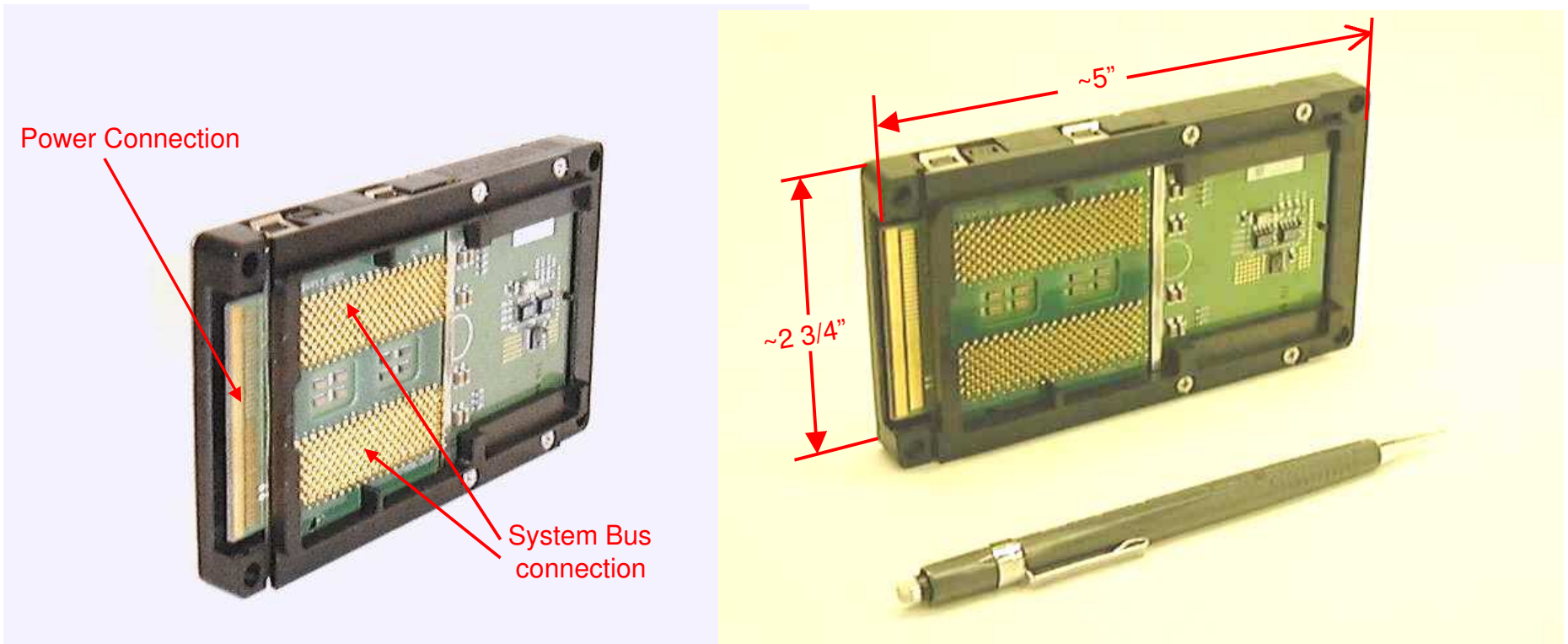
Santa Clara, CA

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Agenda

- Feature Overview
- Cartridge Form Factor Considerations
    - System topology
- System Bus
- Si Packaging
- Power Delivery
- Thermal Attributes
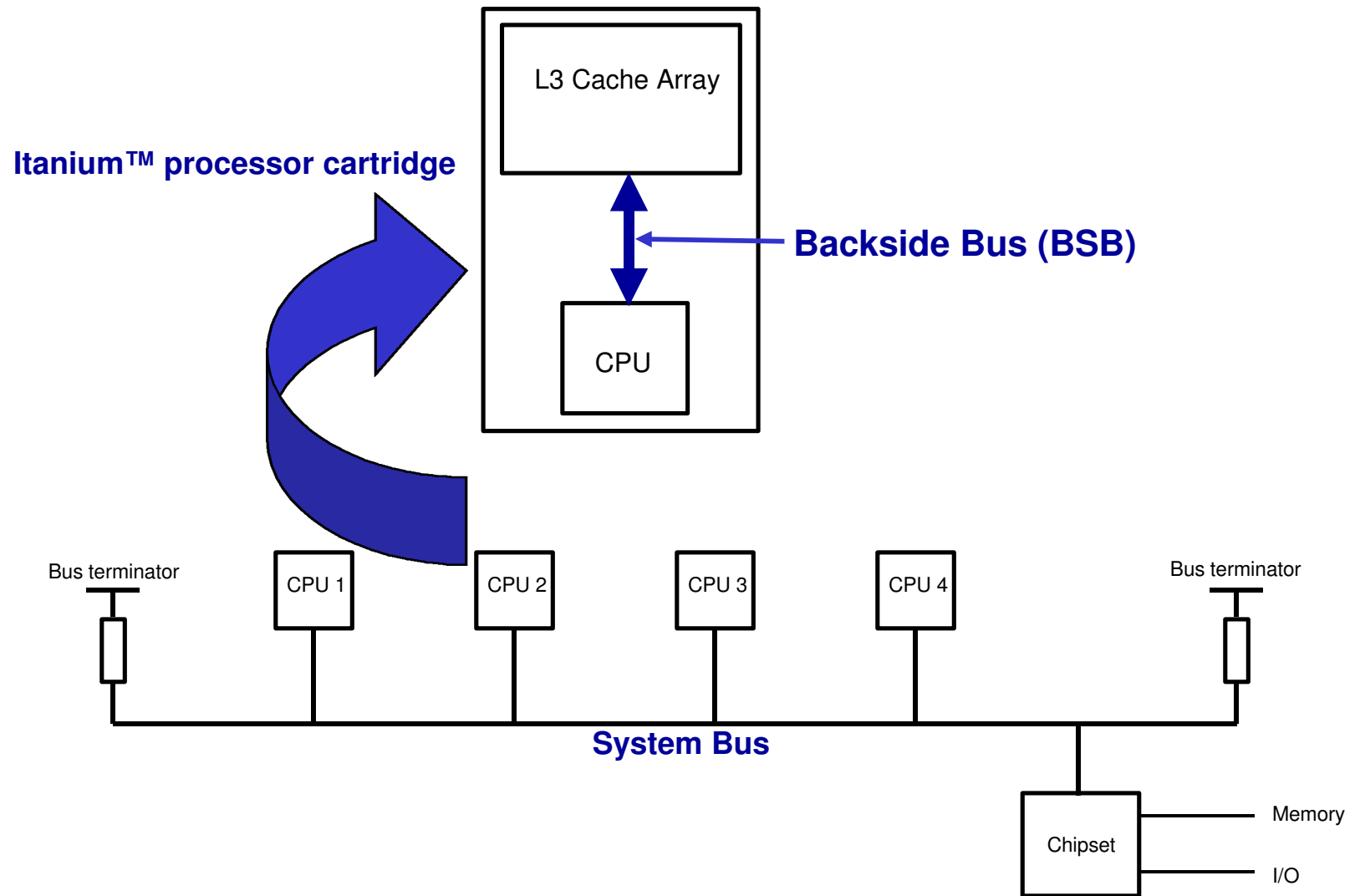- Cache Organization
- Electrical Simulation Environment

Itanium™ Processor Cartridge Overview

- A packaging optimization for electrical and thermal performance in a multiprocessor server environment

- ~3" x 5" cartridge contains the Itanium™ Processor and up to 4 megabytes of external L3 cache

- A glueless bidirectional multidrop system bus (CPU to chipset connection)

  – Continuous data transfers at 266 MHz Mega-transfers per second (MT/s) for a total bandwidth of ~2.1GB/s

- ~13GB/sec 4M external L3 cache operates at the processor's internal (core) clock rate of 800MHz

  – The processor to L3 connection is the BackSide Bus (BSB)

- Power delivered through a custom connection with separate voltages for the 0.18μm CPU and the 0.25μm custom cache devices

- An Integrated vapor chamber thermal lid for heat transfer

- System management features such as temperature monitoring and cartridge identification information

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Itanium™ Processor Cartridge Form factor

Power Connection

System Bus connection

~5"

~2 3/4"

Cartridge Bus connections

L3 Cache Array

Itanium™ processor cartridge

Backside Bus (BSB)

CPU

| Bus terminator | CPU 1 | CPU 2 | CPU 3 | CPU 4 | Bus terminator |

System Bus

Chipset

Memory

I/O

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Physical Topology Considerations

- System Bus & BSB influenced the physical arrangement of the cartridge and the internal die placement more than any other factors

- I/O signals are physically arranged into a pin grid array (PGA) allowing the cartridge to lay flat on the motherboard (system bus will have minimal overall length)

- System topology promotes two cartridges placed next to each other and duplicated on both sides of the motherboard

- Cartridge topology minimizes system bus stub length by positioning the CPU die directly over the pin field array and carefully positioning I/O buffers to align with external Interconnect

- L3 cache silicon is clumped to one end making the on-cartridge BSB electrically short and minimizing the cartridge width

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Critical System Bus Parameters
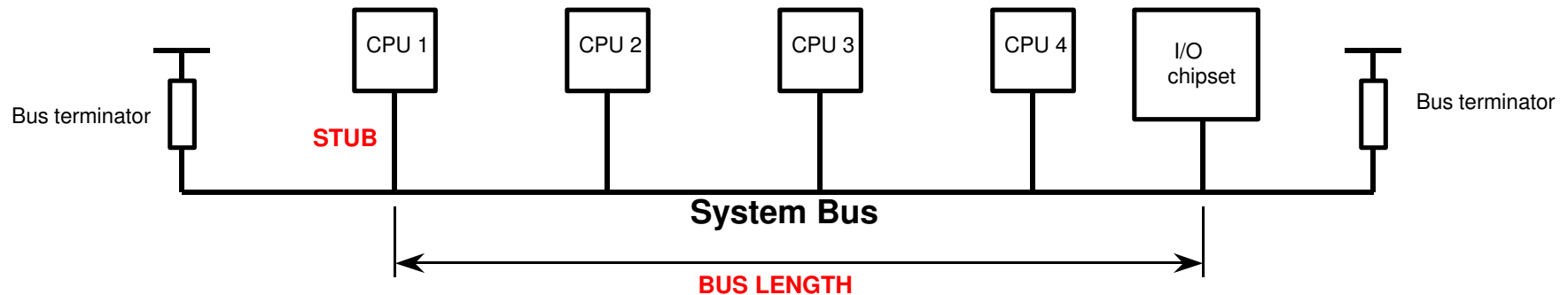
- Critical electrical parameters for a high performance System Bus
    1. Stub length. Distance from CPU to actual bus wire
    2. Overall bus length
- Horizontal processor card placement minimizes stub length
    – CPU FSB die I/O cell placement matches processor card connector pin placement
- Double sided processor card mounting minimizes bus length
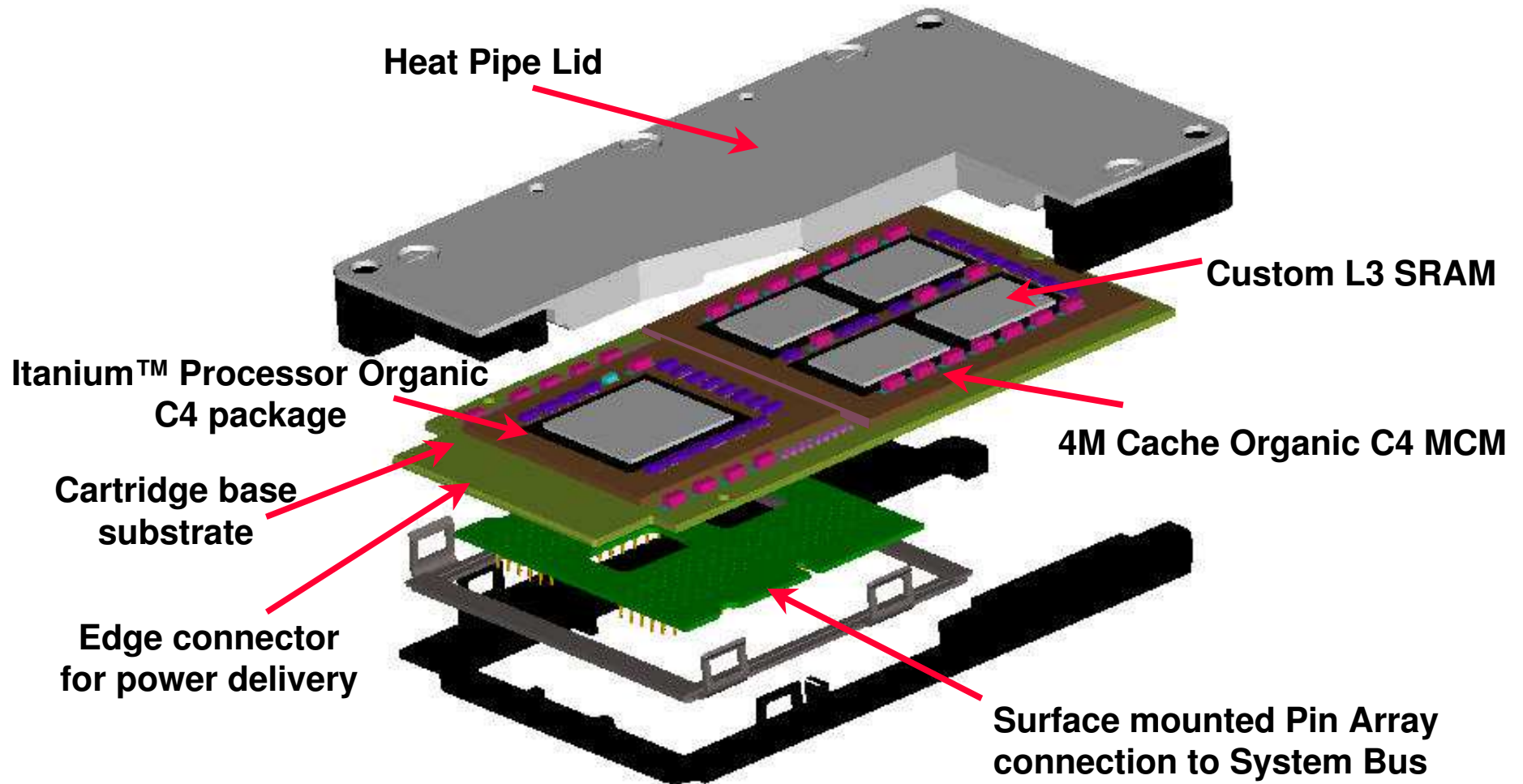
Itanium™ Processor System Bus Topology
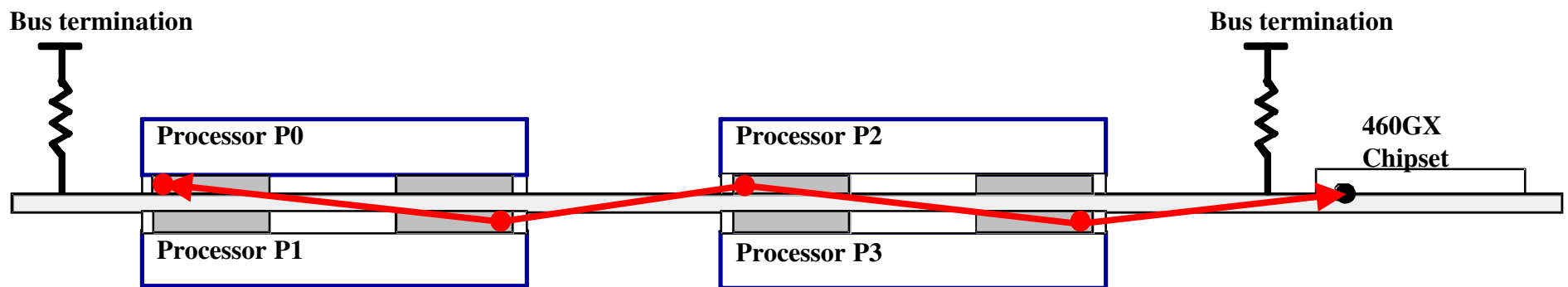
4 Itanium Cartridges double side
mounted to a motherboard

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Packaging

- Itanium™ Processor cartridge contains three substrates
  - Base substrate
    - Twelve alternating layers of impedance controlled interconnect and reference planes
  - CPU package substrate
    - CPU is attached to a 42.5^2mm ten layer organic land grid array (OLGA) package using C4 technology (Controlled Collapsed Chip Connection)
    - CPU OLGA is solder attached to the base substrate as a ball grid array (BGA)
  - Cache MCM substrate
    - Two die or four die multichip module (MCM)
    - Cache devices are C4 attached to a ten layer OLGA. Cache MCM is solder attached to the base substrate as a large BGA
  - All of these substrates contain a significant number of capacitors used for voltage decoupling purposes
    - Essential for a core speed 4M cache bus

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Itanium™ Processor Cartridge Components

Heat Pipe Lid

Custom L3 SRAM

Itanium™ Processor Organic C4 package

4M Cache Organic C4 MCM

Cartridge base substrate

Edge connector for power delivery

**Surface mounted Pin Array connection to System Bus**

Power Delivery

- Cartridge power delivered through a dedicated edge connection that plugs to a custom Power Pod DC -DC converter (voltage regulator)

- The Itanium™ Processor Power Pod contains two power converters; one for each Si voltage

- Power planes of the cartridge base substrate extend into the power converter

- Entire power delivery loop inductance reduced to just a few hundred picohenrys

- Large power currents are eliminated from signal returns paths

Itanium™ Processor Voltage Regulator Module (Powerpod)

Powerpod heatsink
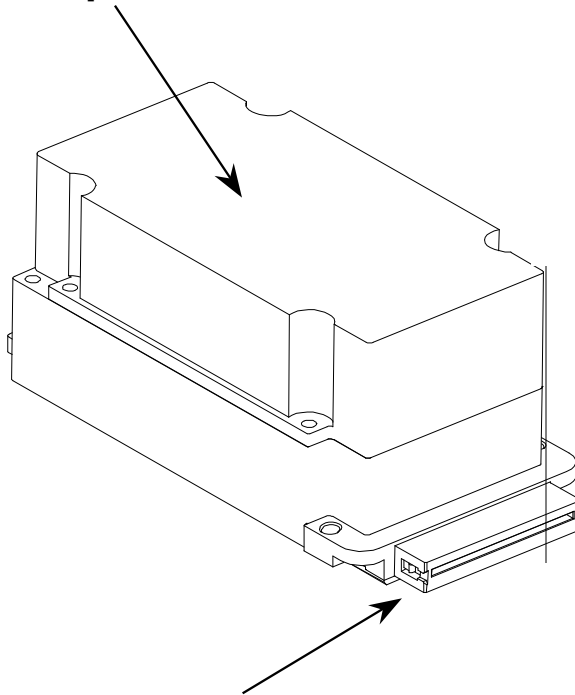
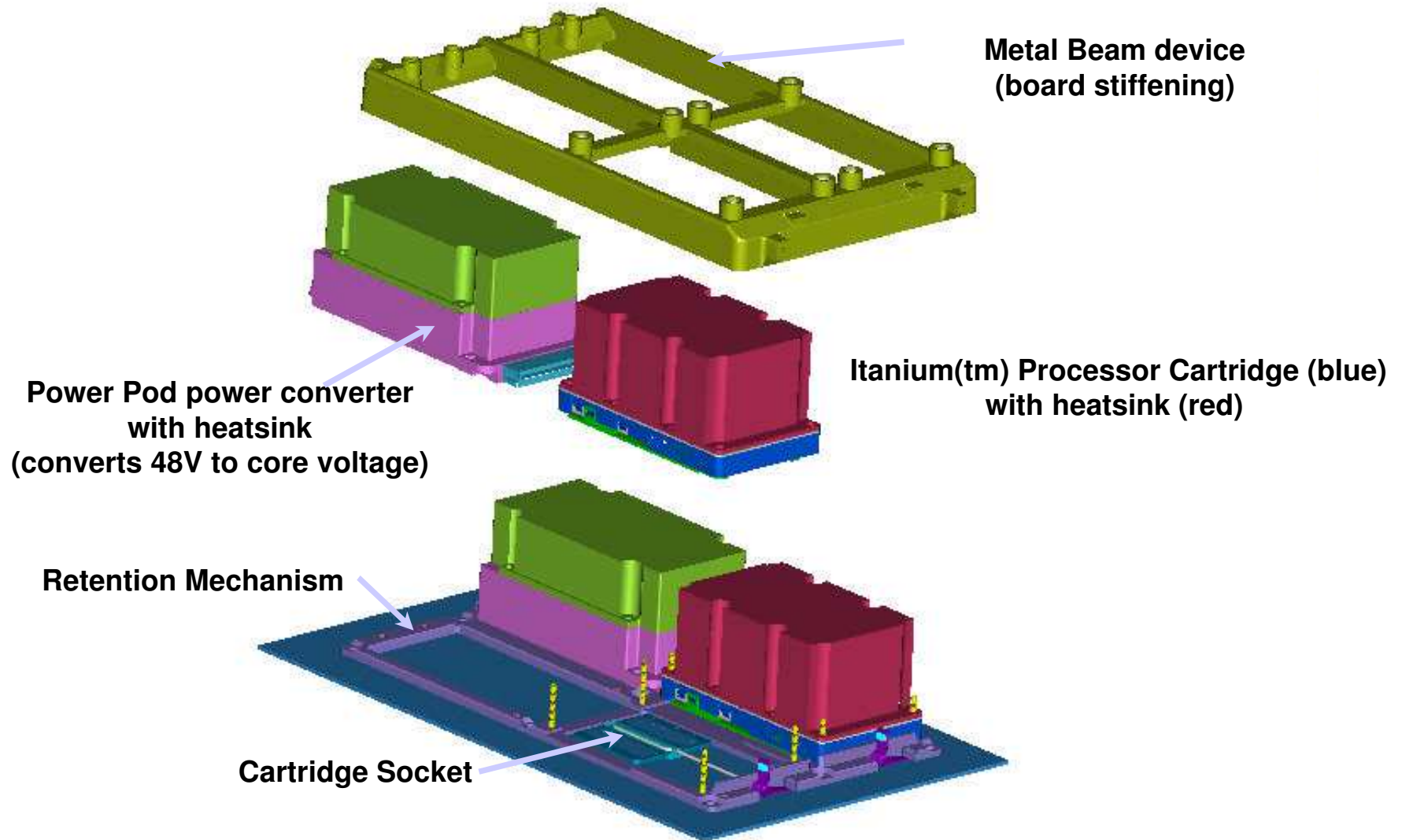**Connection to the cartridge supplies CPU and L3 cache power**
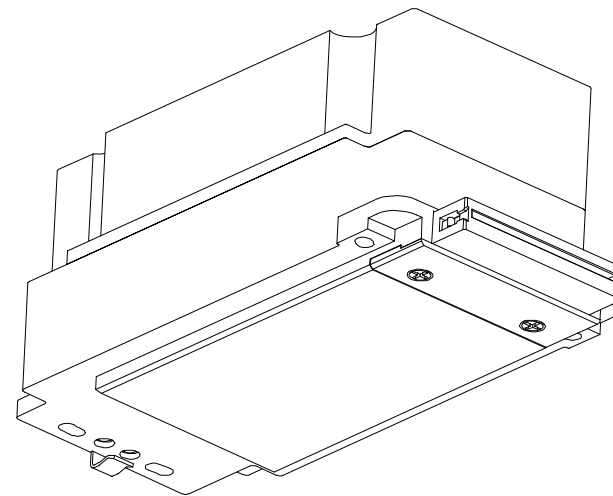
Powerpod converts 12VDC or 48VDC to the appropriate CPU and L3 voltages

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Power conversion

- Power Pod can convert either +48V or +12V DC to processor and cache voltages

- Hierarchical charge storage concept to lower di/dt demands
  - Capacitors are grouped by their ability to deliver charge
  - Much of the bulk storage capacitance is located inside the power pod

- Mechanically, pod mimics CPU cartridge width to prevent interference with bus performance

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Itanium™ Processor System Assembly

Metal Beam device
(board stiffening)

Itanium(tm) Processor Cartridge (blue)
with heatsink (red)

Power Pod power converter
with heatsink
(converts 48V to core voltage)

Retention Mechanism

Cartridge Socket

Itanium™ Processor System Assembly

**Power Pod power converters
with heatsink**

**Itanium™ Processor Cartridges
(with heatsink)**

~3"

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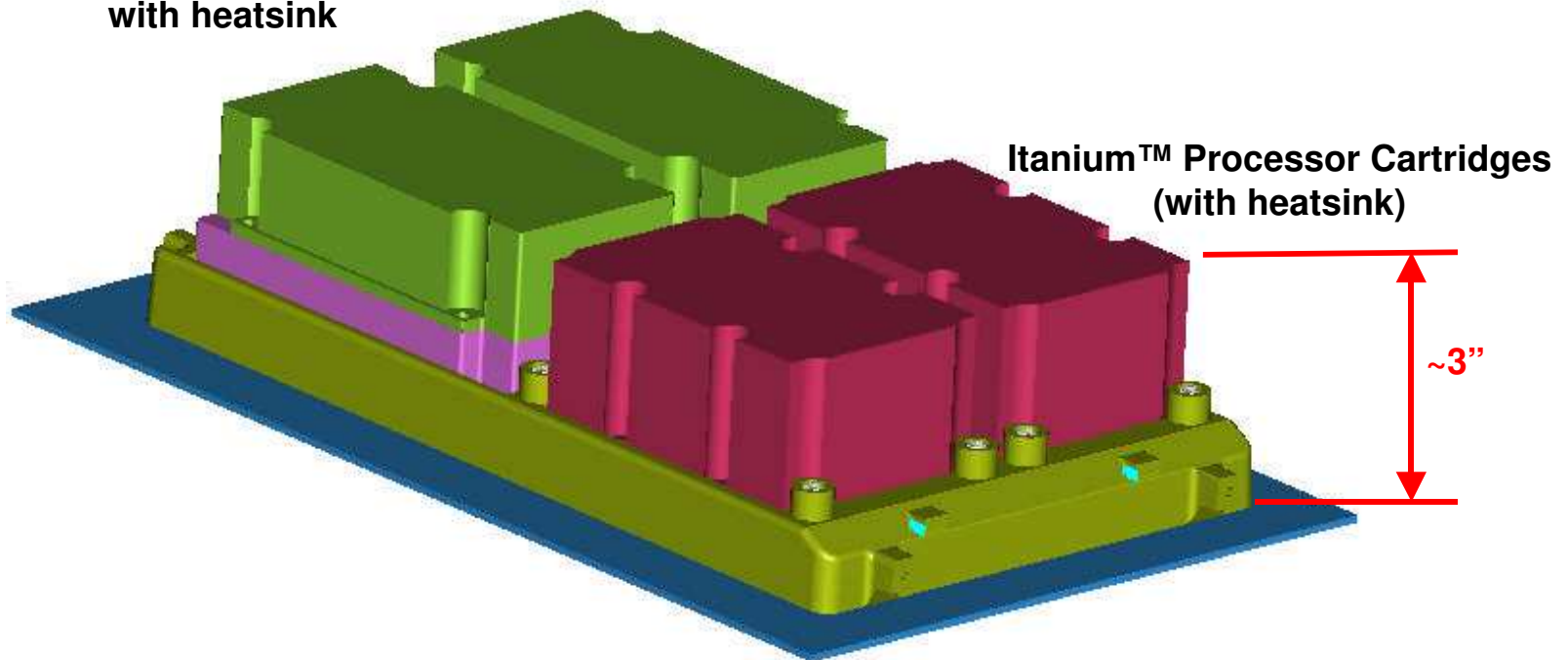
Heat Pipe LID

- The top section of the cartridge is a liquid filled phase change chamber
- Magnifies the thermal performance of the heatsink
- Temperature differential of just a few degrees Celsius across the entire top surface of the cartridge lid
  - Allows the use of a "conventional" air cooled heatsink
- Si contacts the bottom surface of the lid with high performance thermal interface material

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System Bus Overview

- A glueless integrated system bus interface

- Up to four Itanium™ Processor cartridges with Intel's 460GX chipset

- Chipset isolates the memory and I/O subsystems from the system bus

- Bi-directional multi-drop bus

  – 64 bits (plus 8 bits of ECC) for data

- Address bus operates at the system bus frequency (133MHz)

  – Conventional one transfer per clock cycle "common clock" mode

- Data bus can operate in a double pumped (source synchronous) transfer mode

  – Bus is clocked at 133 MHz allowing data transfers up to 266 MT/s or 2.1 GB/s

- double sided topology minimizes the delay impact on address and control signals in the conventional clocking mode

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Source Synchronous Timing Scheme

STROBE

STROBE

DATA[63:0]
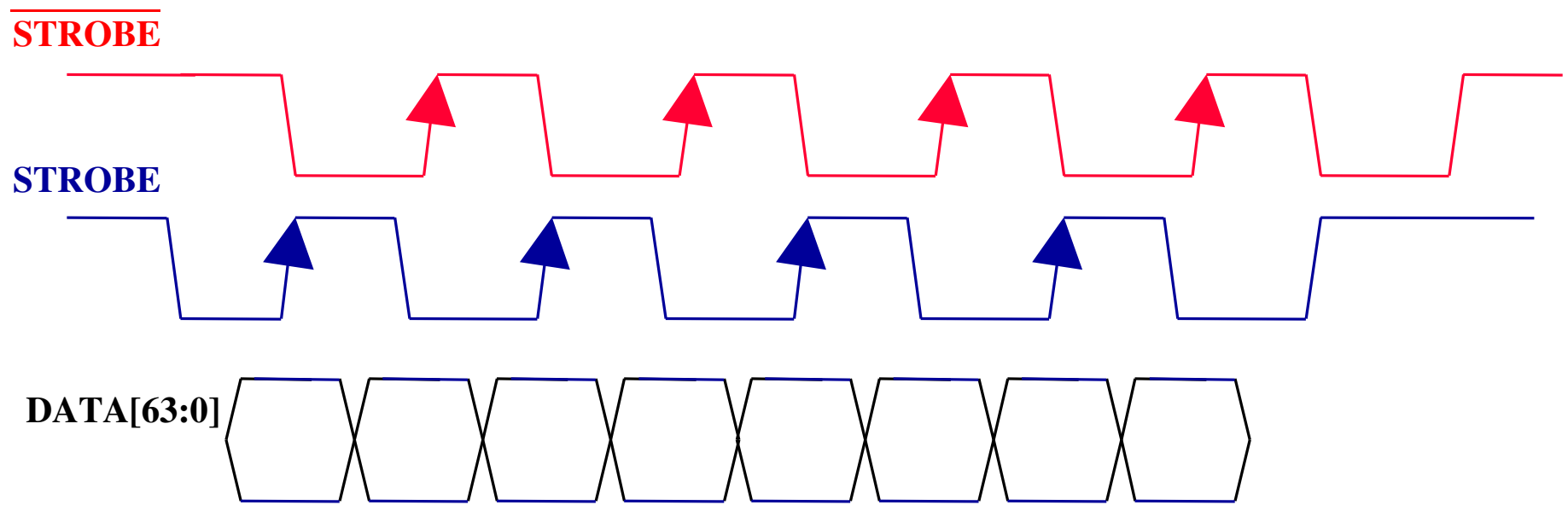
Note: STROBE and STROBE are the Source Synchronous clocks

System Bus Electrical Considerations

- The 460GX chipset architecture splits the address and data paths into separate packages

  - a single electrical load for both data and address

- "package return path inductance" which contributes to simultaneous switching output noise (SSO).

  - return current loops are minimized by proper placement of return vias for image currents

- external termination scheme is used

- system bus signals use Intel's GTL+ signaling scheme

- GTL+ voltage swing is 0.5V to 1.5V (larger swing than standard GTL) for extra noise margin.

- Compensated output drivers minimize bus reflections and control transmission variations in source synchronous signal groups

System Bus & Chipset Topology

133 MHz

System Bus (FSB)

133MHz or 266 MT/s

82460GX SAC

I/O

MEMORY

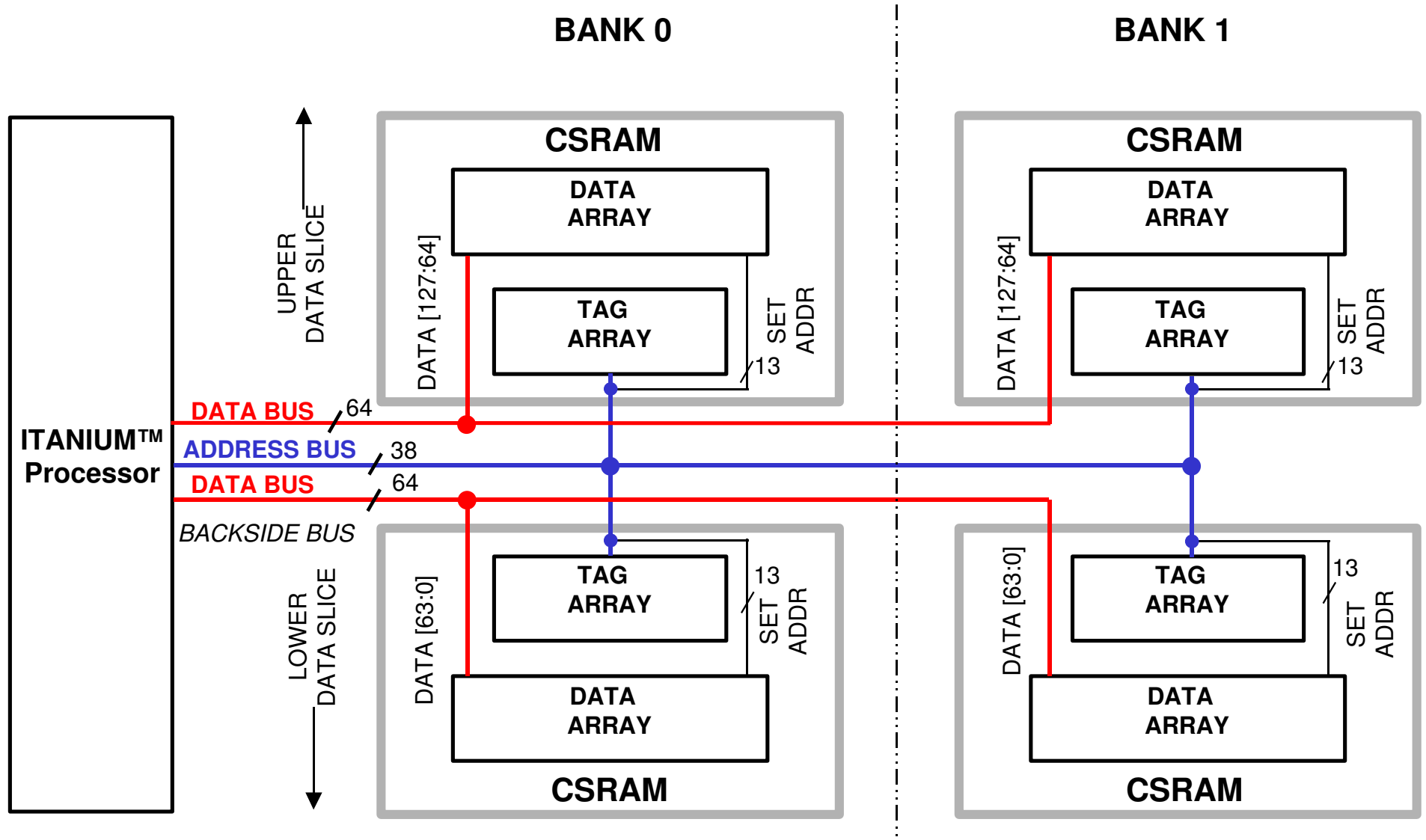82460GX SDC
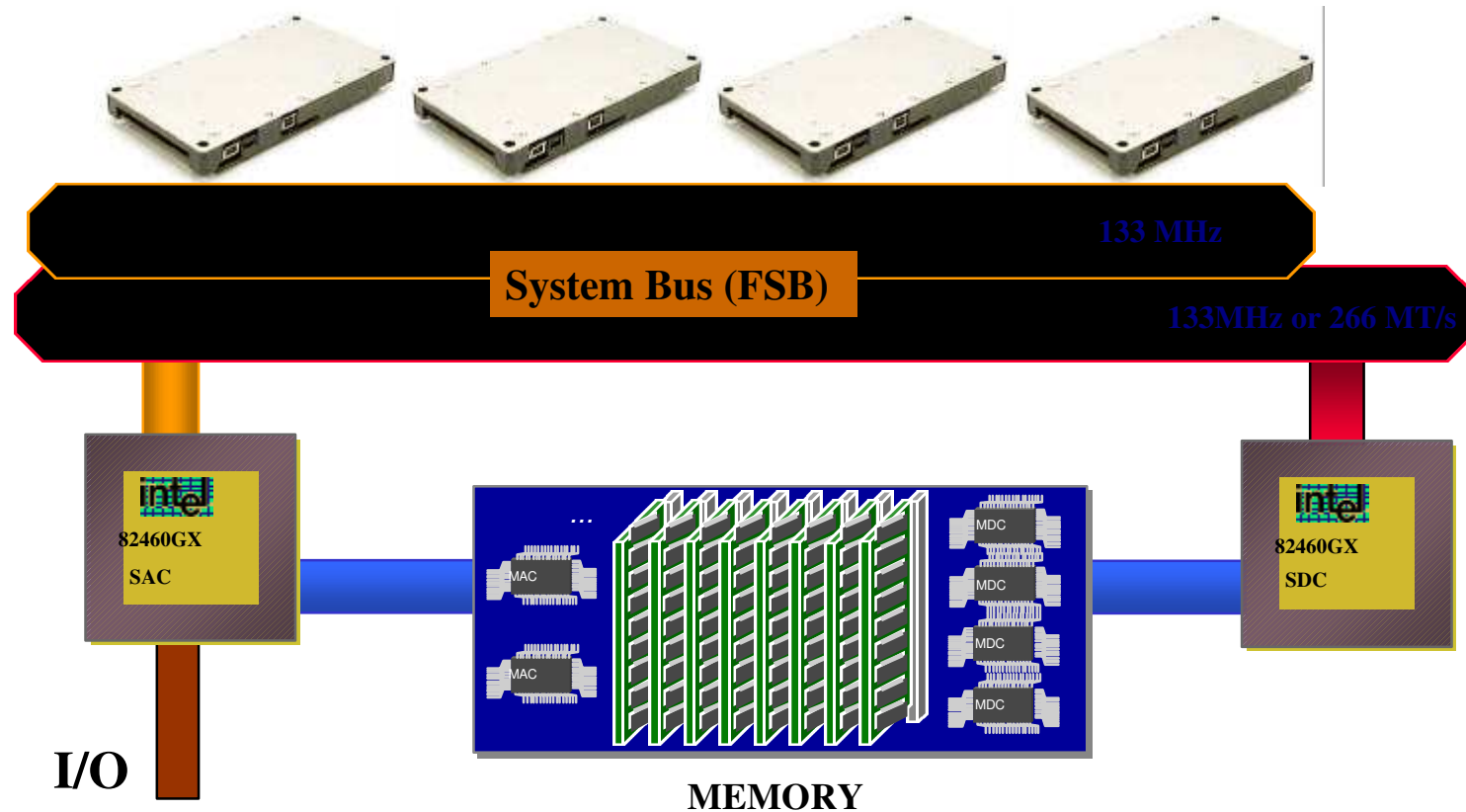
L3 Cache: The Backside Bus (BSB)

- Packaging the Custom Static RAM (CSRAM) as an MCM improves packaging density and performance

  - SRAM cell redundancy techniques alleviate MCM yield issues

- Two or four discrete 1 MB custom SRAM (CSRAM) devices
  - Each with a built in tag
  - Cache devices are organized in two address banks each containing 2MB of data

- Each bank is arranged as two 64 bit data slices for a total data width of 128 bits
  - This organization reduces the number of electrical loads on the data bus
  - Bandwidth of ~13 GB/s

- 128 bit data bus is divided into eight 16-bit, source synchronous, length matched data groups

- Cache address is 38 bits wide and protected by three bits of parity

- First access latency is 10 cycles
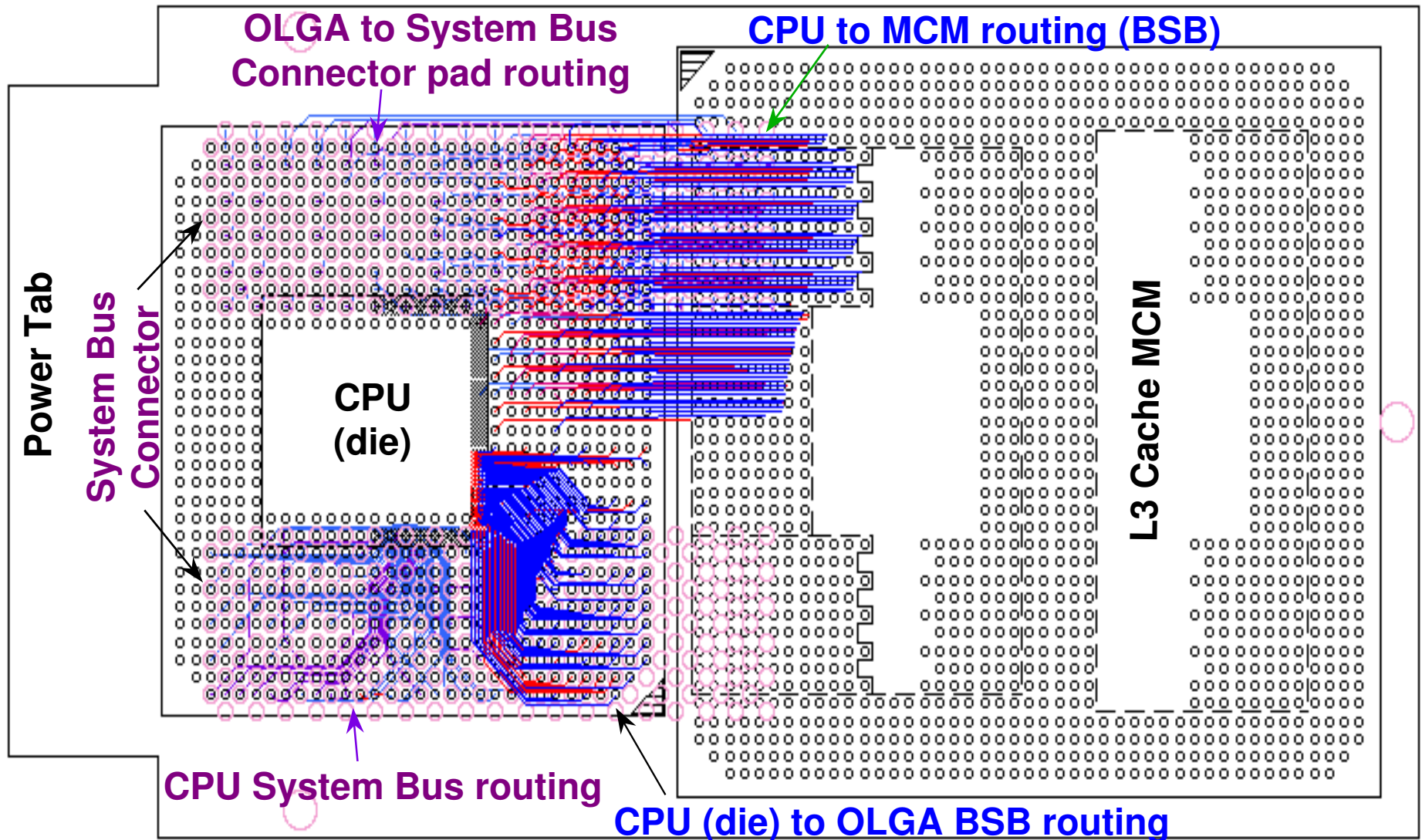 - From the CPU package through the L3 cache and back to the CPU package

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L3 Cache: The Backside Bus (BSB)

- Itanium™ Processor L3 cache line size is 64 bytes accessed as a four cycle burst

- A 128 bit wide data bus with a throughput up to 800 MT/s (full core speed)

- 4 cycle burst capability at core speed (continuous full BW R/W)

- BSB signals use an on die parallel termination scheme to minimize reflections

L3 Cache Organization

BANK 0

BANK 1

UPPER DATA SLICE

LOWER DATA SLICE

ITANIUM™ Processor

DATA BUS   /64

ADDRESS BUS   /38

DATA BUS   /64

BACKSIDE BUS

CSRAM

DATA ARRAY

TAG ARRAY

DATA [127:64]

SET ADDR   /13

TAG ARRAY

DATA ARRAY

DATA [63:0]

SET ADDR   /13

CSRAM

CSRAM

DATA ARRAY

TAG ARRAY

DATA [127:64]

SET ADDR   /13

TAG ARRAY

DATA ARRAY

DATA [63:0]

SET ADDR   /13

CSRAM

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Cartridge Package Routing

OLGA to System Bus Connector pad routing

CPU to MCM routing (BSB)

Power Tab

System Bus Connector

CPU (die)

L3 Cache MCM

CPU System Bus routing

CPU (die) to OLGA BSB routing

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4M Cache MCM Routing

4MB MCM Routing Example

BSB Data

(1/2 shown)

BSB Address, Cmd&Cntl
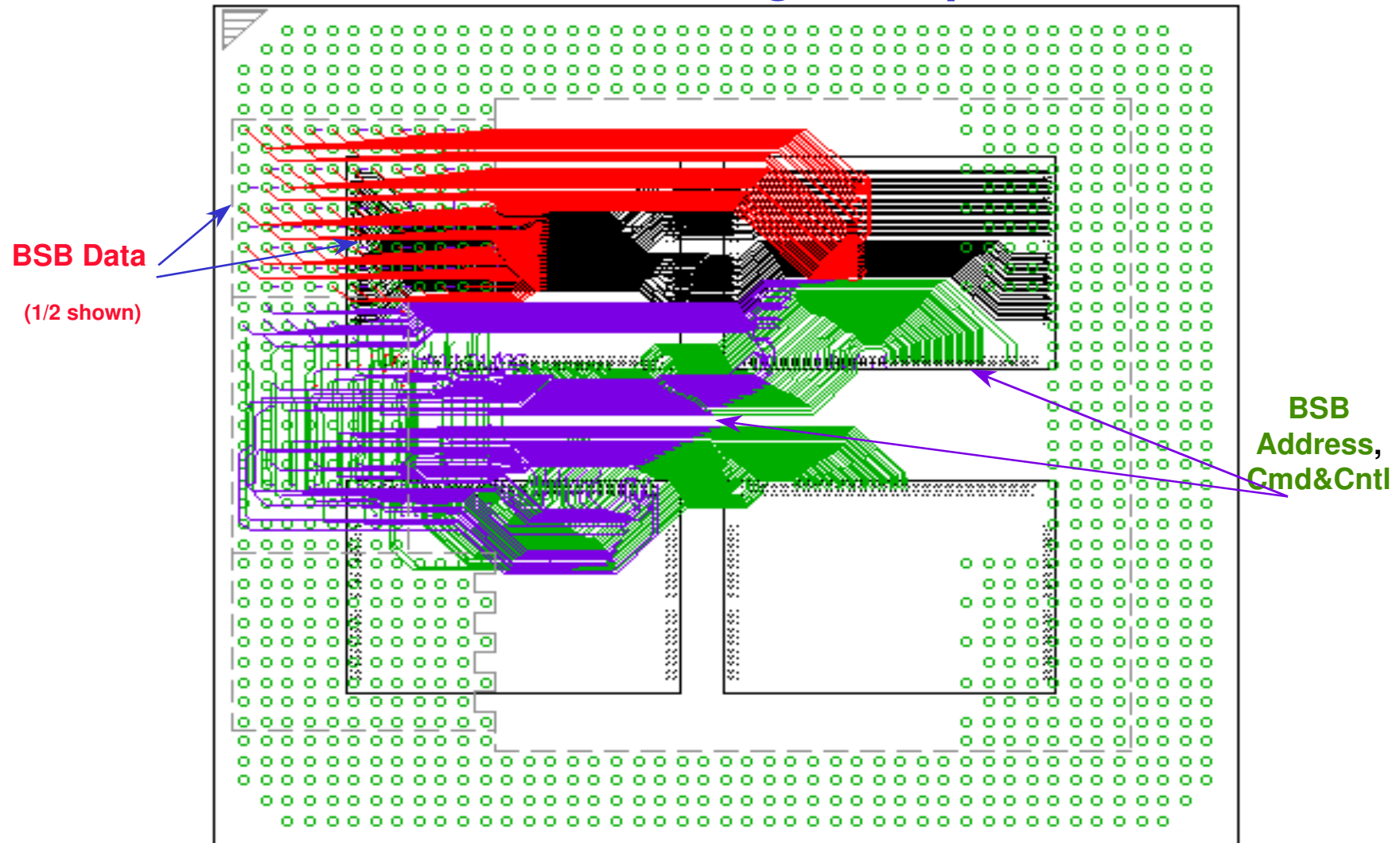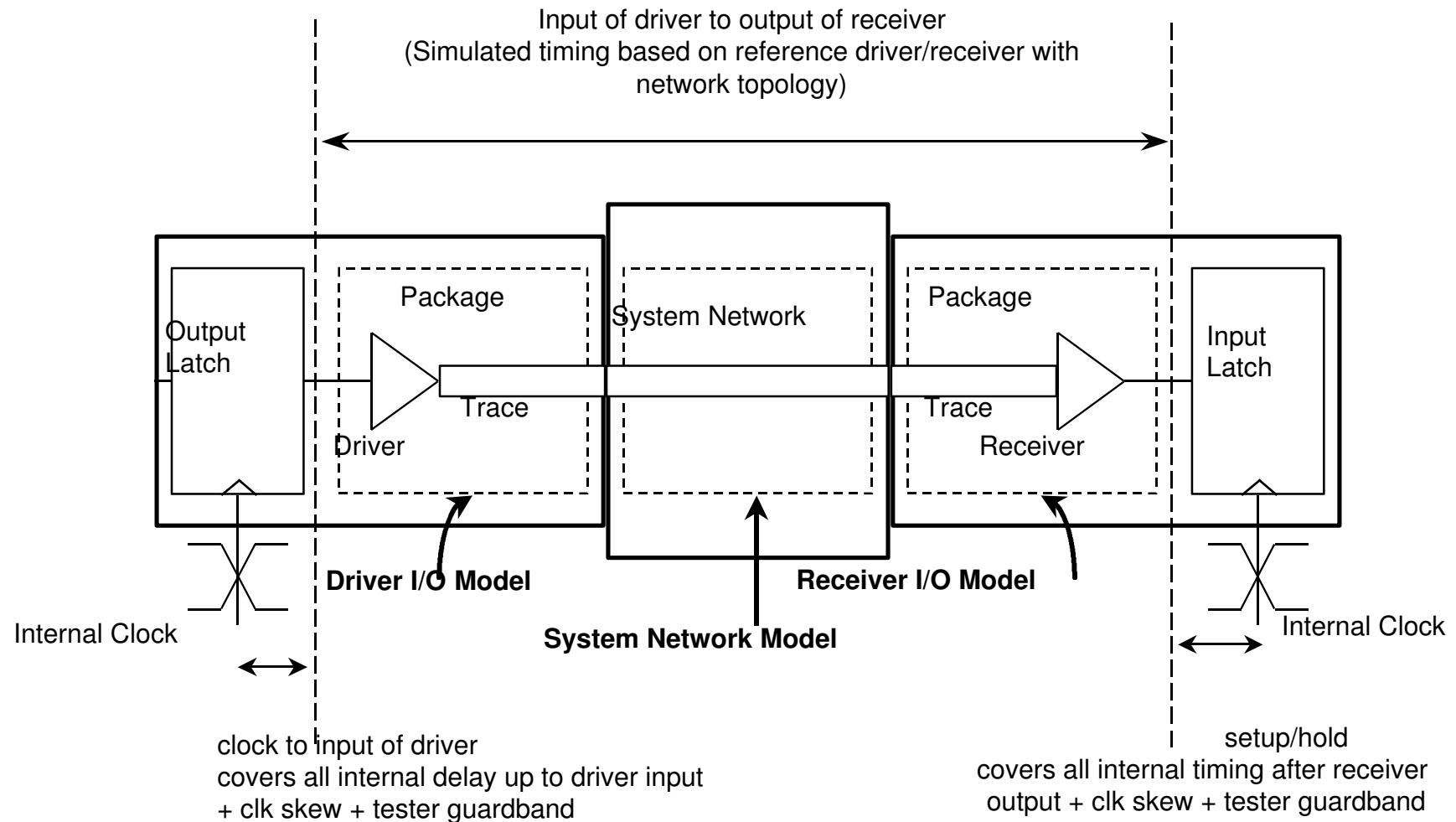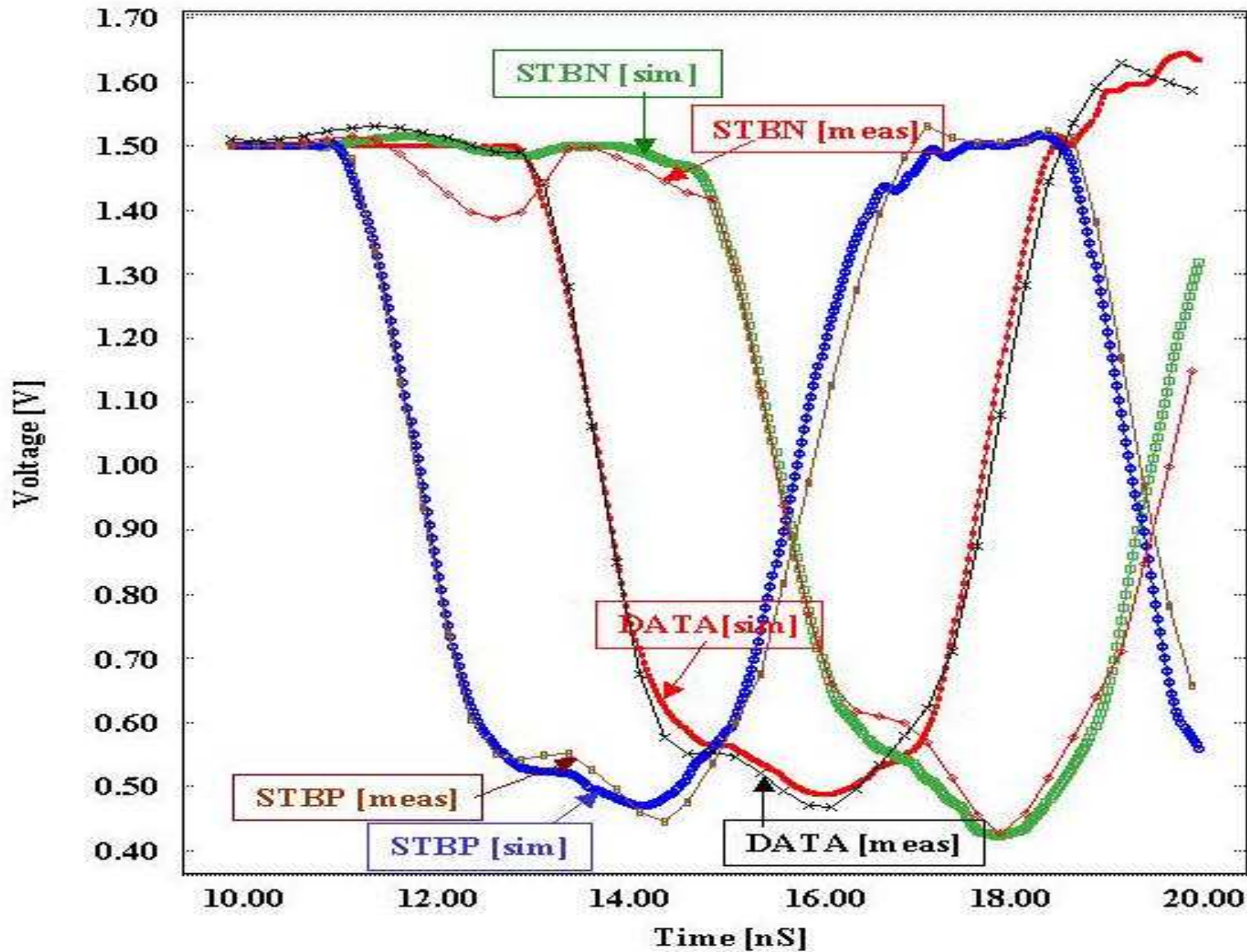
Cartridge Electrical Modeling

- Utilization of full circuit simulators. SPICE or SPICE-like circuit analysis tools capable of combining non-linear transistor models (I/O buffers) with complex interconnect structures

- Electrical parasitics extracted using 3D field solvers

- The partial element equivalent circuit (PEEC) approach, combined with 3D extraction, modeled coupled interconnects and discontinuities

- Explicit return path modeling proved to be a tremendous benefit

Simulation Methodology

Input of driver to output of receiver
(Simulated timing based on reference driver/receiver with network topology)

Output Latch

Package

Driver I/O Model

Driver

Trace

System Network

System Network Model

Package

Trace

Receiver

Receiver I/O Model

Input Latch

Internal Clock

Internal Clock

clock to input of driver
covers all internal delay up to driver input
+ clk skew + tester guardband

setup/hold
covers all internal timing after receiver
output + clk skew + tester guardband

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System Bus Simulation vs. Timing

SUMMARY

- An optimized package for high performance busses

    - High performance system bus

    - High performance core speed 4M cache

- Innovative power deliver scheme

- Thermal solution allowing passive air cooled heat sinks

- Extensive electrical modeling and simulation