The SB-1™ Core:

A High Performance, Low Power MIPS64™ Implementation

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SiByte Background

- **Semiconductor Supplier for Networking and Communications Infrastructure**
  - High Performance, Low Power, Integrated SOC Solutions
- **World's best design capabilities for High Performance, Low Power VLSI**
  - Processor, System, and Software Design Experience
- **Marketing and sales expertise in embedded networking and communications markets**

SB-1 Design Goals

- **Industry Standard ISA**
  - Existing Tool and Application Support
- **Server-class Performance**
  - Highest Embedded Processor Performance
- **Embedded-class Power Consumption**
  - Highest Performance/Watt in its Performance Class
- **Chip Multiprocessor (CMP) Support**
  - Full MP Coherency
  - High Bandwidth Bus Interface
  - Scalable Performance
- **Design Re-use and Flexibility**
  - Building block for multiple generations of SiByte SOCs

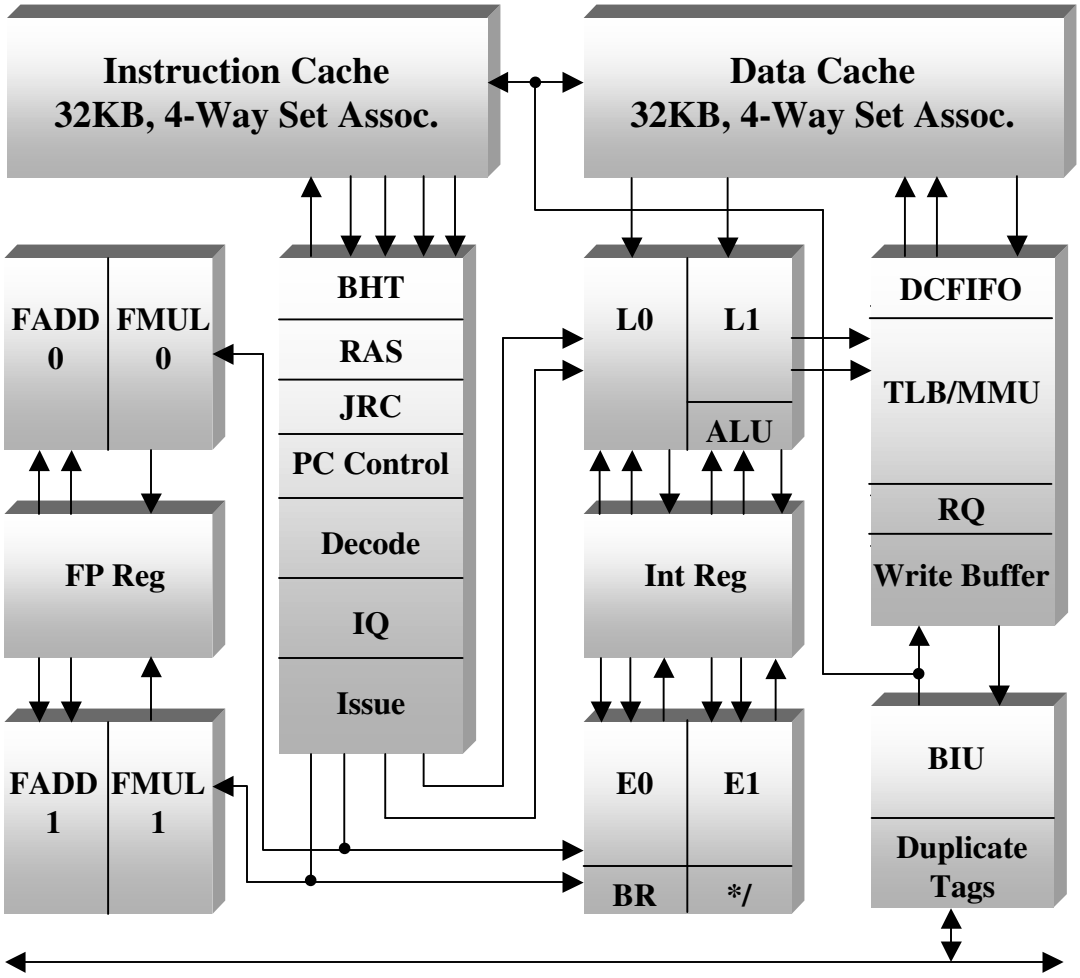
SB-1 High Level Spec

ISA	MIPS64, MIPS-3D™
Frequency	600MHz – 1GHz
Microarchitecture	In-order Quad Issue (Dual ALU/FP, Dual Memory)
Branch Prediction	BHT, JRC, RAS
Instruction Cache	32KB, 4-Way Set Associative
Data Cache	32KB, 4-Way Set Associative
TLB	64 x 2 Entries
MP Support	Fully Coherent MESI Protocol
Process Technology	0.15 micron
Operating Voltage	1.2 Volts
Power Consumption	~2.5 Watts at 1GHz
Estimated Die Area	~25mm^2

SB-1 MIPS64 ISA

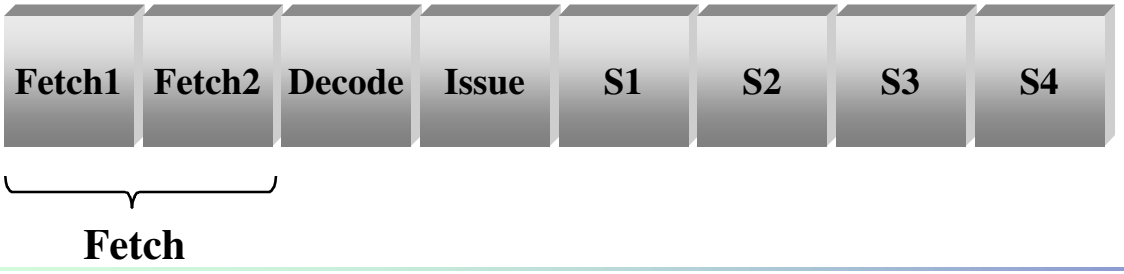
- **MIPS64**
  - Unified 64/32-bit Application ISA
  - Embedded Application Instructions
  - Standardized Privileged Resource Architecture
  - Paired Single Floating Point
- **MIPS-3D**
  - 3D-Graphics Instructions
  - RECIP/RECIPSQRT Approximations
  - Specialized Branches

SB-1 Block Diagram



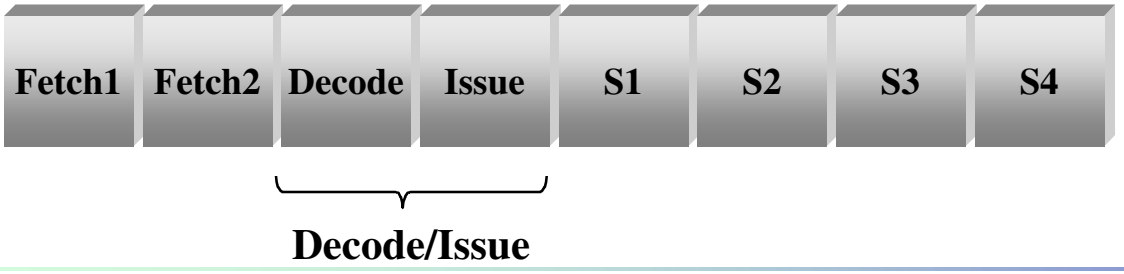
SB-1 Instruction Fetch

- **Four Instructions Fetched Per Cycle**
- **Advanced Branch Prediction**
  - 4K-entry Gshare Direction Predictor
  - 64-entry Indirect Jump Cache
  - 8-entry Return Address Stack
- **Up to Two Branch Predictions each Instruction Fetch**



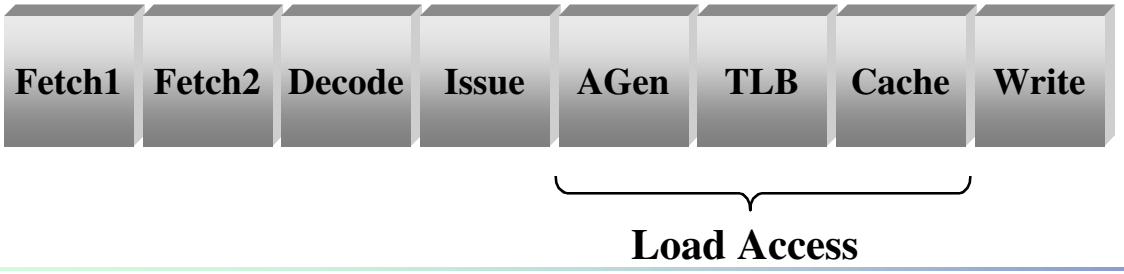
SB-1 Decode/Issue

- **Instruction Queue**
  - Stores up to 24 decoded instructions
  - Decouples Fetch engine from Issue stalls
- **Maximum of Four Instructions Issued**
  - Mix of two Integer or FP instructions
  - Mix of two Load or Store instructions
- **IQ Serves as a Replay Buffer**
  - Eliminates pipeline stalls



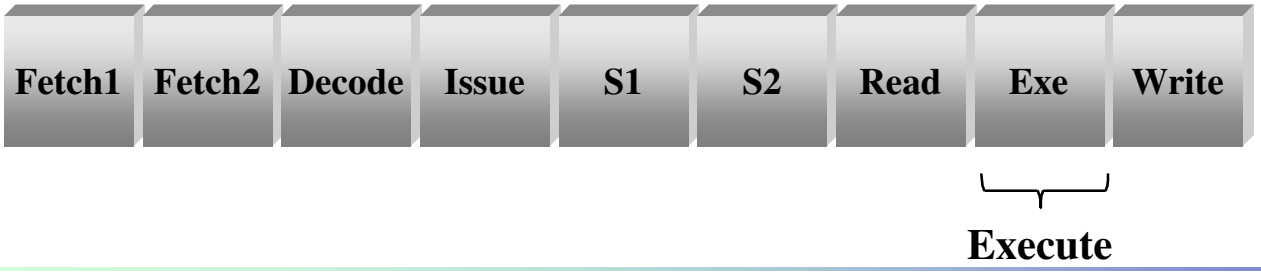
SB-1 Load/Store Unit

- **Two Loads/Stores Per Cycle**
- **Simple 64-bit ALU**
  - Adds, Subtracts, and Logical Instructions
- **Non-Blocking Data Cache**
  - 8 Outstanding Cacheline Misses
  - Request Merging
- **Full Prefetch Support**



SB-1 Integer Unit

- **Two 64-bit ALU Execute Units**
  - 1-Cycle Execution Latency for Most Instructions
- **Branch Evaluate Unit**
- **Integer Multiply/Divide Unit**
  - Fully-Pipelined, 3-Cycle MADD
  - Complete 64-bit Integer Multiply and Divide
- **4 BOPS Peak**



SB-1 Floating Point Unit

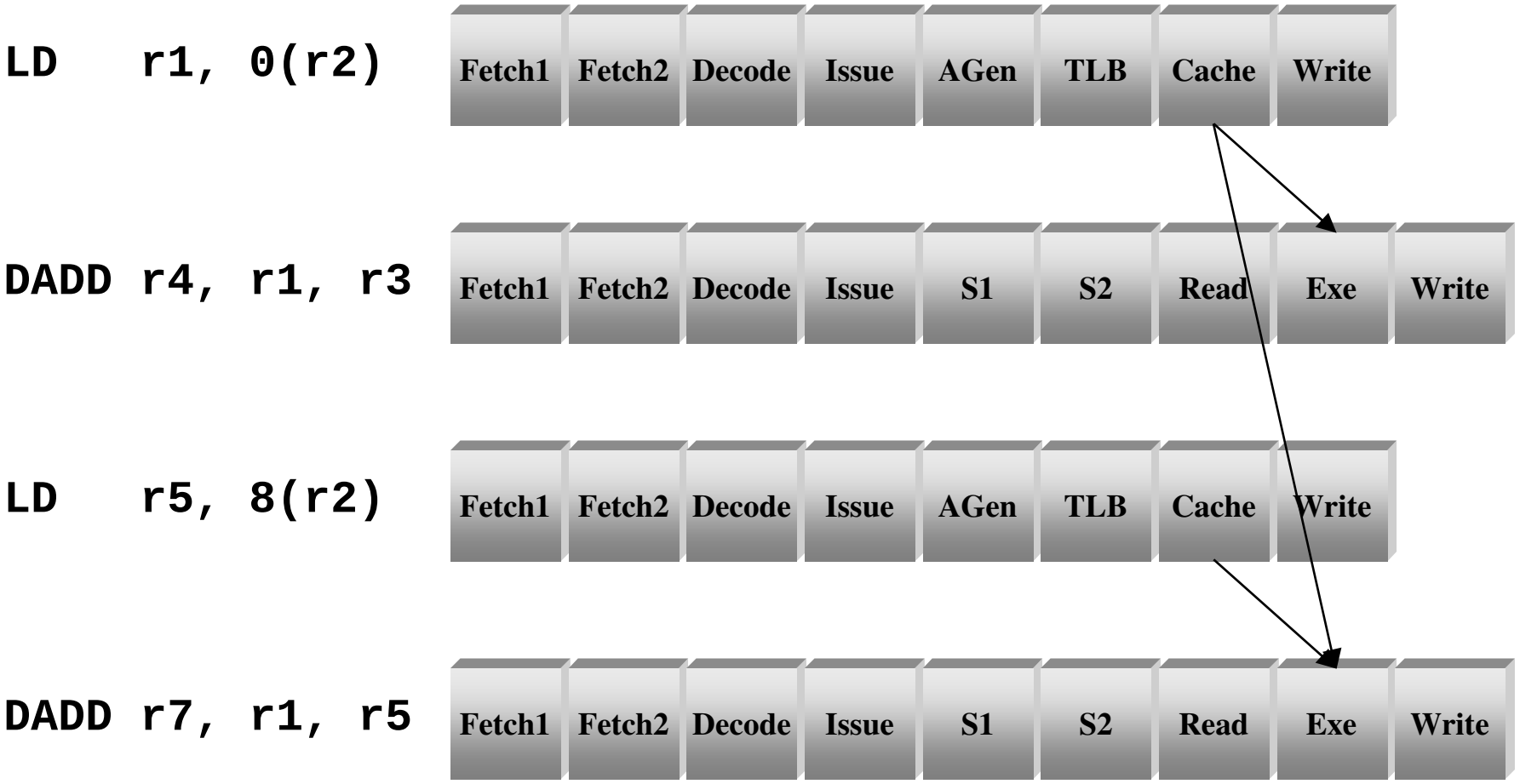
- **Two Double Precision FP Execute Units**
  - 4-Cycle Execution Latency
  - Fully-Pipelined
- **IEEE 754 Compliant**
- **Paired Single Instruction Support**
- **4 SP MADDs/Cycle, 8 SP GFLOPS**

SB-1 Pipeline Highlights

- **Load Data Forwarding**
  - Zero Cycle Load-to-Use Delay
  - High Performance
  - Simple Implementation

- **Simple Load/Store Unit ALU**
  - Early Address Generation for Loads and Stores
  - Dependent Integer Operations may be issued simultaneously

Zero Cycle Load-to-Use



SB-1 Performance/Power

- **Server-class Microprocessor Performance at Embedded Processor Power**

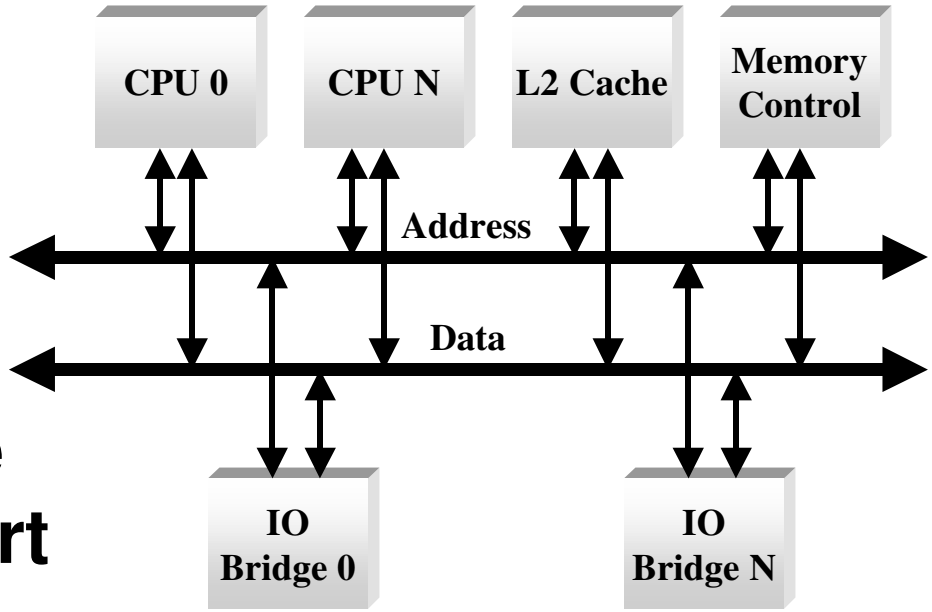
Dhrystone 2.1 MIPS	> 2000 MIPS, > 800 MIPS/Watt
Peak Integer Ops	4 Ops/Cycle, 4 BOPS Peak
Peak FP Ops	8 Ops/Cycle, 8 GFLOPS Peak

SB-1 Low Power Design

- **Low V_{dd}**
  - 1.2 Volts
  - 36% Power Savings vs. 1.5 Volts
- **Extensive Use of Clock-Gating**
  - 30% Power Savings
- **Flip-Flop-Based Design**
  - Saves Power vs. Latch-based Designs
  - Estimated 10% Power Savings
- **Mostly Static Logic**
  - Selective Use of Dynamic Logic (5 - 10% Savings)
- **Optimized Layout**

SB-1 MP Support

- **CMP-Ready Core**
  - Fast, Fully-Coherent, Split Transaction, MP Bus Interface
  - Total Bus BW:
    - 16 GB/Sec
- **Load Linked, Store Conditional Support**
- **Snoop Support**
  - Duplicate L1 Tags



SB-1 Summary

- ✓ **High Performance MIPS64 CPU Core**
  - > 2000 Dhrystone 2.1 MIPS
  - 8 GFLOPS Peak FP Performance
- ✓ **Low Power in a Small Die Area**
  - ~2.5 Watts at 1GHz in 25mm^2
  - > 800 MIPS/Watt
- ✓ **Support for Chip Multiprocessing**
  - Full MP Coherency with Snoop Tags
  - 16 GB/Sec Bus Bandwidth
- ✓ **Foundation for Multiple SOCs**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