A 12-bit 50Mpixel/s Analog Front End Processor for Digital Imaging Systems

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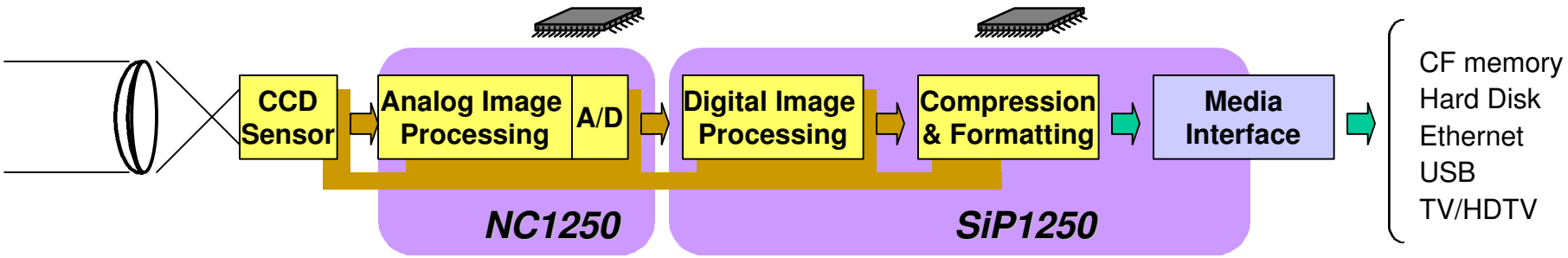
Bird's Eye View of Digital Camera

- A complete system from sensor to storage

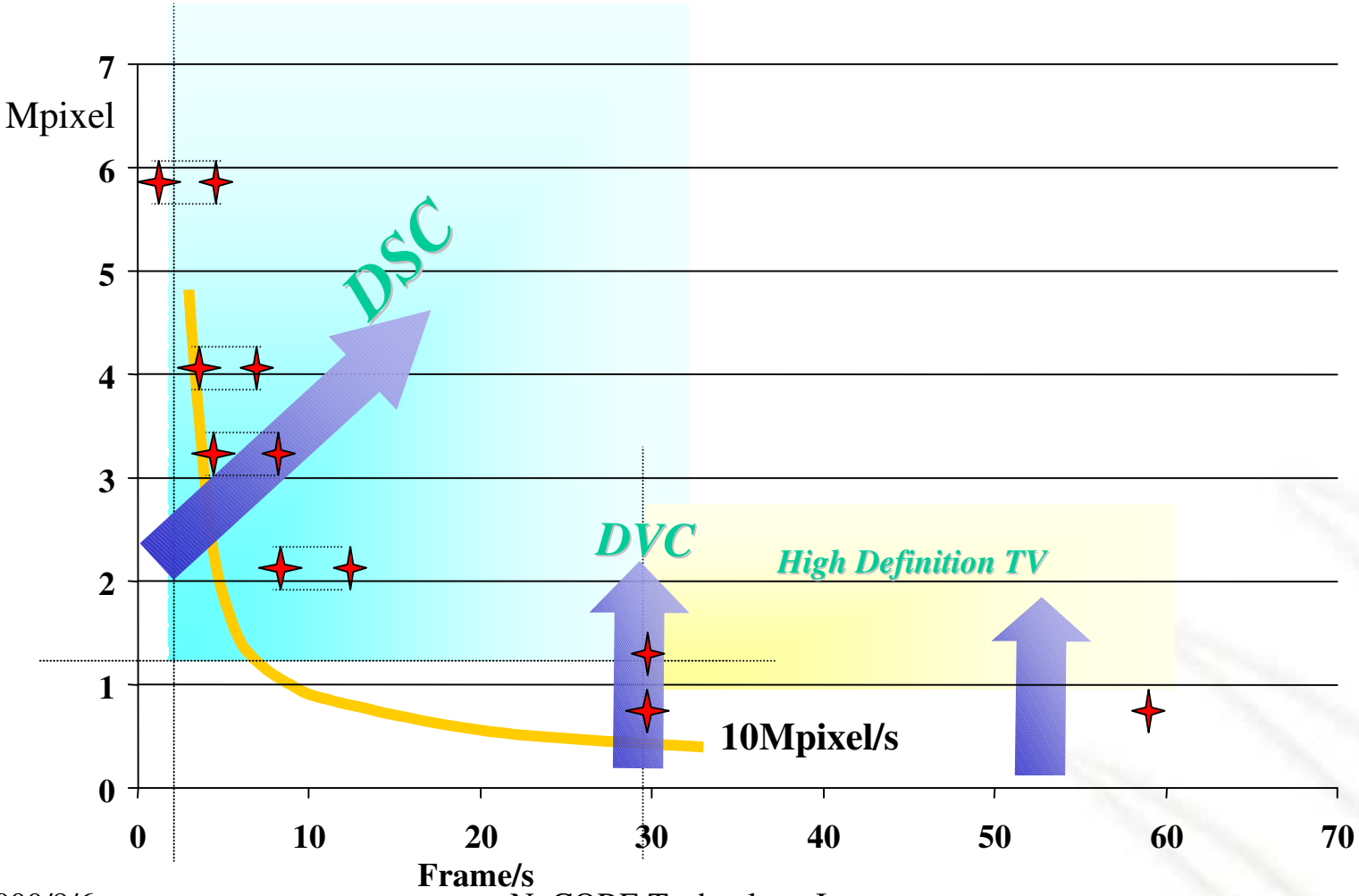
Digital Camera System



Bird's Eye View of Digital Camera

- A complete system from sensor to storage
- 300Kpix 1Mpix 2Mpix 3Mpix ⟹

Digital Camera Requirements



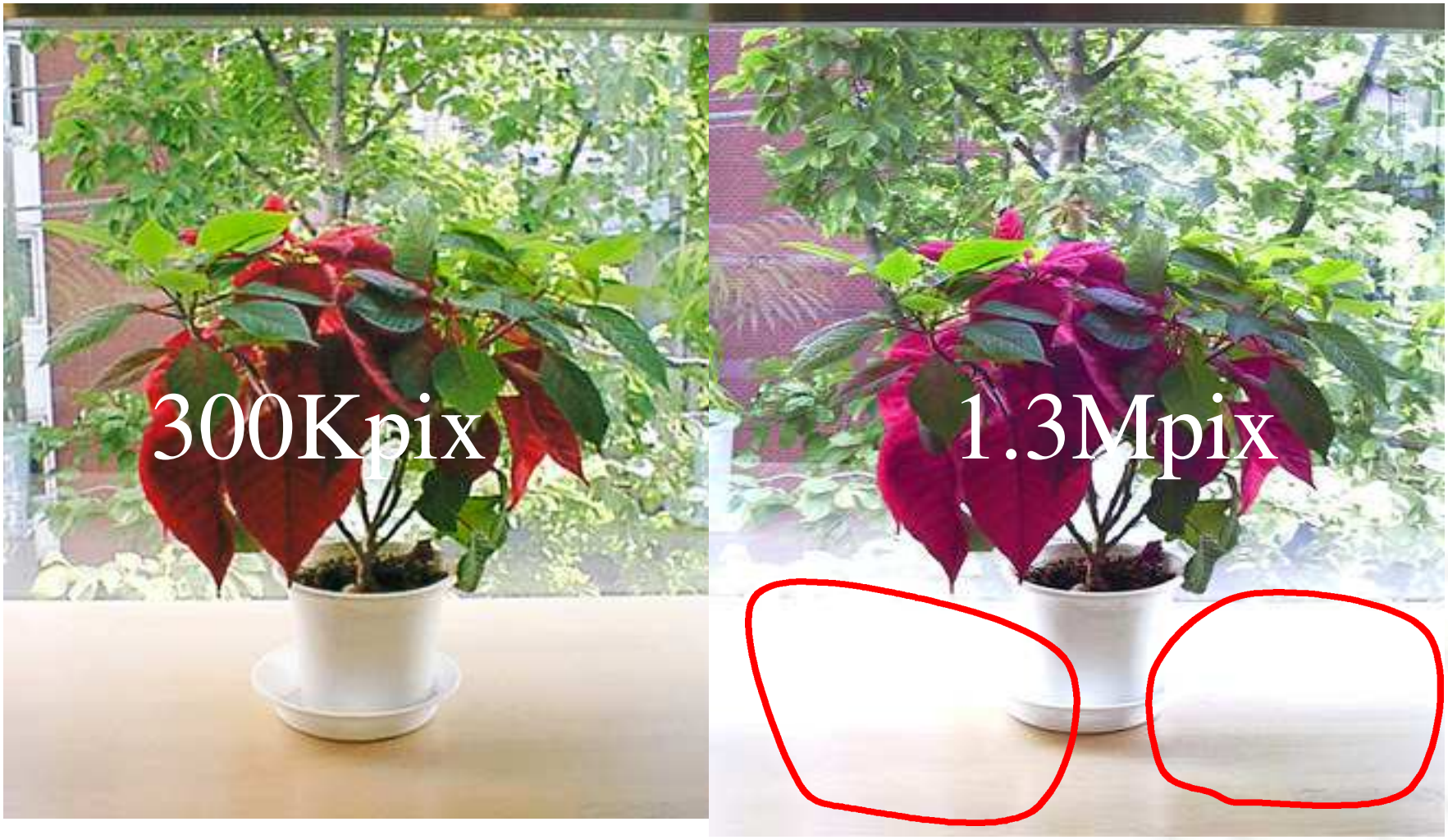
Problem!

- A complete system from sensor to storage
- 300Kpix 1Mpix 2Mpix 3Mpix 
- Slow speed !!!
- Short battery life !!!

Another Problem!?

- A complete system from sensor to storage
- 300Kpix 1Mpix 2Mpix 3Mpix 

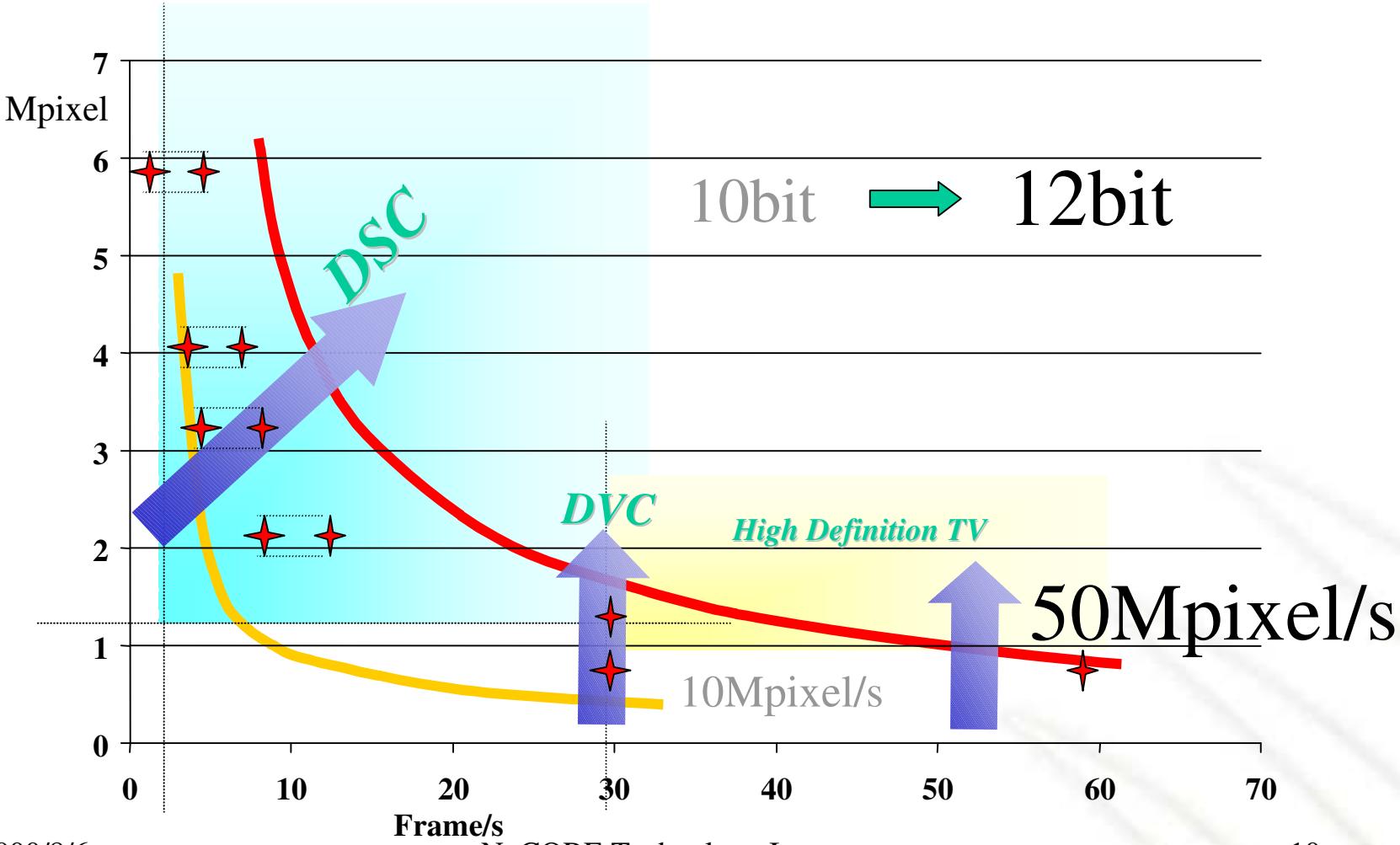
Serious D-Range Problem!



Problem's !

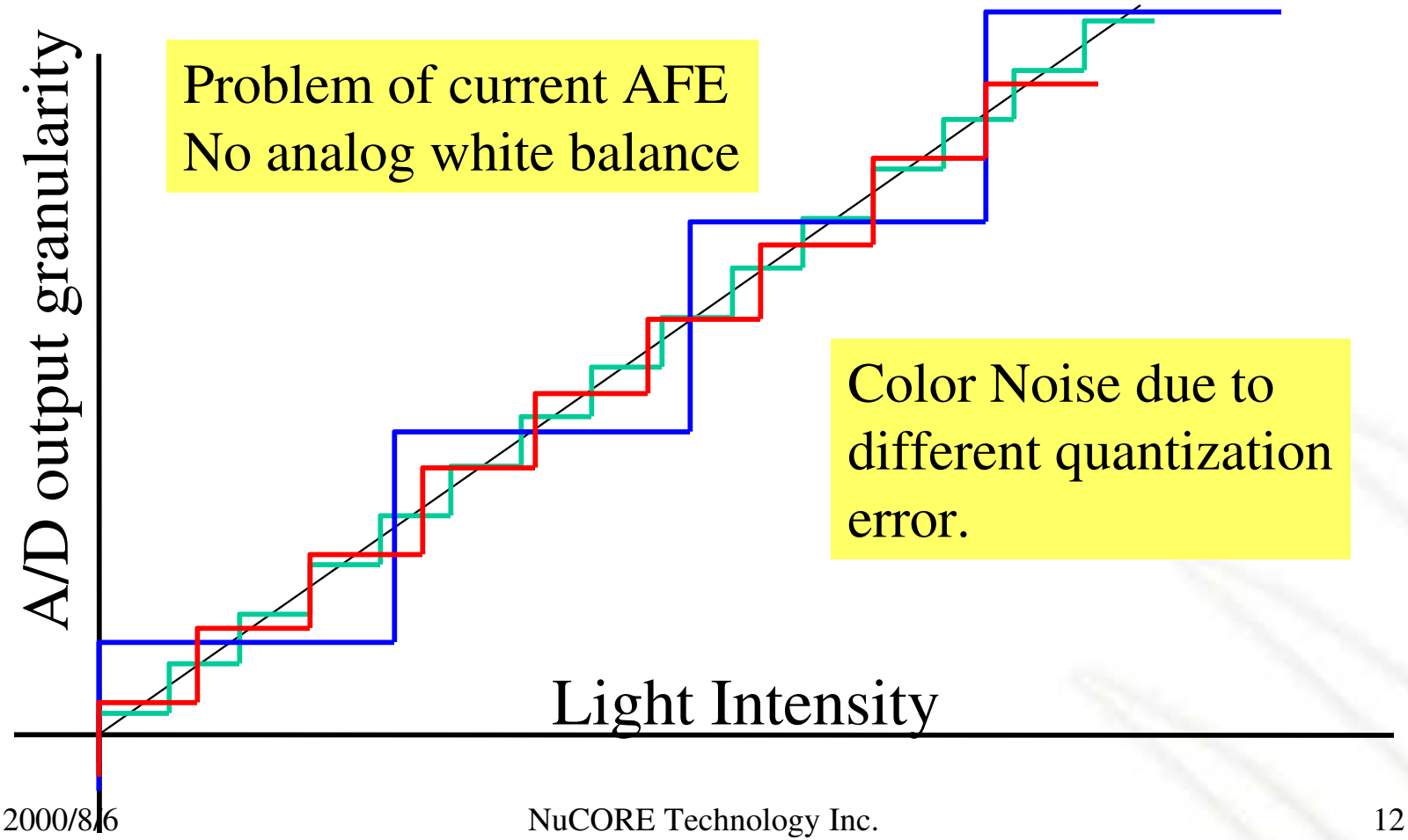
- A complete system from sensor to storage
- 300Kpix 1Mpix 2Mpix 3Mpix 
- Slow speed !!!
- Short battery life !!!
- Low dynamic range !!!
  - 10bits **12**bits,

Performance Goal

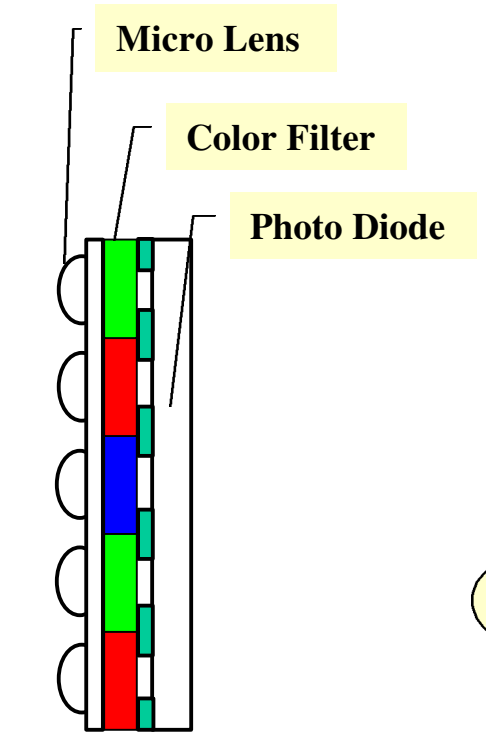


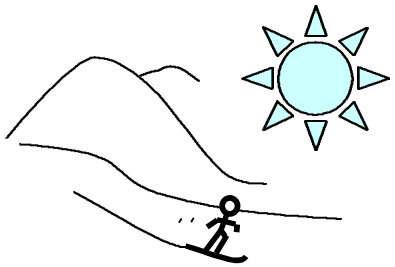
More D-Range Problem!

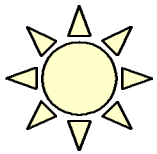
Color Noise in half tone area

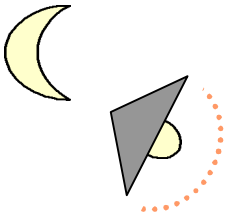


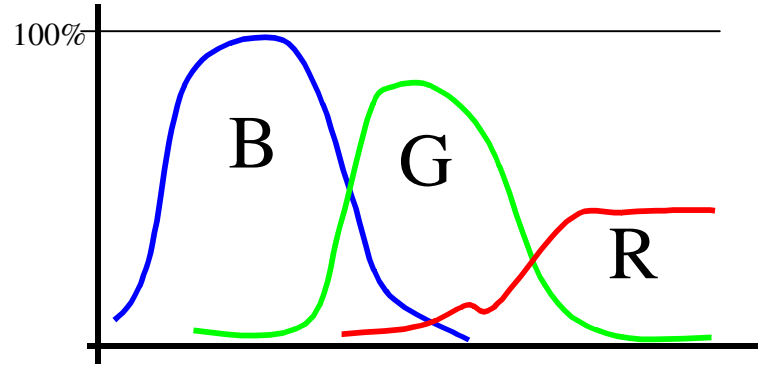
Spectrum Change

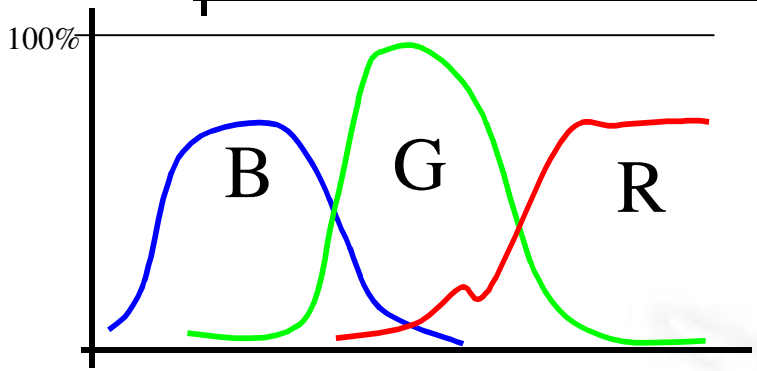


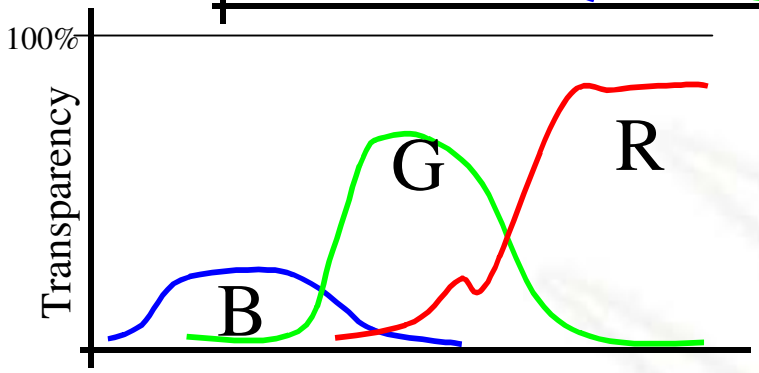






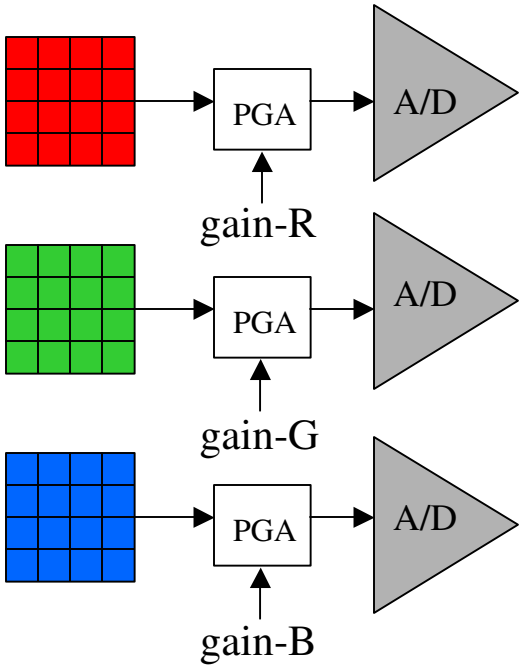


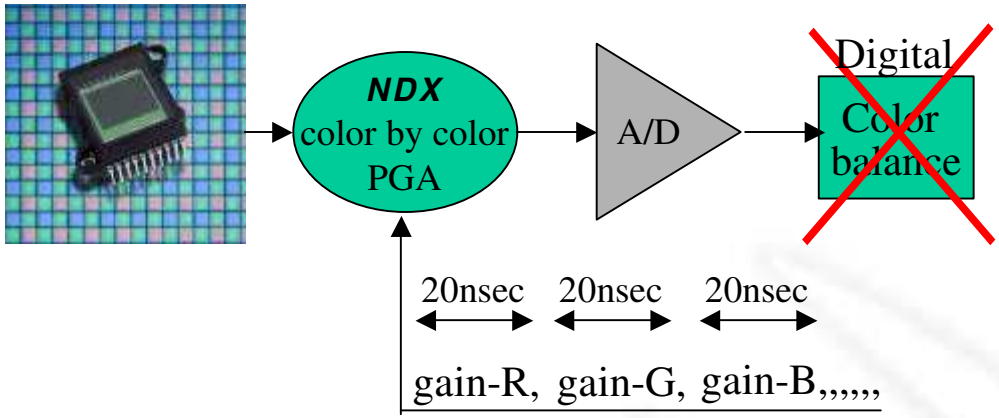




NDX enables analog white balance

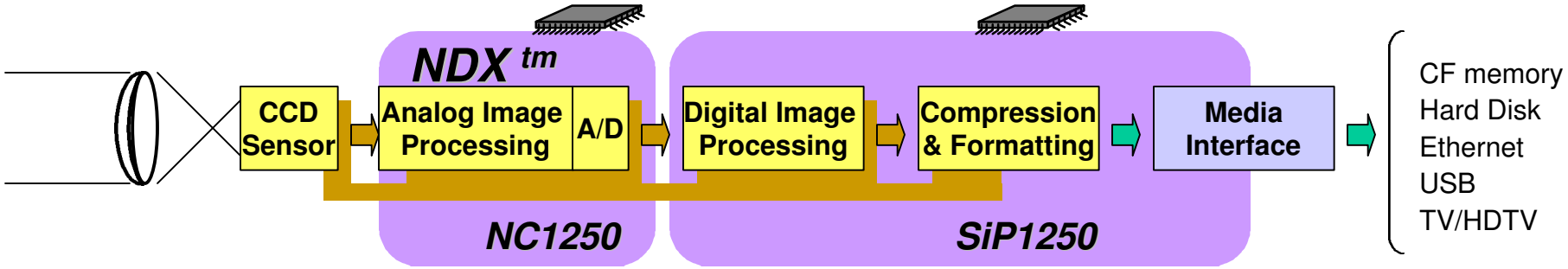
- Equalize Color D-Range before A/D
- Color spectrum vary caused by;
  filter, light source, scene, etc,,,
  need color by color compensation





3 CCD Camera → **"Single CCD + *NDX* " Camera**

Technical Challenges



*** 12-bit accuracy along entire image chain**

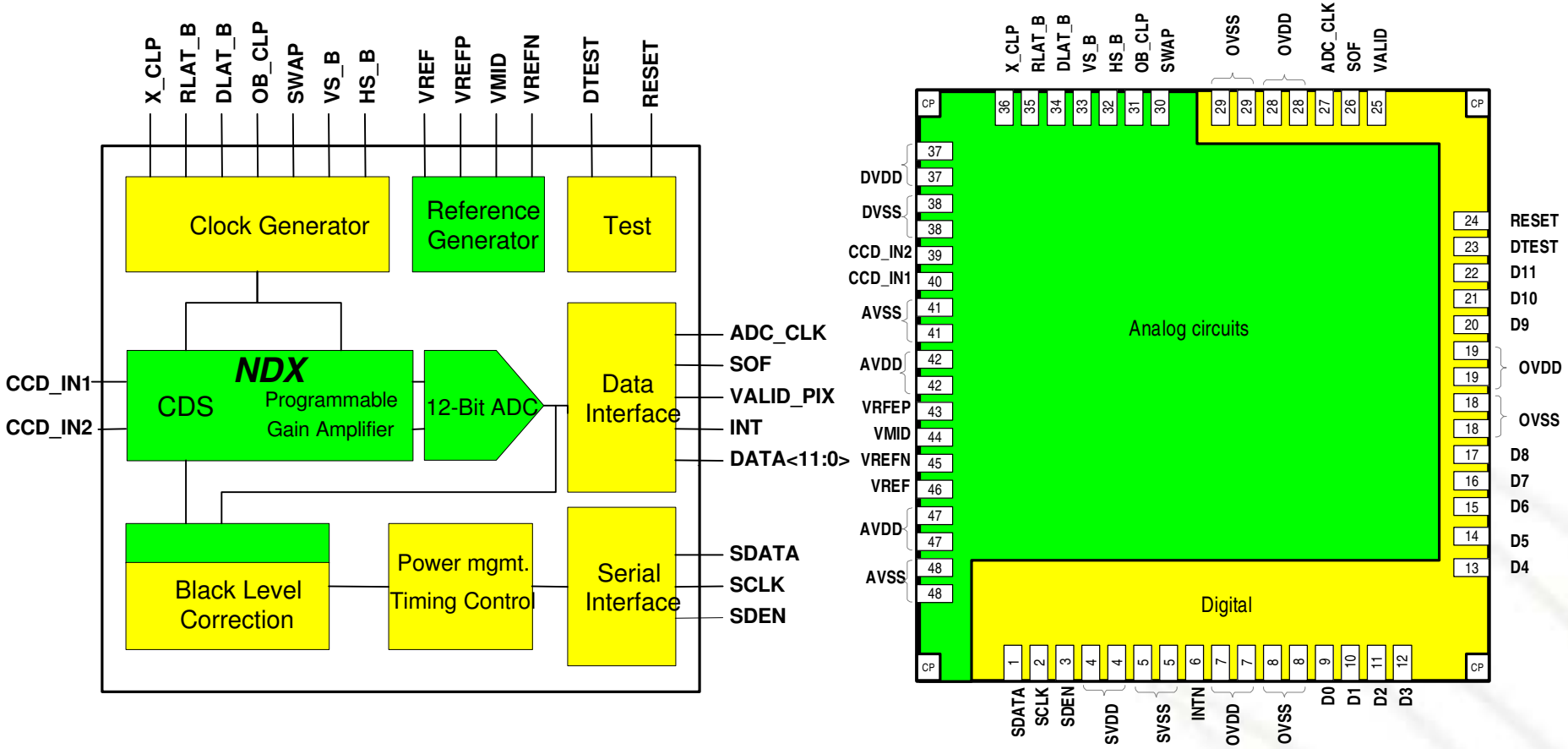
*** Color by color gain control in Analog** ***NDX tm***

*** Very low power dissipation**

*** >50 Mpixel/s <20 nsec time budget !**

13 patents pending

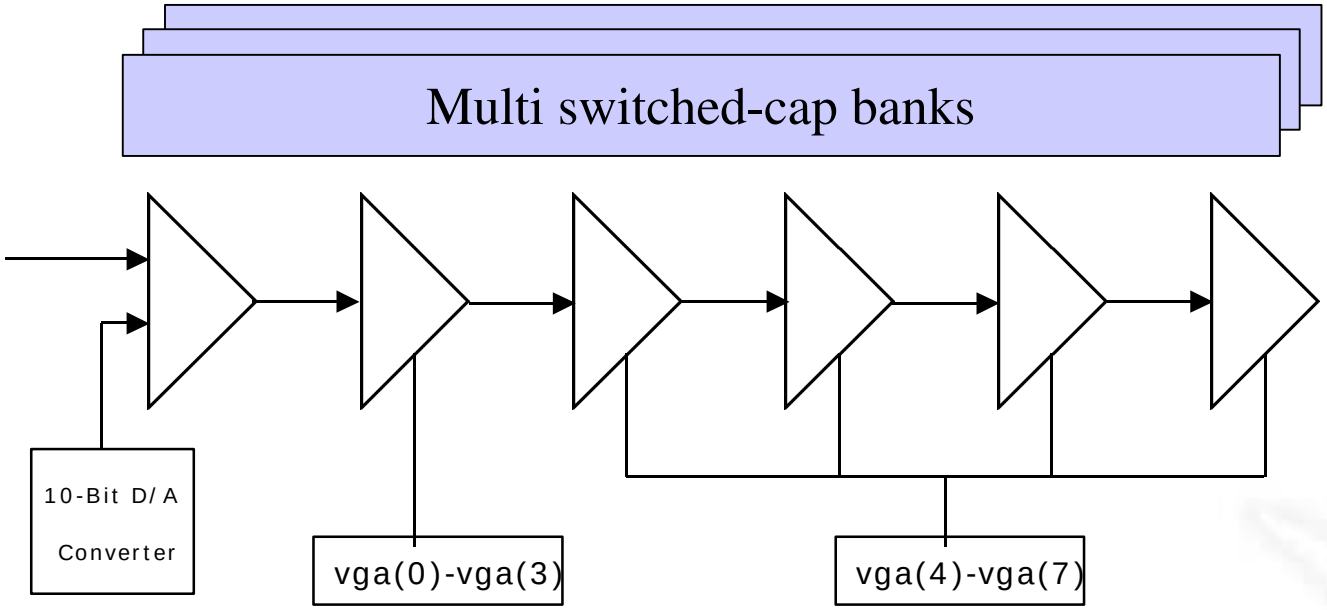
NC1250 - Analog Front End



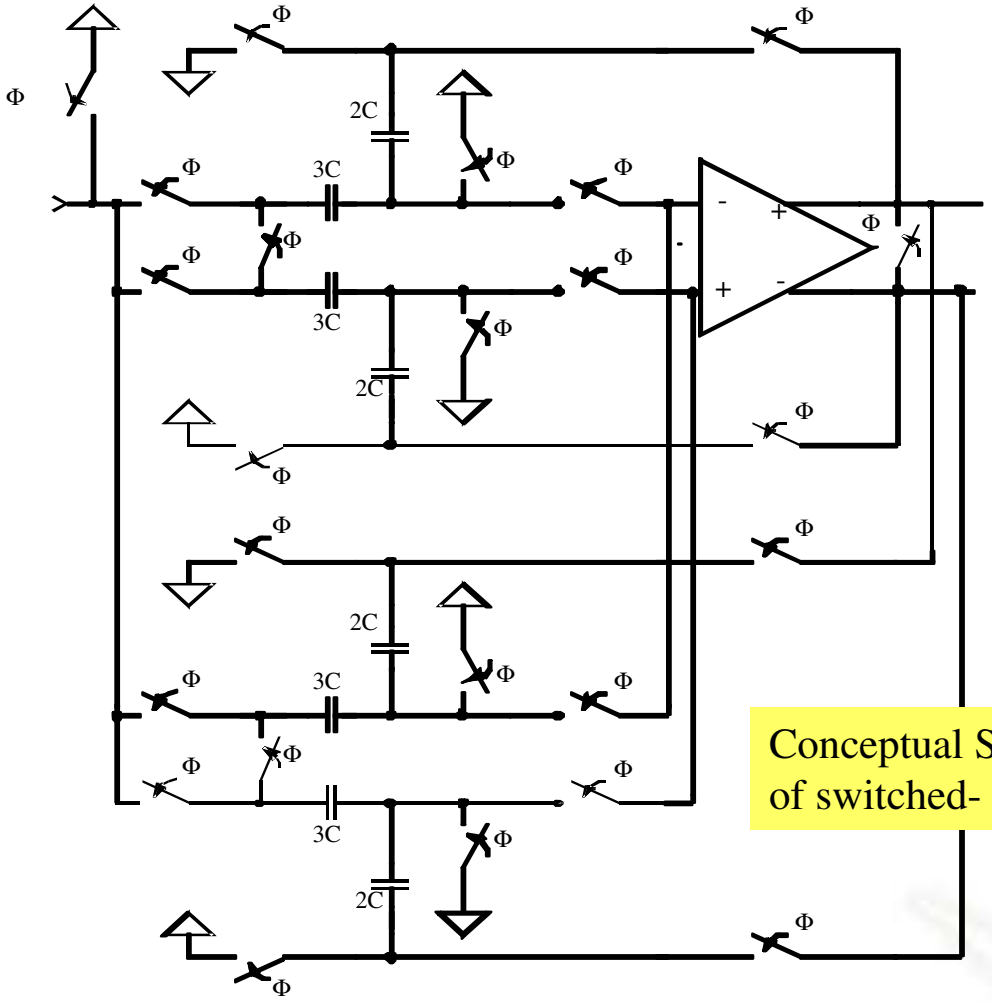
NDX Circuit Techniques
for Fast Gain Changes on the fly

- Switched-capacitor circuits for analog signal processing
- Multi switched-capacitor banks with shared opamps
- Crosstalk minimization
- Power/performance trade-off:
  - stage scaling
  - programmable bias level

NDX CDS/PGA Architecture



NDX CDS/PGA Architecture



Conceptual Scheme of a part of switched- cap. banks

12-bit 50 MS/s ADC

- Pipeline architecture
- Auto-calibration and digital correction
- DNL, INL < 1 LSB
- SNR >TBD dB
- THD < -TBD dB
- Internal reference generator and buffers

ADC Circuit Techniques for 12-bit 50 MS/s

- Switched-capacitor circuits for analog signal processing
- Dual switched-capacitor banks with shared opamps
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- Power/performance trade-off:
  - stage scaling
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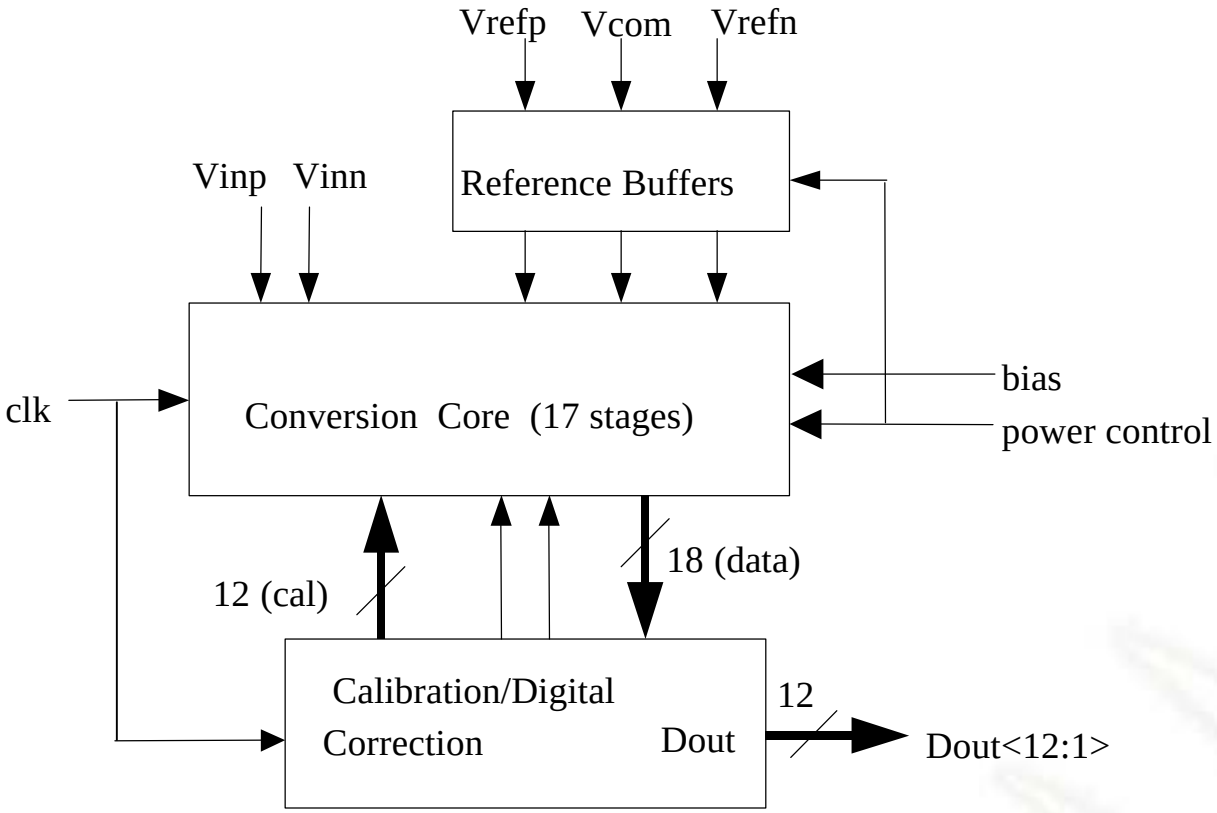
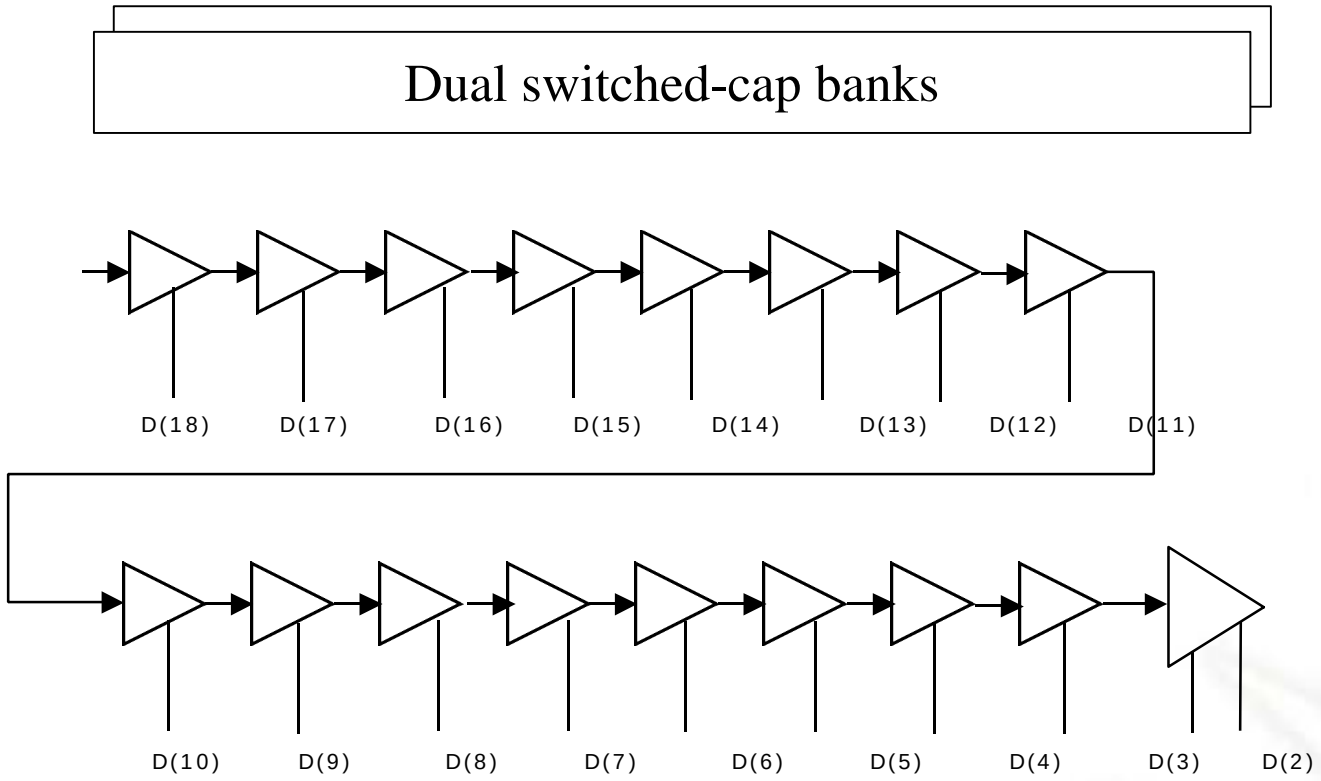
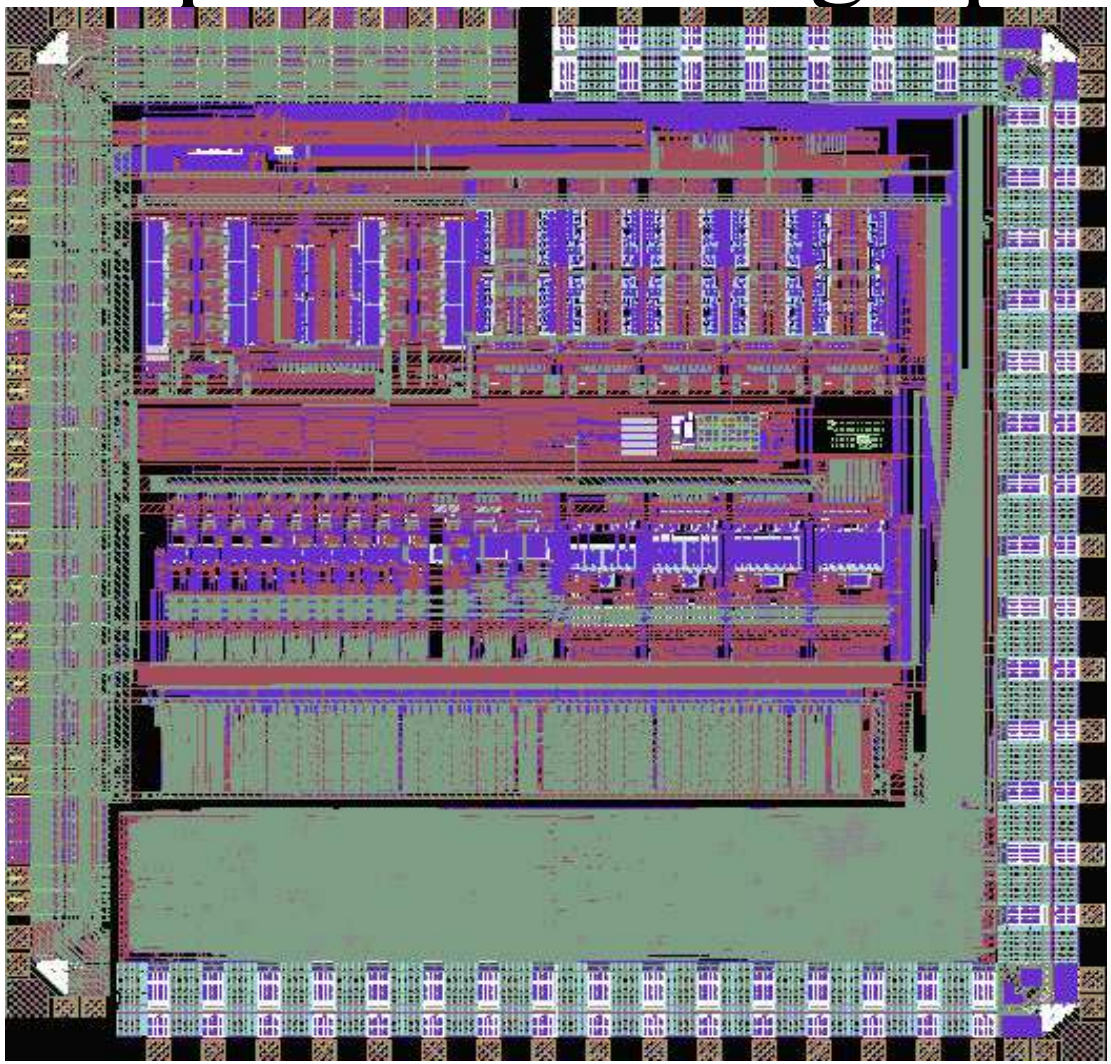
ADC Architecture



ADC Architecture



Chip Photomicrograph



Sample Image

Summary

- 12-bit 50 MS/s digital image acquisition system
- Up to 4 color specific gain setting (complementary color scheme compatible)
- Very low power design (120 mW~50mW)
- Overall system SNR > 60 dB

World Fastest AFE;12-bit, color by color PGA enables High Definition DSC & DVC