



SiRF

SiRFstar™ II ARCHITECTURE:

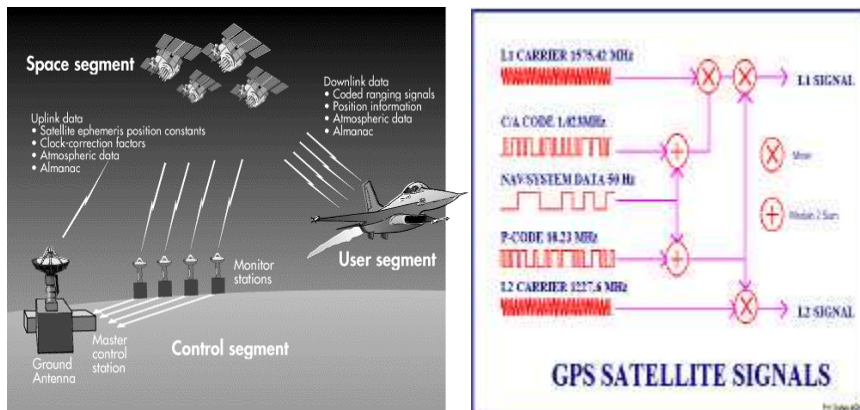
A POWERFUL SYSTEM PLATFORM
for
CONSUMER GPS APPLICATIONS

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SiRF Technology Inc.



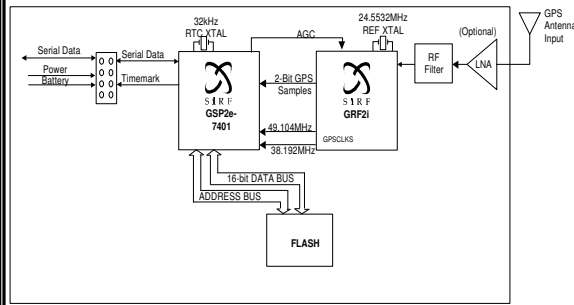
SiRF

GPS System Overview





Typical SiRFstar™ II Architecture

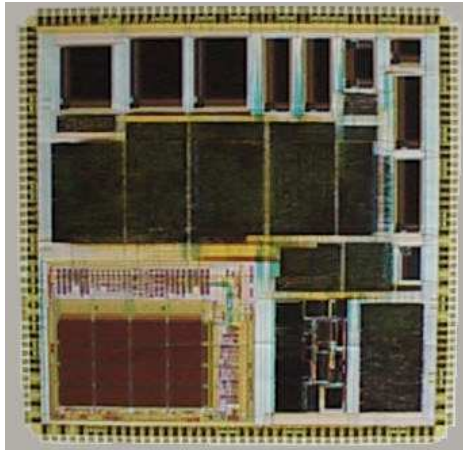


SiRFstar II Architecture

- ◆ GPS receiver footprints as small as 1" x 0.9"
 - < 50 total parts (35 are capacitors and resistors)
 - 1/3 of area is consumed by connectors and mounting holes
- ◆ GSP2: Digital Signal Processor
 - 400K effective gates including: CPU, RAM, Custom GPS DSP, Real Time Clock and I/O
- ◆ GRF2: RF section
 - Complete RF section with no external IF
- ◆ GSW2: Software
 - Designed to integrate with User software on built-in ARM CPU
 - ◆ Low GPS Throughput (~2 MIPS)
 - ◆ Low GPS Interrupt rate (100 ms, non-time critical)



GSP2



TECHNOLOGY SUMMARY

- ◆ Vendor 50 MHz ARM7-TDMI
- ◆ 1 Mbit Vendor EDO RAM
- ◆ P substrate and Triple Wells
- ◆ 4 Polys and 4 Metals
- ◆ Dual gate oxide 70/120 Å
- ◆ $L_{eff}=0.3/0.35\mu\text{m}$ for N/PMOS
- ◆ Custom ASIC Logic at 38 & 49 MHz
- ◆ Simulated at 2.5 to 3.7 V



GSP2 Challenges & Solutions

- ◆ Aggressive cost and size requirements - System-on-a-Chip
 - On board 50 MHz CPU and application RAM
 - Custom GSP DSP core and Satellite Signal Tracking Engine (SSTE)
 - ◆ Acquire, track, demodulate GPS signals without CPU assistance
 - Extensive GPS receiver peripherals
 - ◆ RTC, 2 UARTS, high speed serial bus, battery backed SRAM, > 40 GPIO
- ◆ Industry Leading GPS performance
 - Signal acquisition using 1920 time/frequency search channels
 - Satellite signal tracking engine to perform GPS acquisition and tracking functions without CPU intervention
 - Multipath-mitigation hardware
 - Wide Area Augmentation System (WASS) channel
 - ◆ Rate 1/2, k=7 convolutional decoder at 500 BPS
 - ◆ Horizontal position fix error < 10 m 2-d RMS
 - U.S. Coast Guard DGPS Beacon Signal Processor
 - ◆ Tracking loops & demodulation hardware for 300 KHz, 200 BPS MSK data
 - ◆ Horizontal position fix error < 5 m 2-d RMS

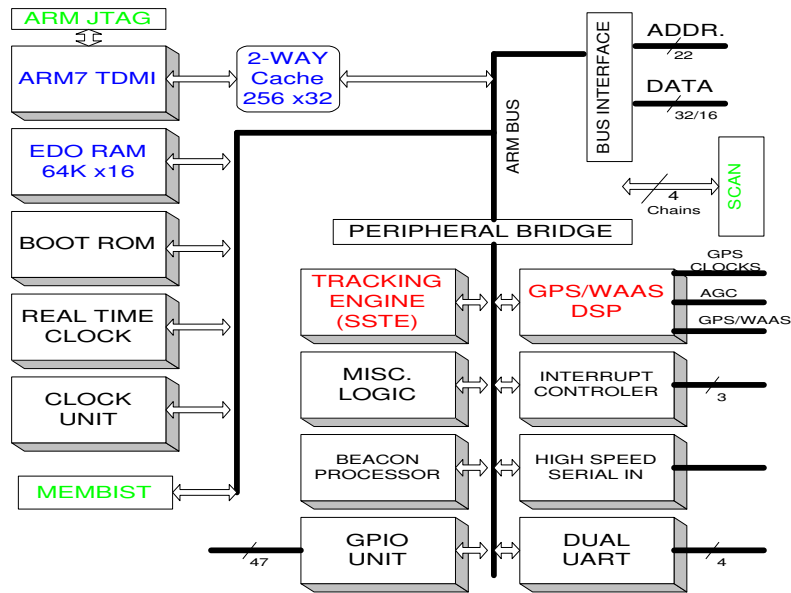


GSP2 Challenges & Solutions

- ◆ Low Power
 - High integration
 - Advanced power management for power saving and stand-by modes
 - Extreme low power in power down mode, but capable of very fast starts
 - ◆ < 350 mW continuous
 - ◆ Advanced TricklePower™ mode for power savings to 98% with no extra parts
- ◆ High Quality (> 99% effective fault coverage)
 - End-to-end simulation
 - ARM7TDMI with JTAG interface
 - EDO DRAM memory with Built-in-self-test (BIST)
 - SRAM with BIST
 - Full scan design-for-testability
 - Sample quality first spin silicon

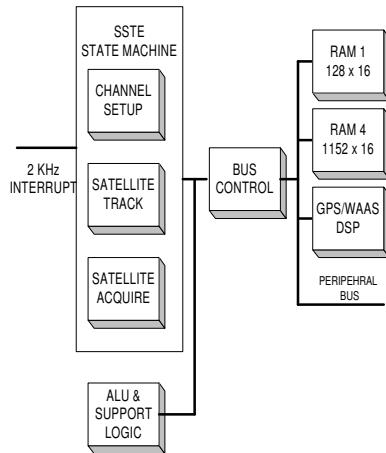


GSP2 Functional Block Diagram





Satellite Signal Tracking Engine (SSTE)

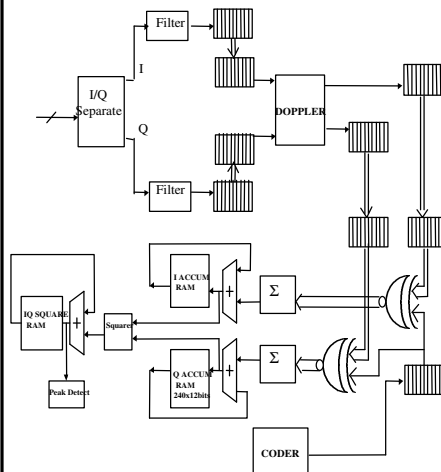


SSTE FEATURES

- ◆ All Acquisition / Tracking Tasks
- ◆ Reduces SW Interface to 10 Hz
- ◆ Programmable
 - Acquisition Sensitivity
 - ◆ 0.01 to 1000 Hz Search Rate
 - Loop Order
 - ◆ 1 or 2 Order AFC
 - ◆ 2 or 3 Order Costas
 - ◆ 1 or 2 Order Code
 - Loop Bandwidths
 - ◆ 0.125 to 8 Hz AFC Loop
 - ◆ 4 to 64 Hz Costas Loop
 - ◆ 0.03 to 8 Hz Code Loop
 - Data Rate
 - ◆ 50 Hz or Slower Ranges



GSP2 GPS/WAAS DSP



GSP2 DSP FEATURES

- ◆ Custom, Patented, DSP Hardware
- ◆ 1920 Acquisition Taps or 12 Parallel 48 MHz Channels
- ◆ 2,000 MIPS (Equiv.) Throughput, Power Consumption for <48 MHz
- ◆ GPS + WAAS Capability
- ◆ Multipath-mitigation hardware < 50 ns sensitivity
- ◆ Programmable Coherent/Non-coherent Integration Capability with Signal Detection Hardware



GSP2 Performance/Current

TTFB Performance

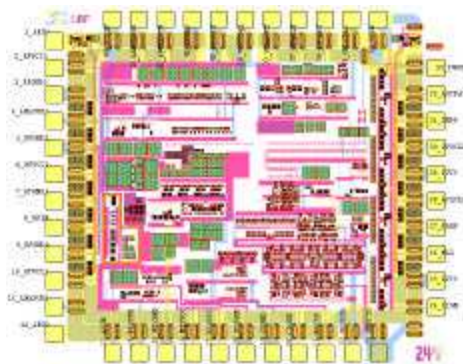
Mode	TTFB(Sec)
Cold Start	<= 45
Warm Start	<= 38
Hot Start	< 2
Reacquisition	<= 0.2

Current

Mode	Current @ 3.3V
Normal	< 75 mA
Standby	< 1 mA
Power Down	< 2.5uA
TricklePower™	
1 Hz	< 25 mA
2 Hz	< 15 mA
Push-to-Fix	~1 mA



GRF2



TECHNOLOGY SUMMARY

- ◆ 6" wafers, Non-epi BiCMOS
- ◆ 3 Metal Layers
- ◆ 0.6um x 1.8 um emitter
- ◆ 0.44um CMOS, Tox=85A
- ◆ Tested at 2.7 to 3.7 V
- ◆ Input: 50 Ω , 1575.42 MHz RF
- ◆ Output: Single ended PECL, 2-bit A/S samples at 38.192 MHz with 9.548 MHz IF

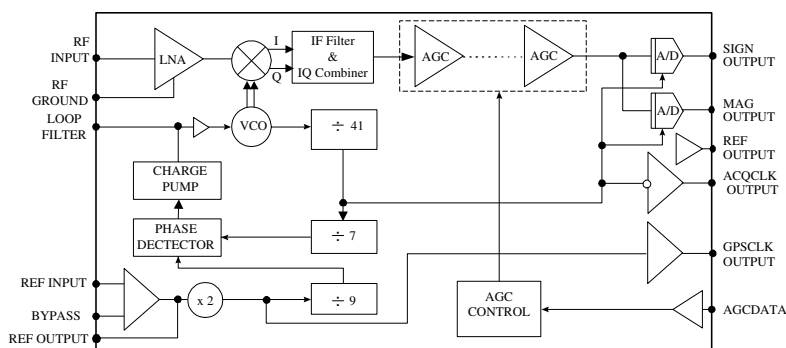


GRF2 Challenges and Solutions

- ◆ High Integration
 - Integrated LNA
 - ✦ Noise figure < 4.5 dB
 - ✦ Minimize matching components, $S_{11} < -15\text{dB}$
 - Integrated IF Filter & Image Reject combiner
 - ✦ No external parts
 - ✦ Image Rejection > 20 dB
- ◆ Low Cost Process / Product
 - Fabricate in a non-epi BiCMOS process
 - Minimize die size to reduce per unit cost
 - 7mm body plastic 48-pin LQFP
 - Low cost, 20 to 30 MHz RF Filter for Broadband Noise Rejection
- ◆ Marketing required backwards compatibility with SiRFstar I
 - Retained sample bandwidths, sample rate and clock rates
 - ✦ 1575.42 MHz, 50 Ω balanced pair input
 - ✦ 38.192 MHz, 2-bit, PECL outputs with an IF of 38.192/4 MHz



GRF2 Block Diagram





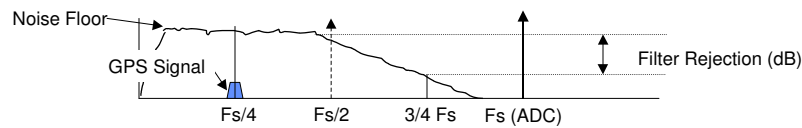
Integrated IF Filter

◆ Challenge:

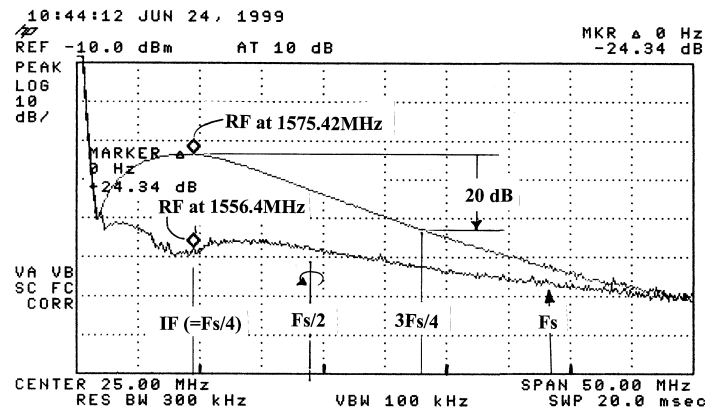
- Filter frequency setting elements R and C have +/- 15% tolerances
 - ◆ Filter center or cutoff can range from: 0.75 to 1.38 times nominal
- Filter must work over worst-case process corners

◆ Approach:

- Sample rate $F_s=38.19\text{MHz}$ and Sample IF = 9.548 MHz for compatibility with digital processing
- Set IF center to $F_s/4 = 9.5\text{MHz}$
 - ◆ IF Filter image rejection at $3/4 F_s$.
 - ◆ IF filter rejection = $[(\text{Gain}@9.5\text{MHz})/(\text{Gain}@28.5\text{MHz})]$



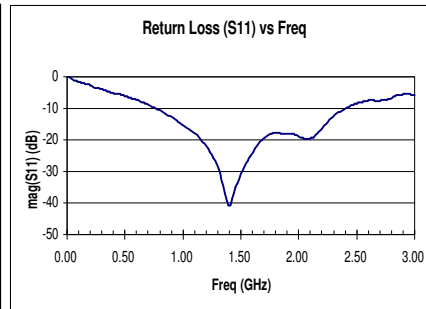
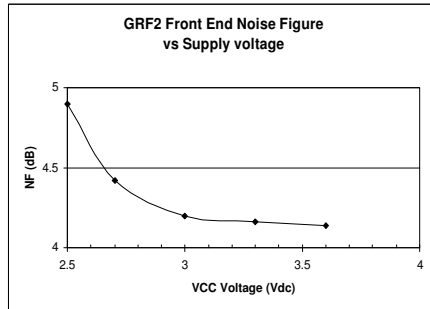
IF Filter & Image Rejection Performance



- ◆ Top trace: IF Filter frequency response
- ◆ Bottom trace: RF Image Reject response



GRF2 LNA Performance

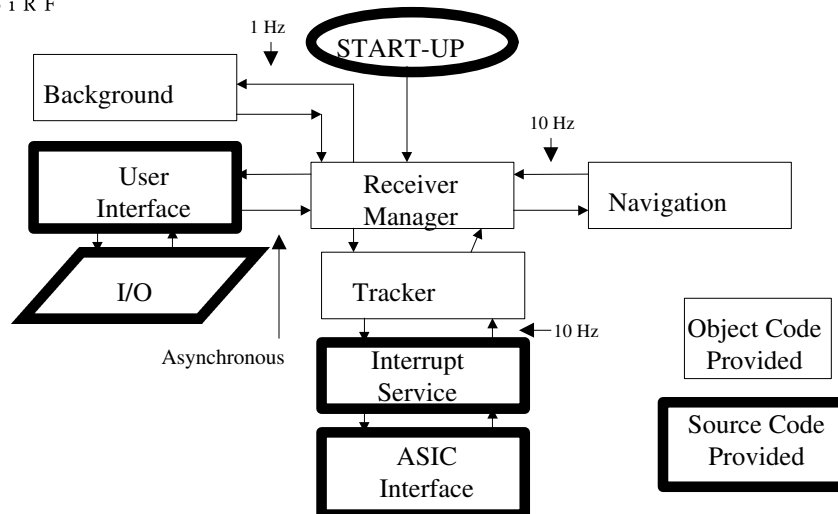


- ◆ Noise Figure (up to ADC)
 - Front end noise figure NF < 4.5dB for normal Vcc operating range

- ◆ RF Input Return Loss
 - S11 @ 1.575GHz < -20dB without ext. matching elements



GSW2 Software Organization





GSW2 Software Features

- ◆ > 90 % of throughput available to user software
 - 2 MIPS used by GSW2
- ◆ Low Rate CPU interrupts
 - 100 ms non-time critical interrupt rate
 - Easy to integrate with User's application software
- ◆ Flexible Operating Systems
 - User supplied OS or SiRF minimalist OS
 - GPS can schedule User Tasks (GPS Major)
or User Tasks can schedule GPS (GPS Minor) at low priority
 - "Stub" tasks provided for 1ms, 10 ms, 100 ms and 1s User Functions
- ◆ Flexible I/O System Source Code Provided
 - Users can easily implement own I/O messages and protocols