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# AMD Athlon™ Northbridge with 4x AGP and Next Generation Memory Subsystem

Chetana Keltcher, Jim Kelly, Ramani Krishnan,  
John Peck, Steve Polzin, Sridhar Subramanian,  
Fred Weber

Advanced Micro Devices, Sunnyvale, CA

\* AMD Athlon was formerly code-named AMD-K7

# Outline of the Talk

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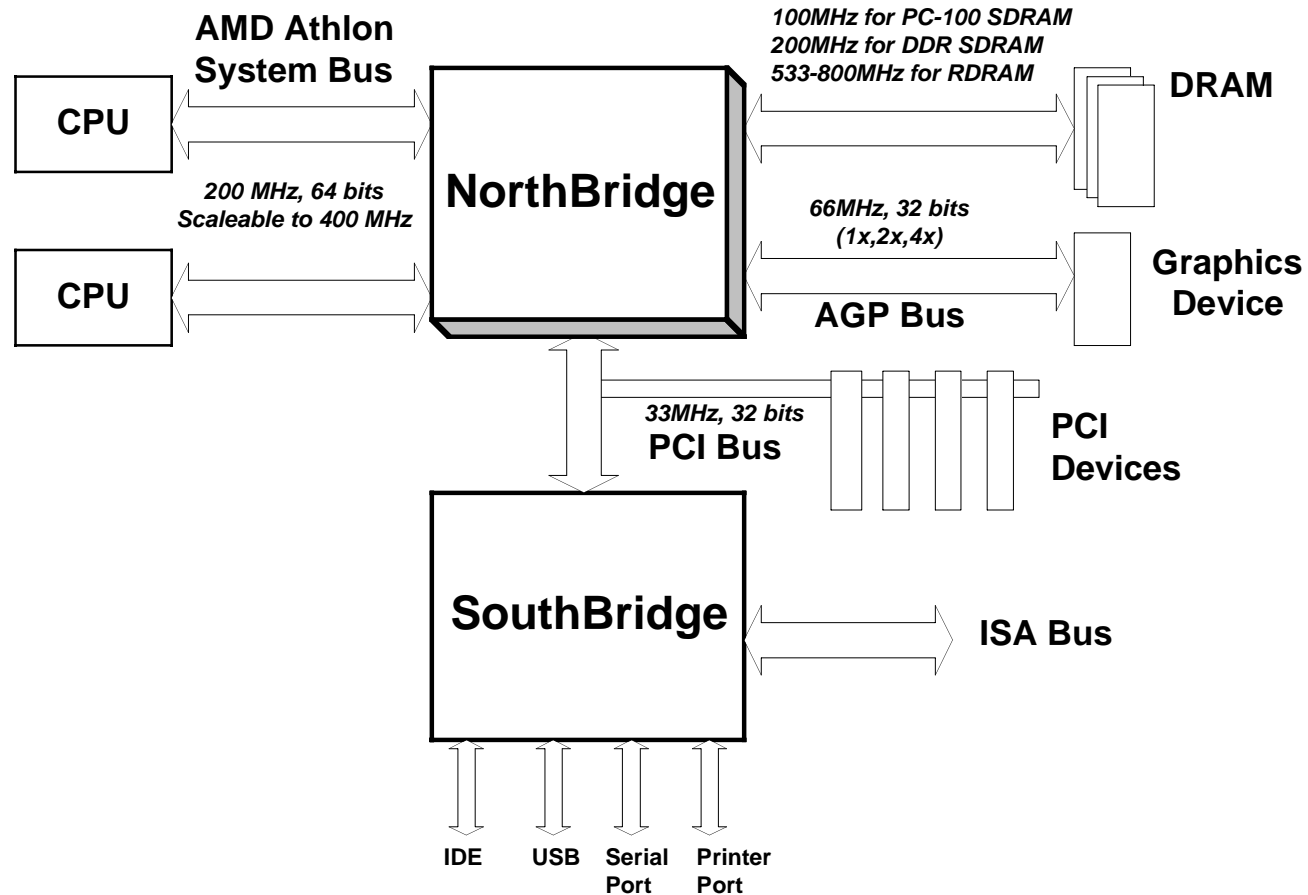
- Introduction
- Architecture
- Clocking and Gearbox
- Performance
- Silicon Statistics
- Conclusion

# Introduction

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- NorthBridge: “Electronic traffic cop” that directs data flow between the main memory and the rest of the system
- Bridge the gap between processor speed and memory speed
  - Higher bandwidth busses
    - Example: AGP 2.0, EV6 and AMD Athlon system bus
  - Better memory technology
    - Example: Double data rate SDRAM, RDRAM

# System Block Diagram

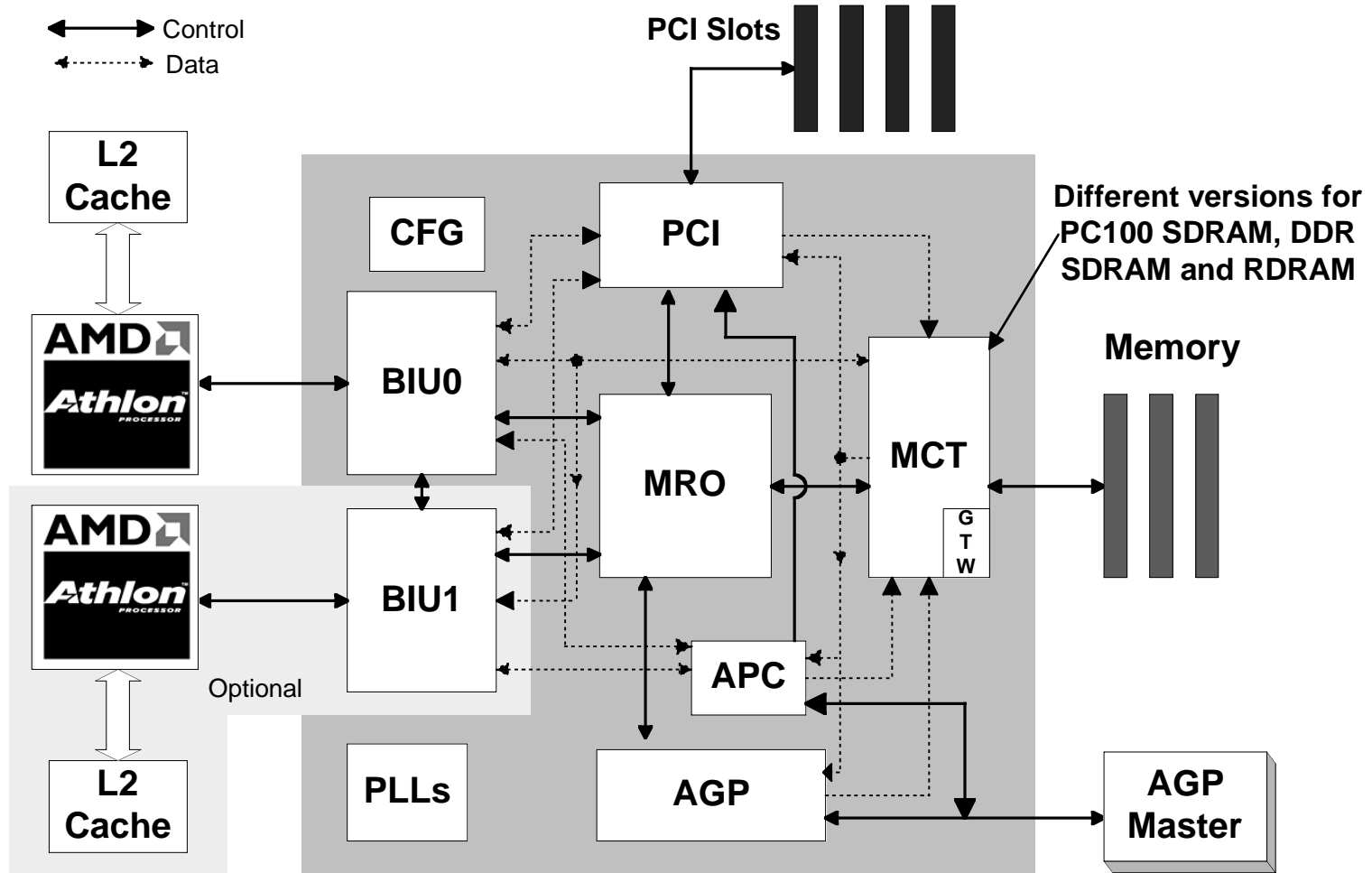


# Features of the AMD Athlon Northbridge

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- Can support one or two AMD Athlon or EV6 processors
- 200MHz data rate (scaleable to 400MHz), 64-bit processor interface
- 33MHz, 32-bit PCI 2.2 compliant interface
- 66MHz, 32-bit AGP 2.0 compliant interface supports 1x, 2x and 4x data transfer modes
- Versions for SDRAM, DDR SDRAM and RDRAM memory
- Single bit error correction and multiple bit error detection (ECC)
- Distributed Graphics Aperture Remapping Table (GART)
- Power management features including powerdown self-refresh of SDRAM and PCI master grant suspend

# Architecture

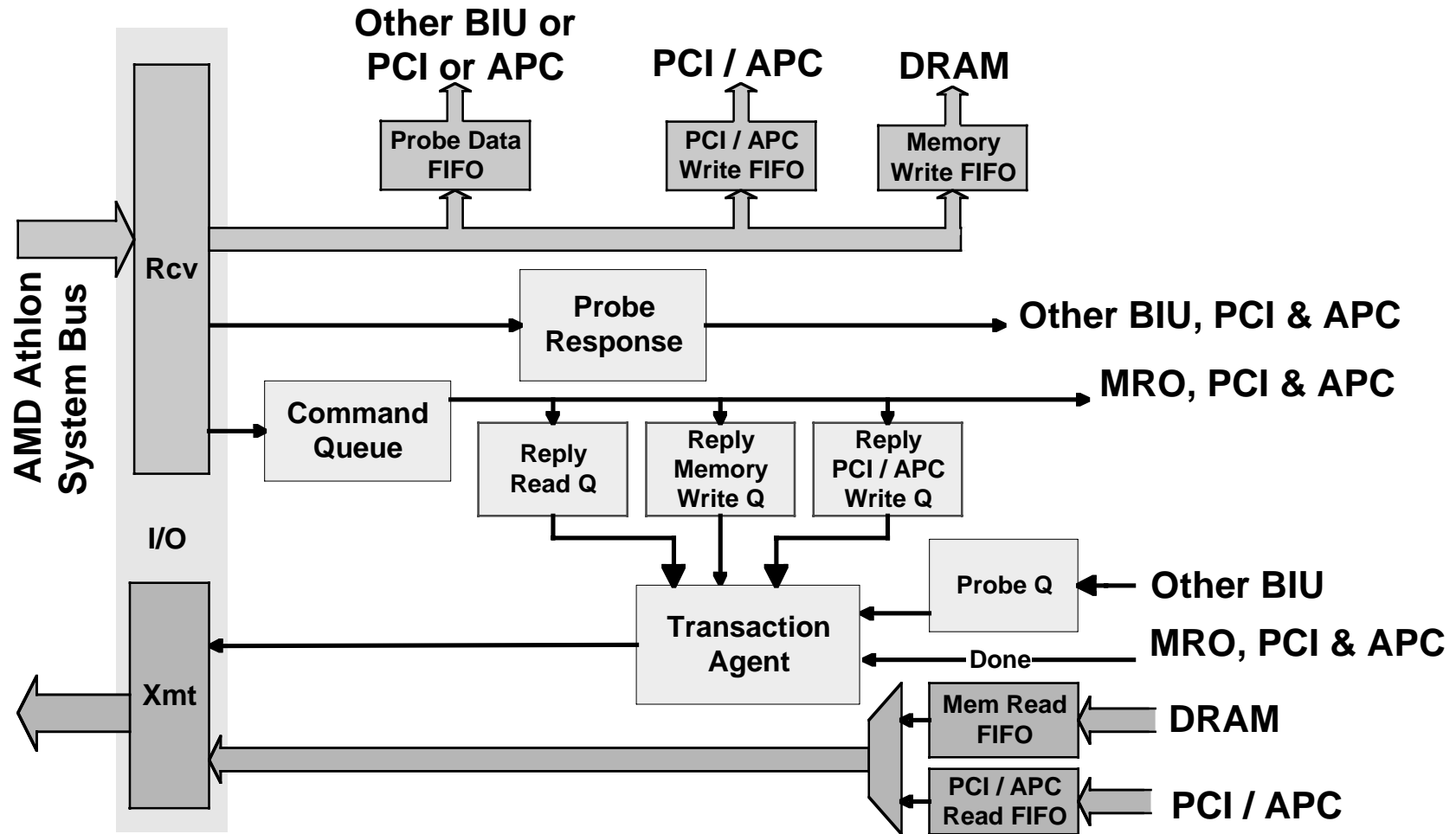


# Bus Interface Unit (BIU)

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- Processor interface; one per processor
- The AMD Athlon Front side bus:
  - high performance point-to-point bus
  - non-multiplexed command, address, data and reply/snoop interfaces
  - double-data rate transfers on address and data busses
  - split transaction bus: up to 24 outstanding operations per processor
  - source synchronized clocking to compensate for PC board propagation delays

# BIU Block Diagram



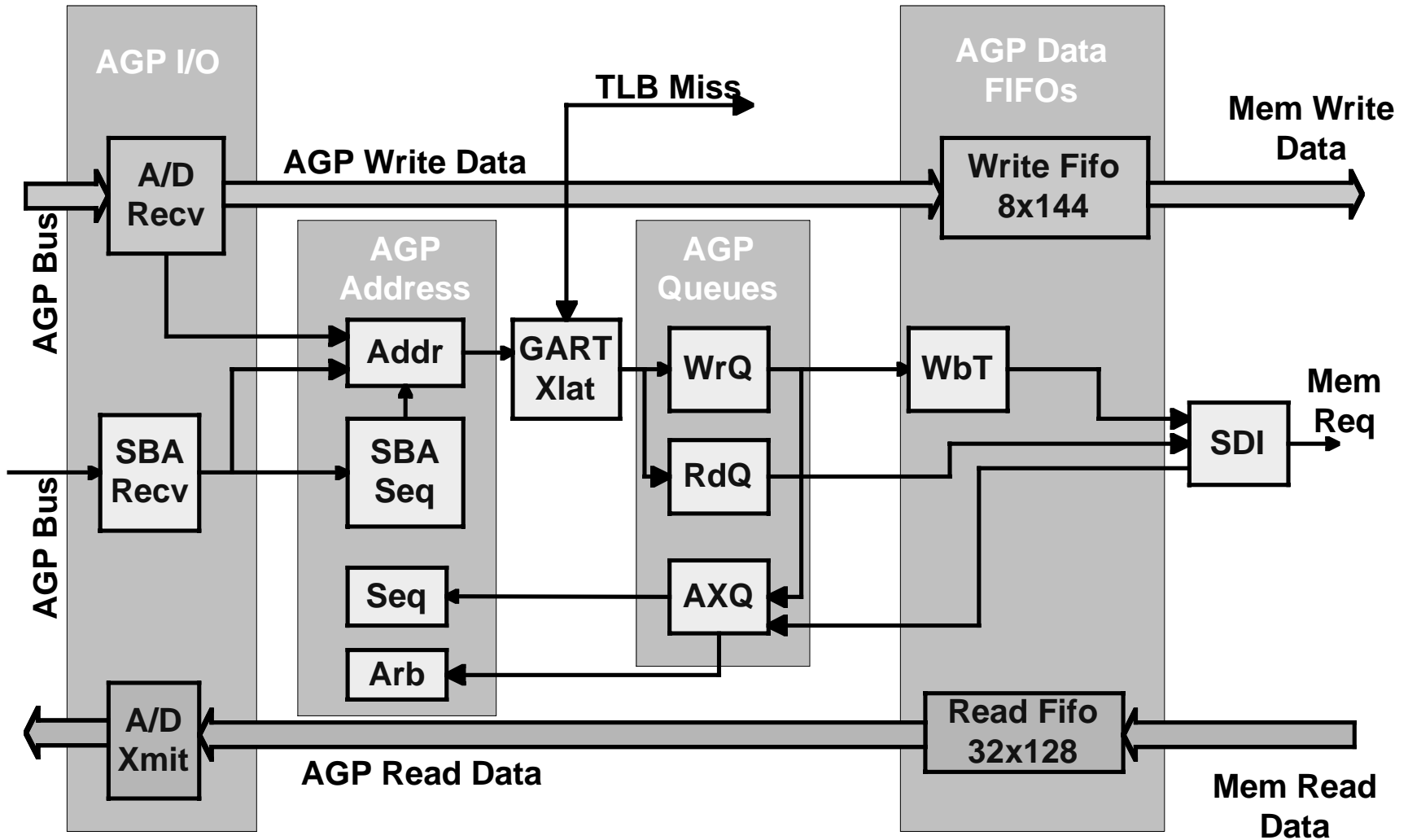


# Accelerated Graphics Port (AGP)

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- 1x, 2x and 4x data transfer rates in pipelined and side band addressing (SBA) modes
- Fast Write implementation for CPU to AGP master write transfers
- Distributed GART mechanism using 3 fully associative translation lookaside buffers (TLBs)
- Dynamically compensated AGP 2.0 compliant I/O buffers
- Independent R/W data buffers
  - Reordering of high priority over low priority transactions

# AGP Block Diagram



# PCI Controller

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- The PCI arbiter supports five external PCI masters plus the SouthBridge
- PCI to memory traffic is coherent w.r.t. the processor caches
- Consecutive processor cycles to sequential PCI addresses are chained together into one burst PCI cycle
- Same controller block is instantiated to handle the AGP PCI Protocol (APC block)

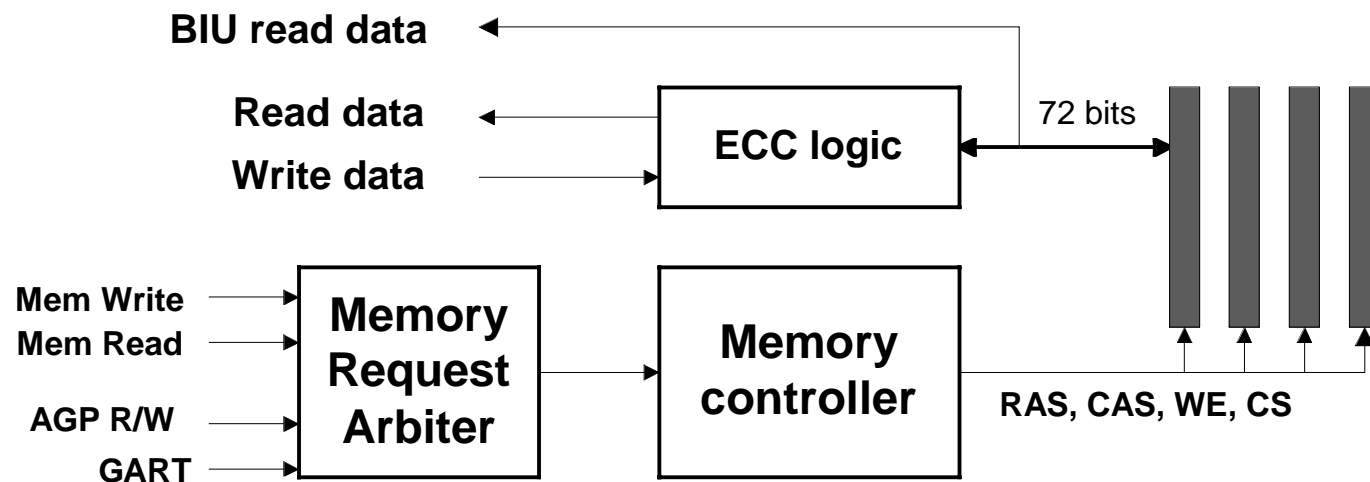
# Memory Request Organizer (MRO)

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- Request crossbar responsible for scheduling memory read and write requests from CPU, PCI and AGP
- Serves as the coherence point
- Requests are reordered to minimize page conflicts and maximize page hits
- Anti-starvation mechanism by aging of entries
- Arbitration bypassed during idle conditions to improve latency

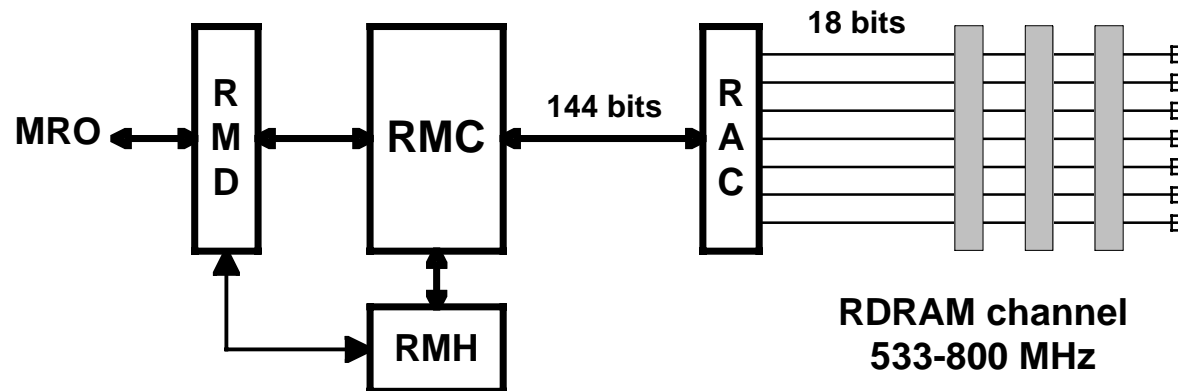
# SDRAM Memory Controller

- Controls up to 3 PC100 SDRAM or 4 DDR SDRAM DIMMs. 16, 64, 128 and 256Mb densities supported
- Open page policy with 4 banks open
- Peak bandwidth = 800MB/sec (PC100 SDRAM), 1.6GB/sec (DDR)



# Rambus Memory Controller

- One 16-bit RDRAM channel with upto 32 devices distributed across 3 RIMMs. 64, 128 and 256Mb densities supported
- Rambus RMC uses a closed page policy, but can keep banks open with special chained commands
- Memory address mapped to reduce adjacent bank conflicts
- Peak bandwidth = 1.6GB/sec using 800MHz RDRAMs

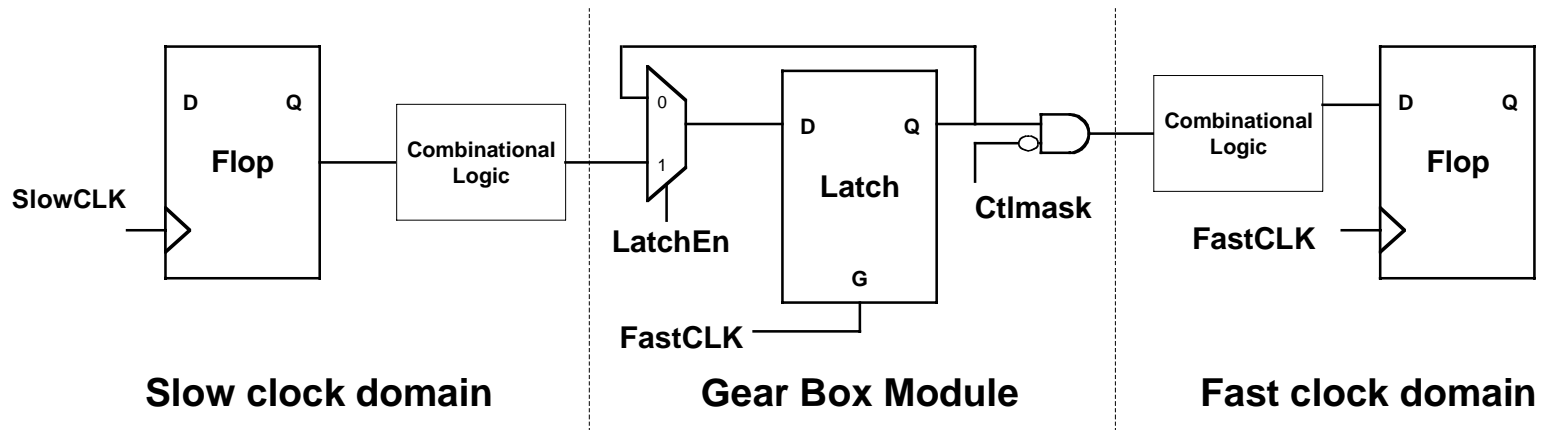
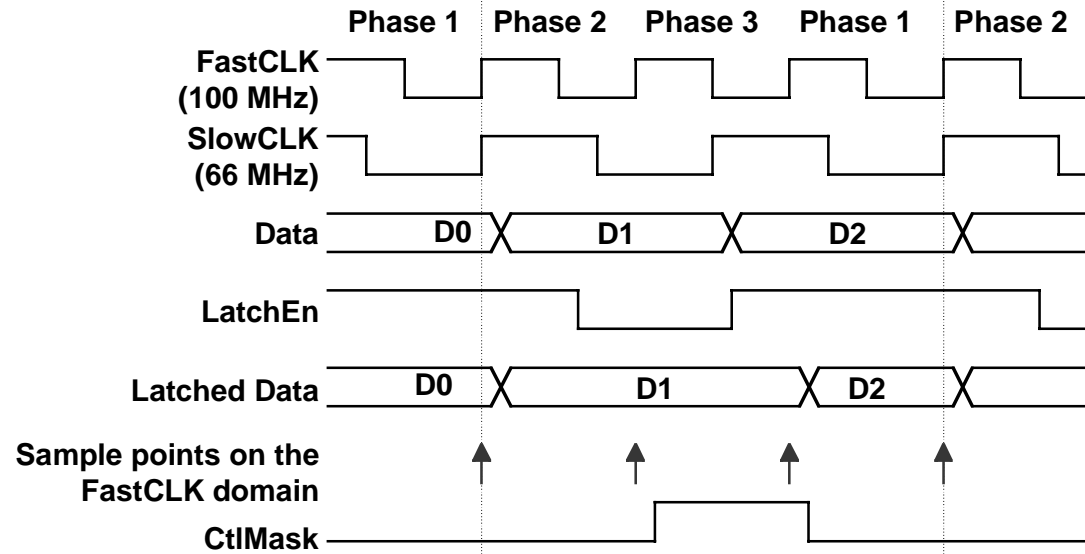


# Clocking and Gear Boxes

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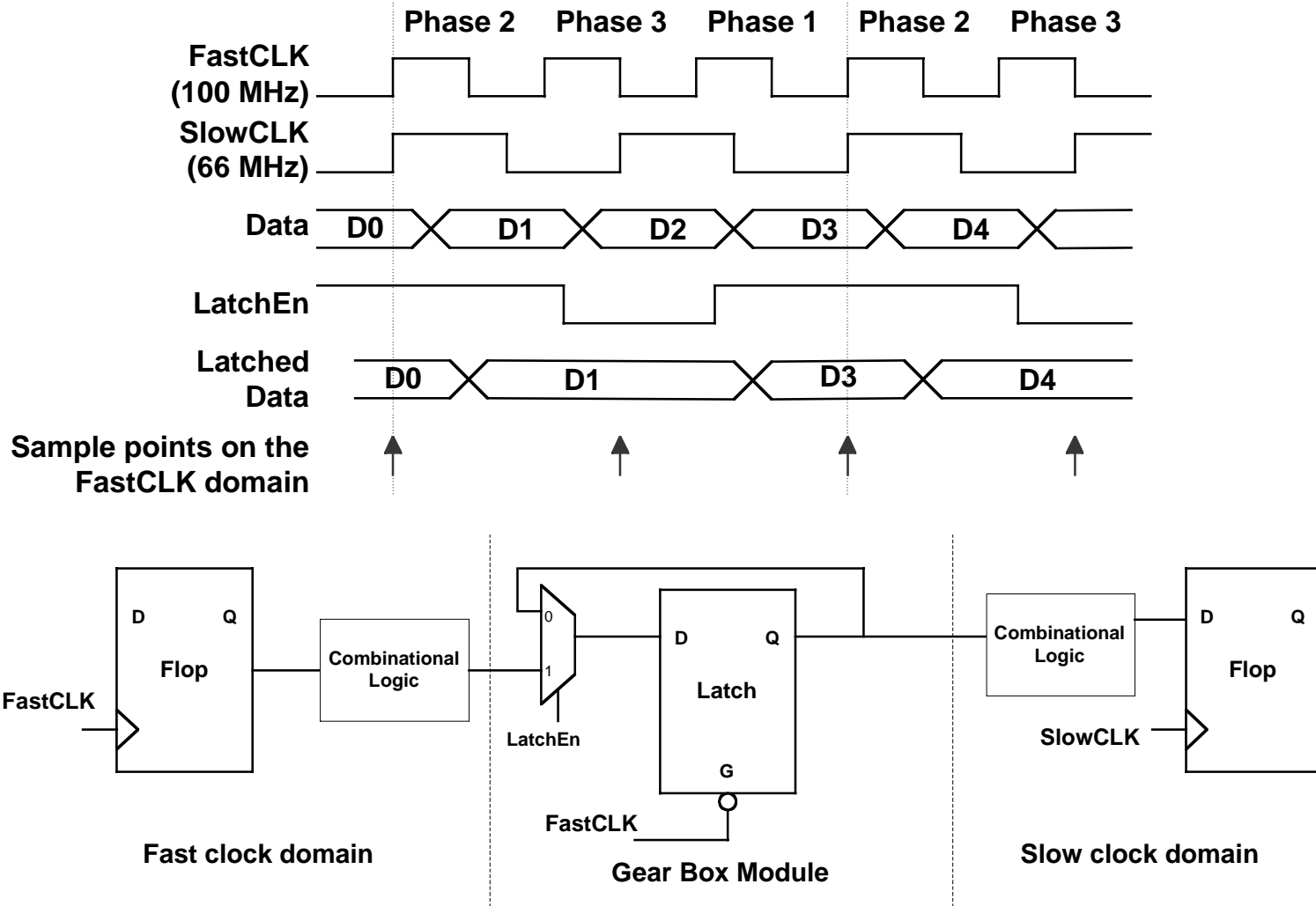
- Many clock domains have to be supported
  - 66 MHz peripheral (PCI and AGP) logic clock
  - 66 / 133 / 266 MHz 1x / 2x / 4x AGP clock
  - 66 / 100 / 133 MHz Core logic clock, AMD Athlon bus clock and SDRAM clock
- Gear box logic is used to synchronize data transfers between two clock domains
- The gearbox logic is correct by design for holdtime across clock domains
- The Rambus RAC synchronizes with the RMC using a different gearbox design

# Slow to Fast Clock Domain





# Fast to Slow Clock Domain

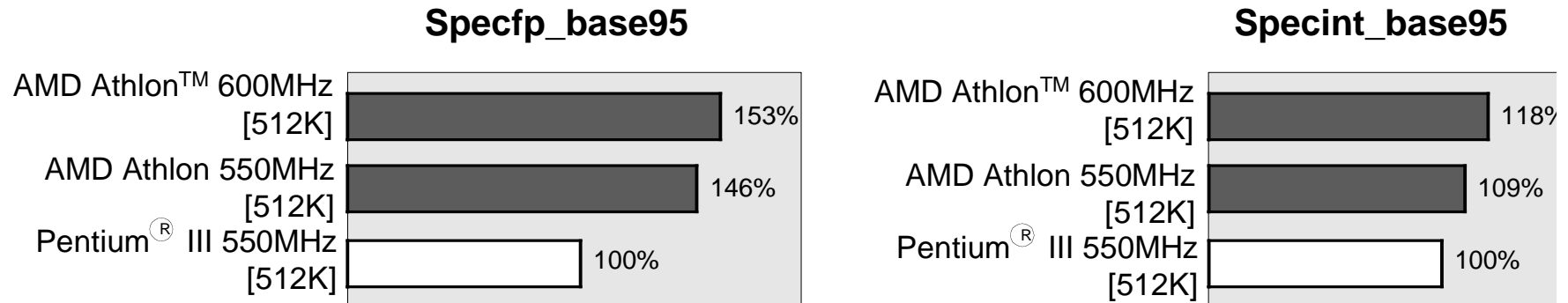


# Performance

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- Bypassing:
  - Can bypass MRO and BIU under low system loads for 25% reduction in latency of CPU reads from main memory
  - Overall performance boost equivalent to  $\sim 1/2$  CPU speed bin on Ziff-Davis WinBench<sup>®</sup> benchmark
- SPECint95 and SPECfp95 benchmarks on AMD Athlon and Pentium<sup>®</sup> III
  - 512K L2 cache, Single PC100 128MB DIMM
  - <http://www.amd.com/products/cpg/athlon/benchmarks.html>

# Performance



Normalized Pentium® III Performance = 1

Benchmark System Configuration: Diamond 770 using nVidia TNT2 Ultra 150MHz core, 183MHz memory clock 32MB, Western Digital Expert 41800, Single PC-100 128MB DIMM, SoundBlaster Live (Value) Audio, LinkSys HPN100 Ethernet card, Toshiba 6X DVD SD-M1212, Dual Boot Windows® 98 & Windows NT® 4.0 using Norton System Commander. Windows NT 4.0 is installed with SP4, Windows 98 with DX 6.1A build 2150, and nVidia TNT2 Ultra Driver Rev 1.81 under Windows 98 and Windows NT.

AMD Athlon™ processor-based system: Reference Motherboard Rev. B\*, Bios Rev AFTB00-2, Bus Mastering EIDE Driver v1.03, AGP miniport v4.41.

Pentium® III processor-based system: ASUS P2B Rev 1.02, BIOS Rev 1008 beta 4, EIDE-BM Driver 5/11/98, AGP miniport 5/11/98.

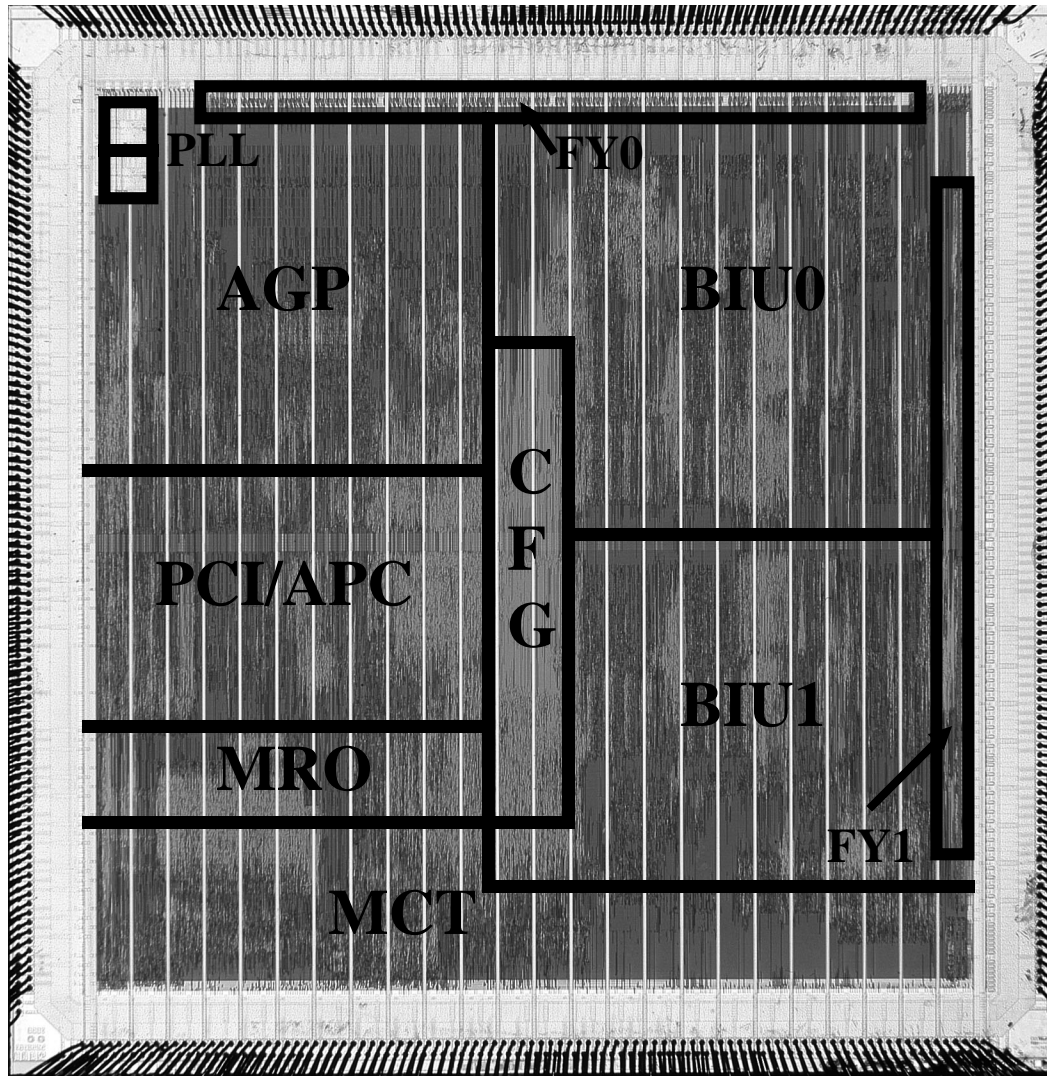
\* This motherboard is not commercially available at this time.

# Silicon Statistics

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Chip Version	Tech & Voltage	Max Core Speed	Die Size (pad limited)	No. of Pins
SDRAM, 1P, 2xAGP	0.35 $\mu$ , 3.3V	100 MHz	107 mm <sup>2</sup>	492
SDRAM, 2P, 2xAGP	0.35 $\mu$ , 3.3V	100 MHz	130 mm <sup>2</sup>	656
DDR, 1P, 4xAGP	0.25 $\mu$ , 2.5V	133 MHz	133 mm <sup>2</sup>	553
DDR, 2P, 4xAGP	0.25 $\mu$ , 2.5V	133 MHz		
RDRAM, 1P, 4xAGP	0.25 $\mu$ , 2.5V	133 MHz	107 mm <sup>2</sup>	492

# Die photo: SDRAM, 2P, 2xAGP



Approx. 500K gates  
11.43x11.43mm<sup>2</sup>

# Conclusions

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- Low cost, high performance system solution for the AMD Athlon processor - EV6 in a PC
- Multiprocessing architecture for workstation and server markets
- Design provides for a high degree of concurrency which optimizes throughput under heavy system loads
- Support three memory sub-systems:
  - PC-100 SDRAM
  - Double Data Rate SDRAM
  - Direct Rambus SDRAM