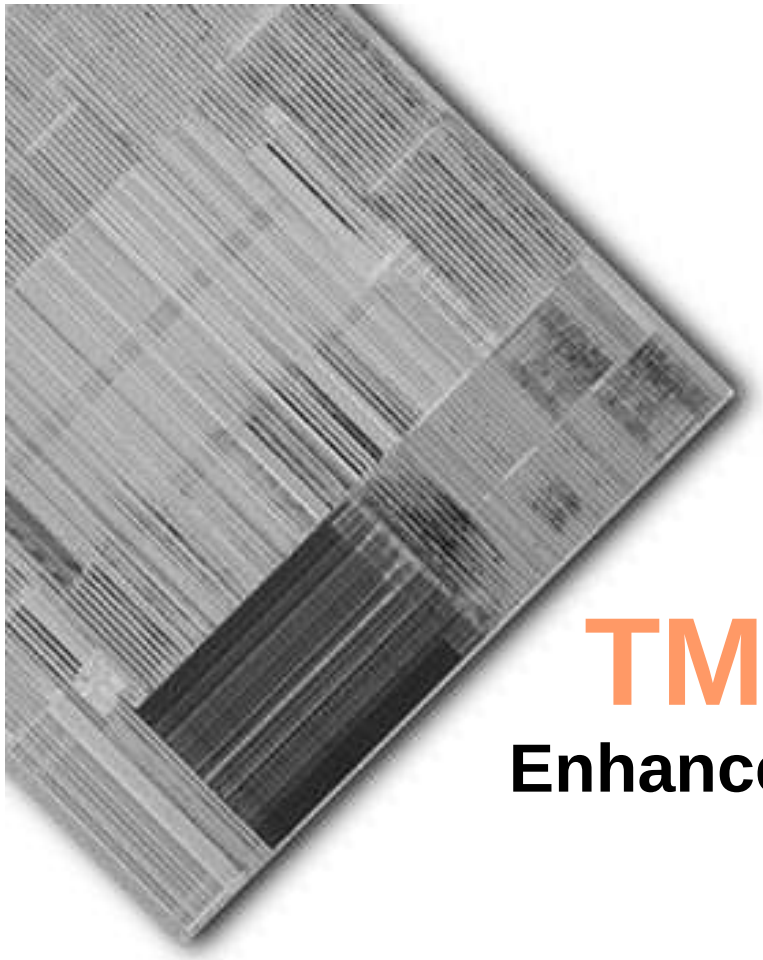

TriMedia

TM-1300 High-speed, Low-cost, Enhanced PCI, VLIW Media Processor

1999 Hot Chips Symposium

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Content

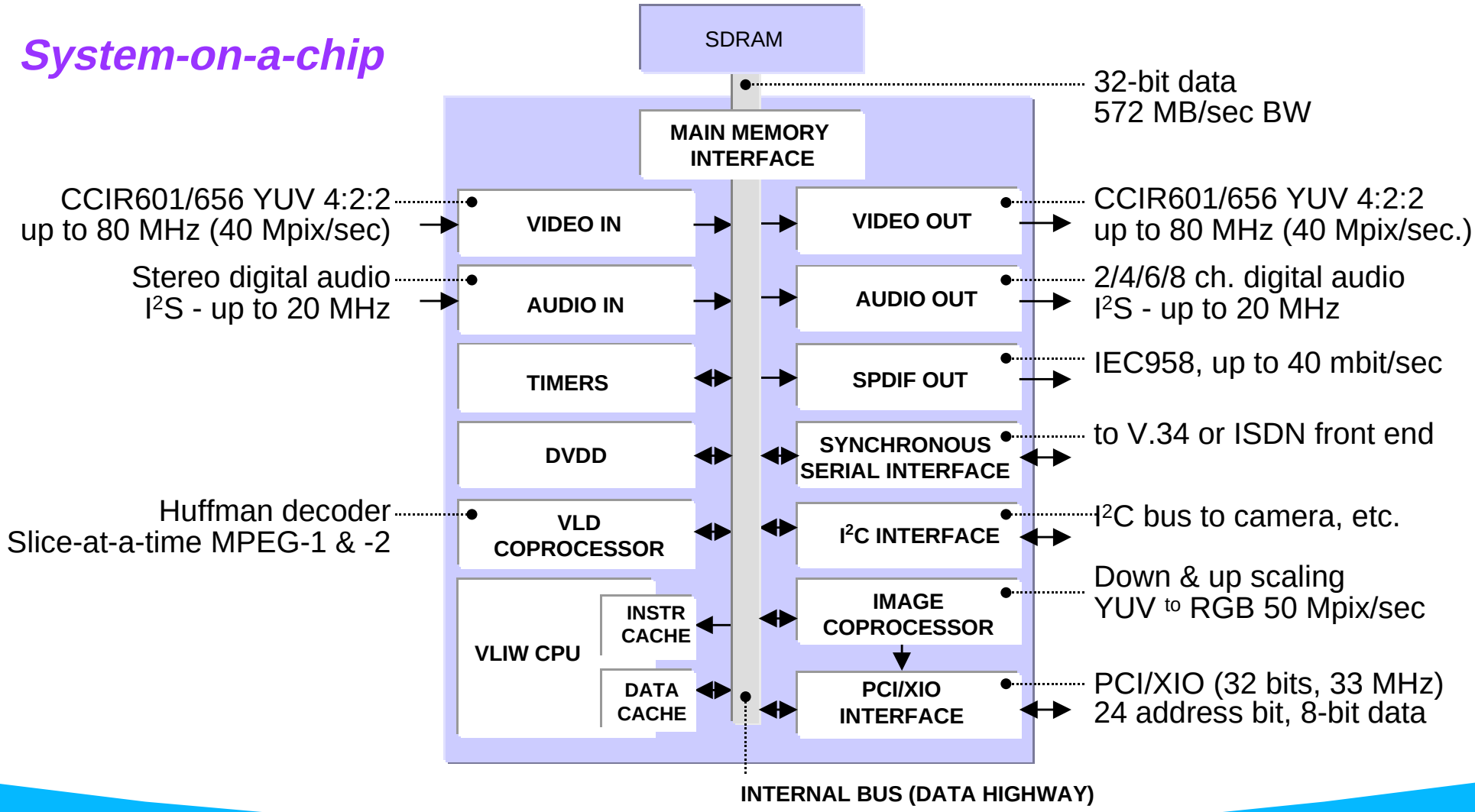
- Highlights
- Enhanced very-long instruction word (VLIW) engine
- System-on-a-chip
- Silicon information
- Conclusion

TM-1300 Applications

- Standalone or PC-based systems
- Video editing
- Videoconferencing (including modem)
- Security systems
- Digital television
- Set-top decoder/web browser
- DVD decoder
- Audio/Video en/de/transcode (Dolby AC-3®, MPEG)

TM-1300 Block Diagram

System-on-a-chip



TM-1300 System Software Support

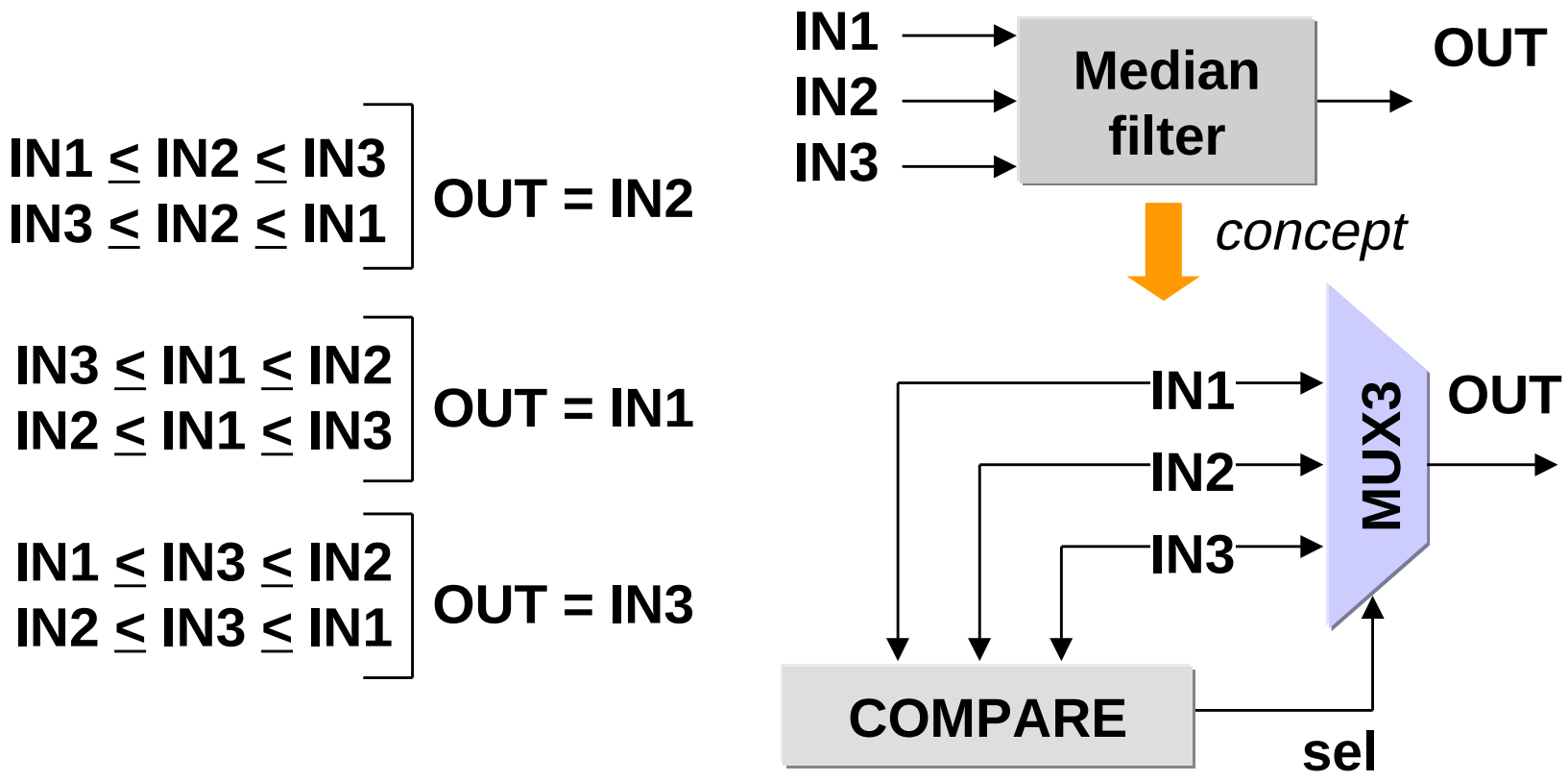
- Powerful C/C++ compiler
  - interprocedural analysis
  - automated in-lining, unrolling
  - shows an increase in performances up to 15%
- No assembly programming required
- pSOS+™ embedded, real-time kernels
  - code size: 130 KB
  - overhead : 5-10%
- Multiprocessor run-time and multitasking debug support
- Extensive multimedia library including several real-time video decompression standard packages

TM-1300 VLIW Highlights

- Instruction cache
  - 32-KB, 64-byte block size
  - 8-way set associative
  - contains compressed VLIW instructions
- Dual-ported data cache
  - 16-KB, 64-byte block size
  - 8-way set associative
- Up to 5 RISC operations per cycle
- Conditionally guarded operations
- Multimedia operation set (extended for median filter and 9-bit iDCT support)

Median Filter

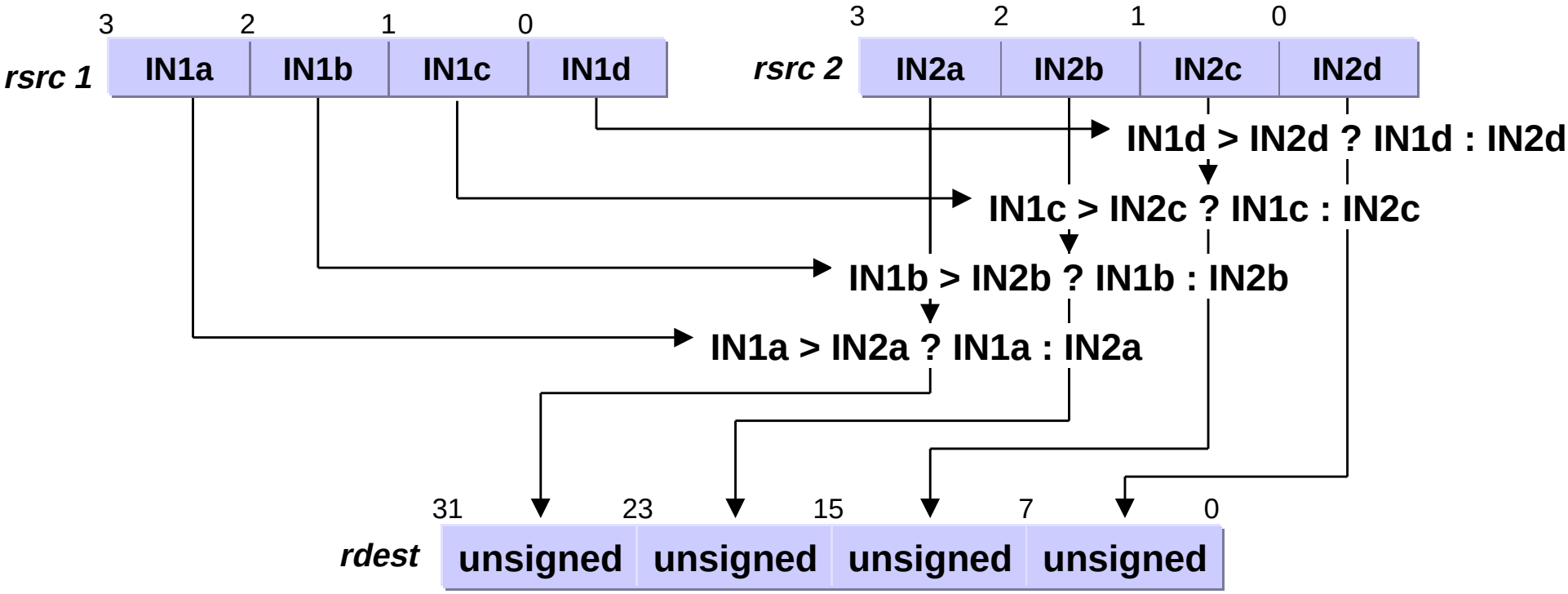
Used to De-Interlace a CCIR601 Resolution Video



Median Filter

Median Filter

- R0 = QUADUMIN(IN1, IN2)
- R1 = QUADUMAX(IN1, IN2)
- R2 = QUADUMAX(R0, IN3)
- MEDIAN(IN1, IN2, IN3) = QUADUMIN(R1,R2)

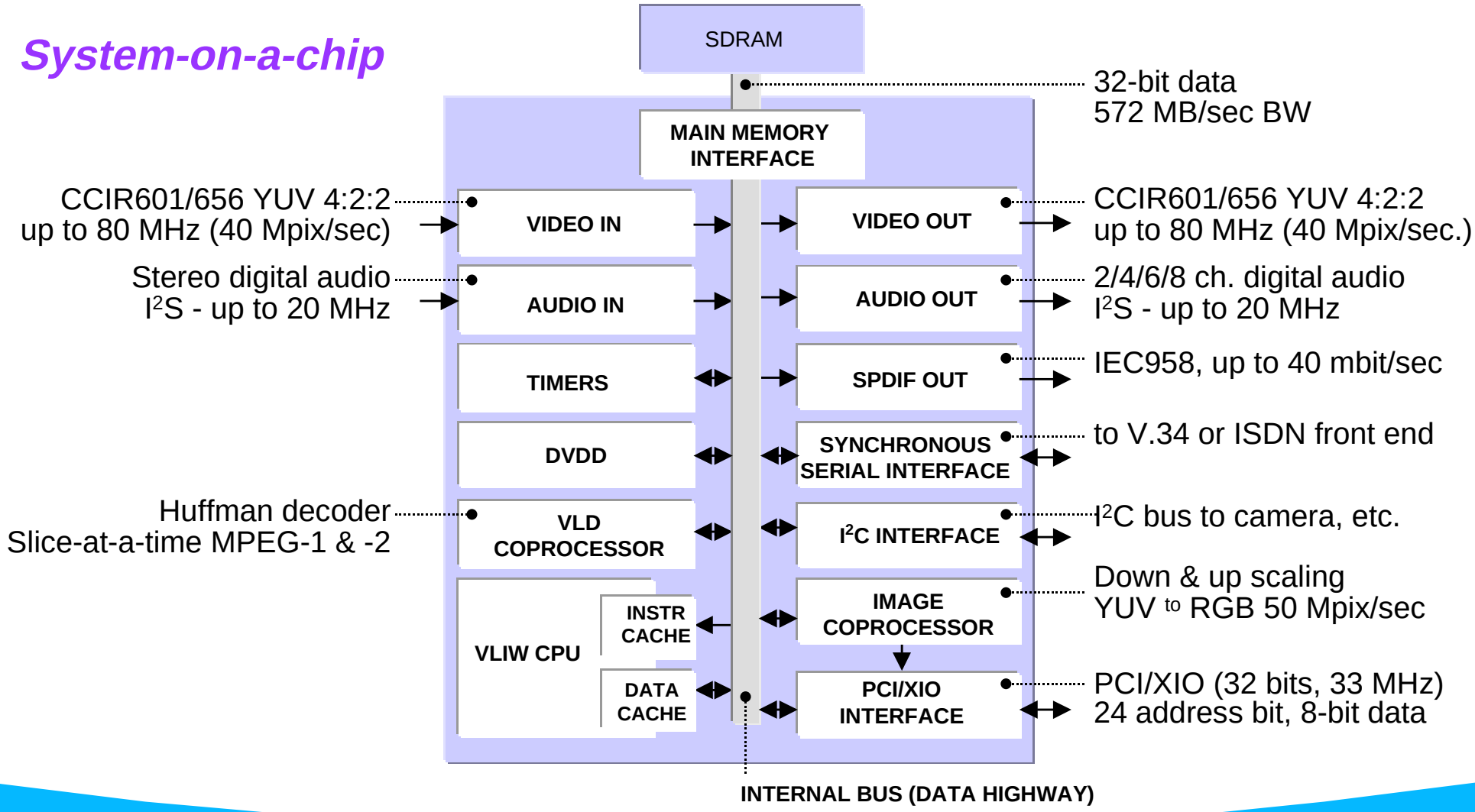


Performance Improvement

- Original TM-1000 requires 35 operations for 4 pixels; TM-1300 requires only 8 operations
- Reduces CPU load from 63% to 29% for the full application with only two new operations
- Similarly 9-bit precise iDCT has been improved by 11% using 4 new operations dualasr, dualiclipi, dualuclipi, mergedual16lsb

TM-1300 Block Diagram

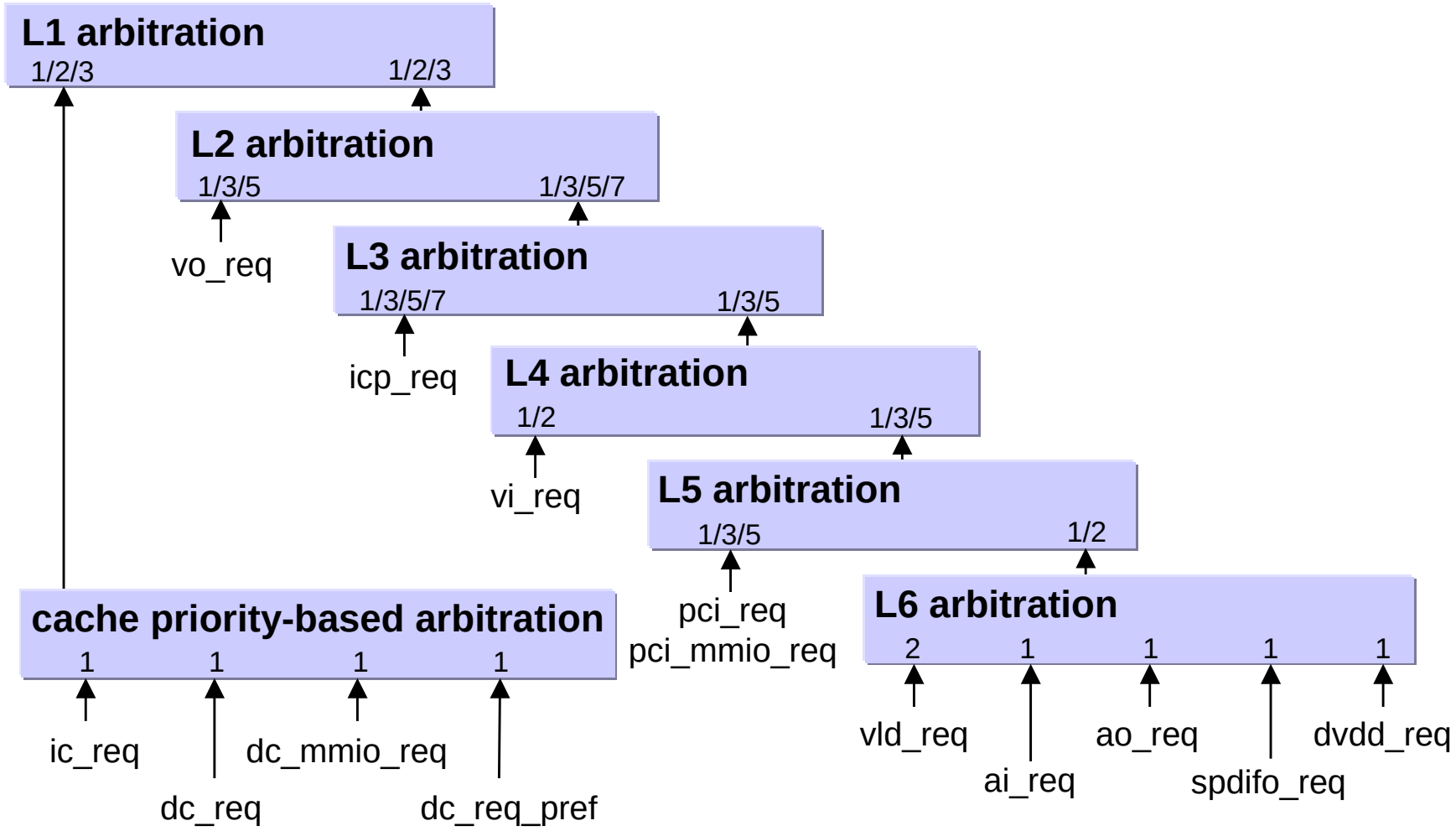
System-on-a-chip



Arbiter Characteristics

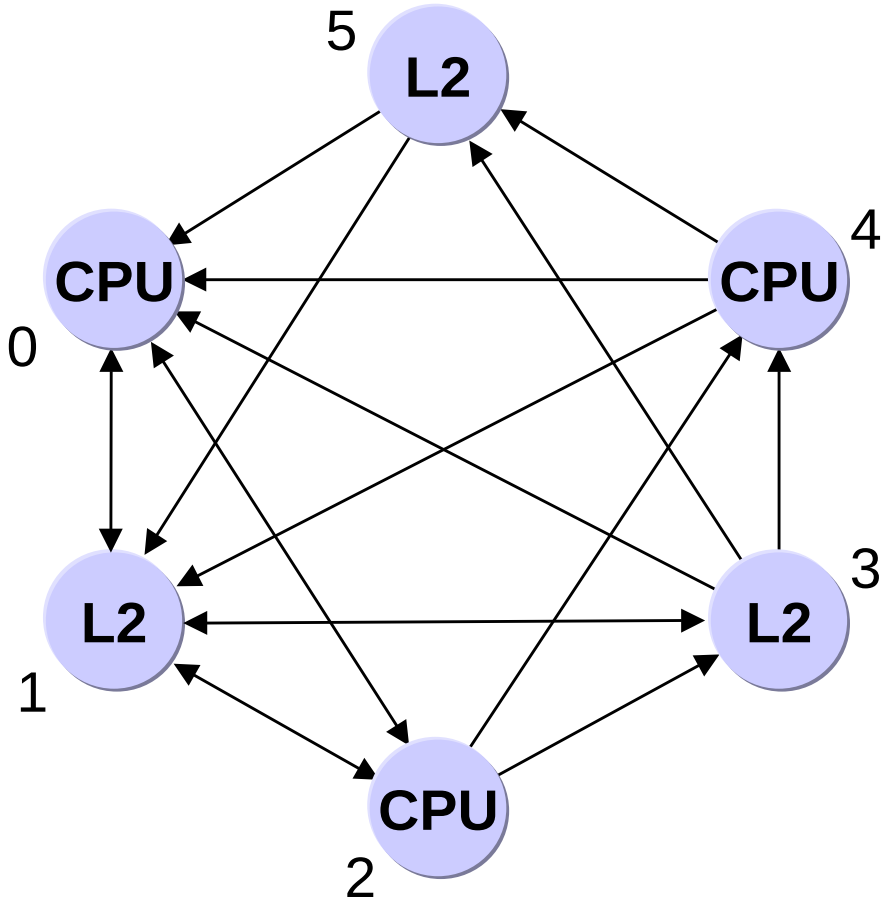
- Round robin
- Programmable
- Hierarchical
- Low- and high-priority requests

Arbiter Block Diagram



Arbiter Implementation

For CPU weight of 3 and L2 weight of 1, states used are 0, 2, 4 and 1



Arbiter: Latency

$$L_i = (D_i * T) + E + REF + LOW$$

T = 20 SDRAM cycles (transaction length)

E = 10 SDRAM cycles (critical word first)

REF = 19 SDRAM cycles (SDRAM refresh)

LOW = the number of cycles the request is at low priority

$$D_{CPU} = \text{ceil}\left(\frac{CPU_{weight} + L2_{weight}}{CPU_{weight}}\right)$$

$$D_{VO} = \text{ceil}\left(\frac{VO_{weight} + L3_{weight}}{VO_{weight}}\right) \times D_2 + 1$$

$$D_2 = \text{ceil}\left(\frac{CPU_{weight} + L2_{weight}}{L2_{weight}}\right)$$

Arbiter: Bandwidth

$$B_i = (Mcycles - K)*64/(E_i*T)$$

T = 20 SDRAM cycles (transaction length)

K = the number of cycles taken by the refresh over the period Mcycles

$$E_{CPU} = \left(\frac{CPU_{weight} + L2_{weight}}{CPU_{weight}}\right)$$

$$E_{VO} = \left(\frac{VO_{weight} + L3_{weight}}{VO_{weight}}\right) \times E_2$$

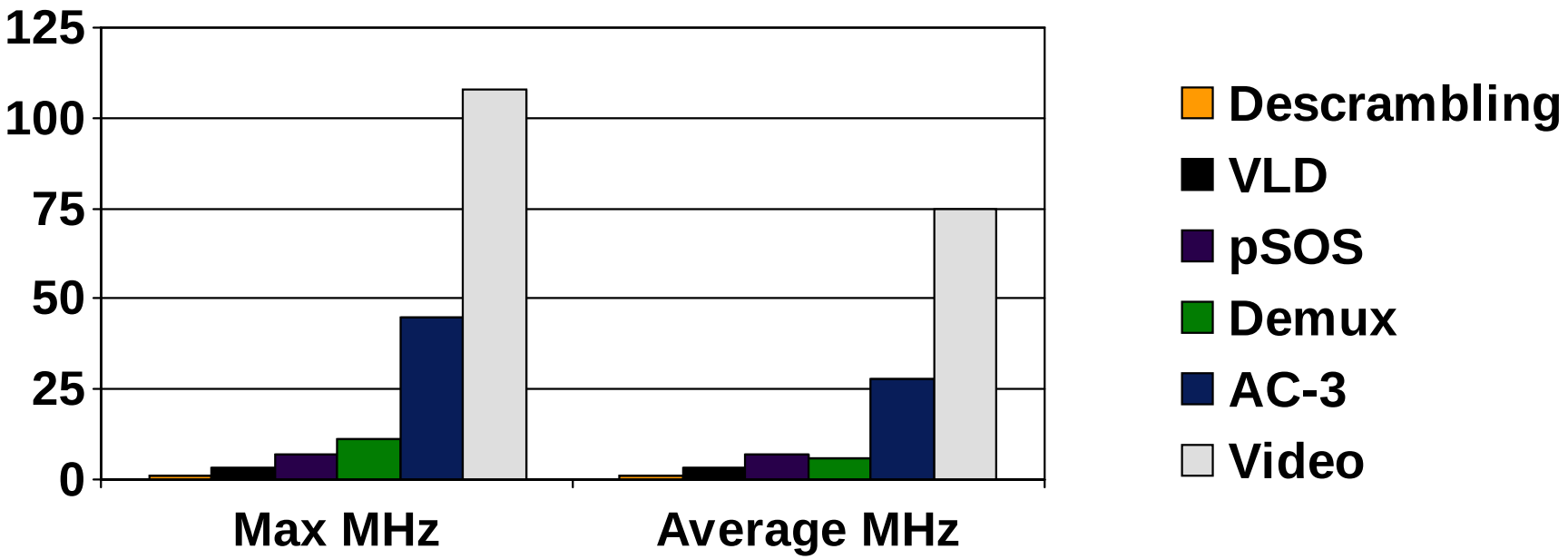
$$E_2 = \left(\frac{CPU_{weight} + L2_{weight}}{L2_{weight}}\right)$$

High-Speed SDRAM Interface

- Up to 64 MBytes
- 64 Mbit generation organized in x32 and x16
- Up to 143 MHz with 4 chips load (32 MBytes)
- Expected to support 166 MHz
- Sustains full bandwidth thanks to pipelined and optimized SDRAM accesses:
  - Interleaved bank access every 32-byte block

MPEG-2 Performance

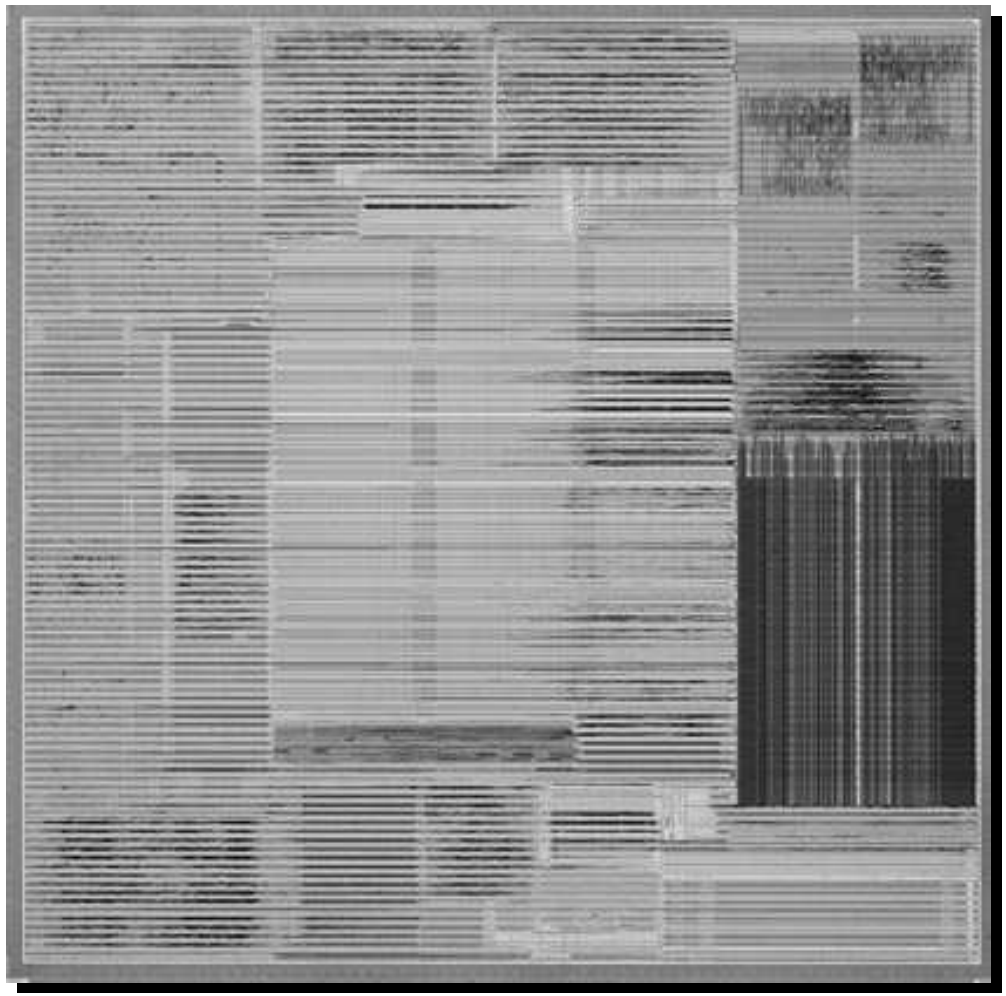
- 180 MHz CPU speed and 143-MHz SDRAMs
- For high-action DVDs, such as ***Twister***, ***The Mask*** or ***Star Ship Troopers***



TM-1300 Silicon

- 58 mm^2
- 6 metal layer
- 5.6 million of transistors
- .25 µm, 2.5 V core supply, 3.3 V I/O supply (5 V tolerant)
- 143 and 166 MHz at min. voltage (2.375 V) and 85 °C
- 180 to 200 MHz under more controlled conditions
- 3.2 W consumption for typical conditions
- Block level powerdown saves up to .5 W
- BGA292 (169 functional I/Os)

TM-1300 Silicon



In Conclusion

- **Powerful VLIW engine (average of 4 instructions/cycle)**
- **Low cost thanks to an integrated system-on-a-chip**
- **Excellent audio/video quality at low cost at system level**
- **For peak performances required by DVD playback: 180-MHz CPU with 143 MHz SDRAM**