POWER4 Test Chip

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Presentation Overview

- Design objectives
- Chip overview
- Technology
- Circuits
- Implementation
- Results

Test Chip Objectives

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Technology feasibility

- Understand product level Silicon technology
- Vehicle for small device level experiments from manufacturing as well as design
- Understand product level packaging technology

Critical circuit learning

- Logic circuitry
- Clocks
- I/O
- Arrays
- Power delivery

Design team skills building

- 40% of product design team contributed to the POWER4 test chip design
- Many facets of the design exercised to product level requirements

Tools learning

- > 80% of point tools exercised
- Execute methodology on a large chip

Powered on 12/17/98

Included in POWER4 Test Chip:

- Experiments from each unit of the POWER4 chip (called DUTs)
- L1, L2, trace and SLB caches
- Product level pumped I/O design implemented
- Product level clock design implemented
- Experiments to stress power delivery
- Engineering and service processor interface
- On chip tester

Chip characteristics:

- 379 mm^2
- 35 million transistors
- 2,217 chip signal I/Os

Built to product level test requirements

Test Chip Logic Diagram

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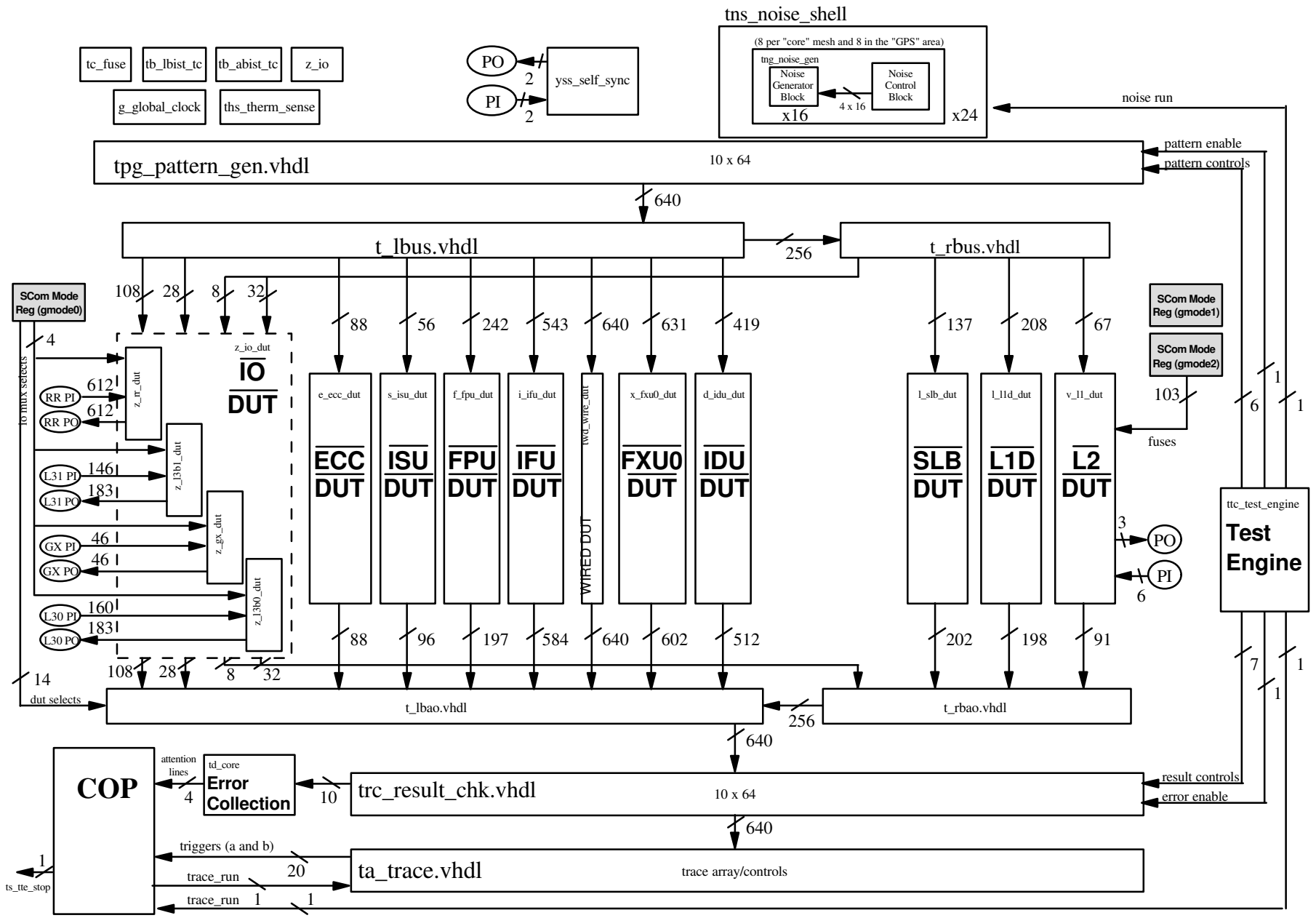

Testchip Die Photo

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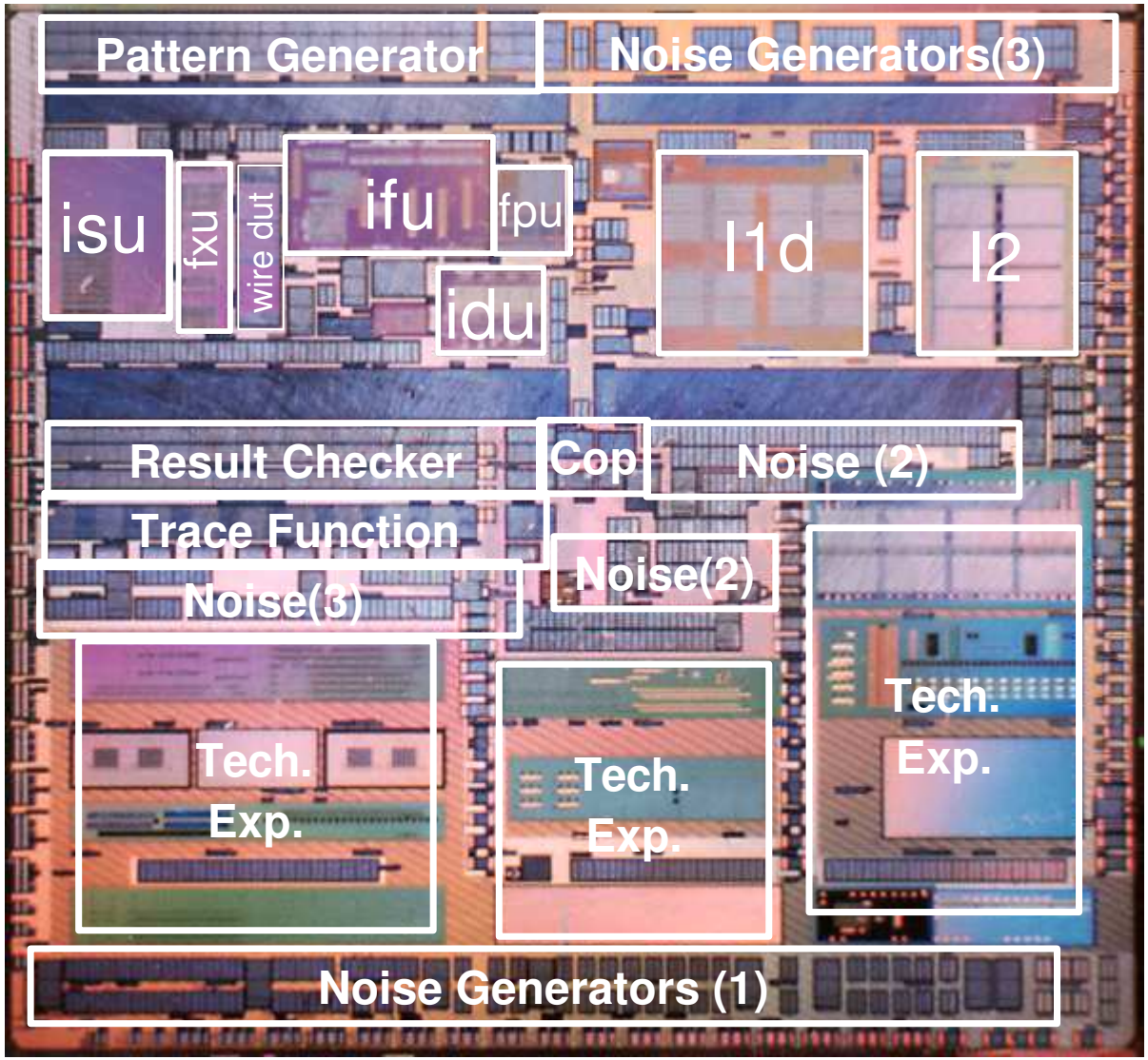

On chip tester

- 640 bit wide, 16 cycle deep vector generation and compare
- Vector ordering, selection, and loop control is programmable
- Cycle accurate result compare
- Random pattern generation mode with MISER

Noise generation

- Cycle by cycle programmable noise generation
- Chip contains 384 noise generation macro's
- Each macro noise amplitude and signature is programmable
- Each cycle noise generator macros can dissipate a total of 0 - 100W

Chip interface, debug infrastructure and test

- Chip accessed and programmed using product level support processor
- Manufacturing level test infrastructure implemented
- On-chip logic analyzer implemented for debug purposes
- Product level clock controls implemented

CMOS 8S Technology

- 0.18 micron general lithography
- Silicon on insulator substrate
- 7 layers of metal, all Cu
- SRAM cell size: 4.23 sq microns
- Vdd = 1.5V

Package Technology

- Glass substrate
- No thin film required
- > 5500 4mil C4 chip to substrate connections
- C4 connections on an 8mil pitch

Clocks

- High frequency PLL design compared to low jitter reference source
- On chip clock distribution latency and skew measured

I/O

- Elastic and non-elastic I/O implemented and measured
- Performance of both I/O types "chip" limited

Arrays

- L1, L2 and SLB implemented and measured
- The performance and density critical L2 cache design is solid

Power/Noise experiments

- Noise amplitude measured under several different current excitations
- Package impedance empirically determined for full GHz bandwidth

Clock source experiment

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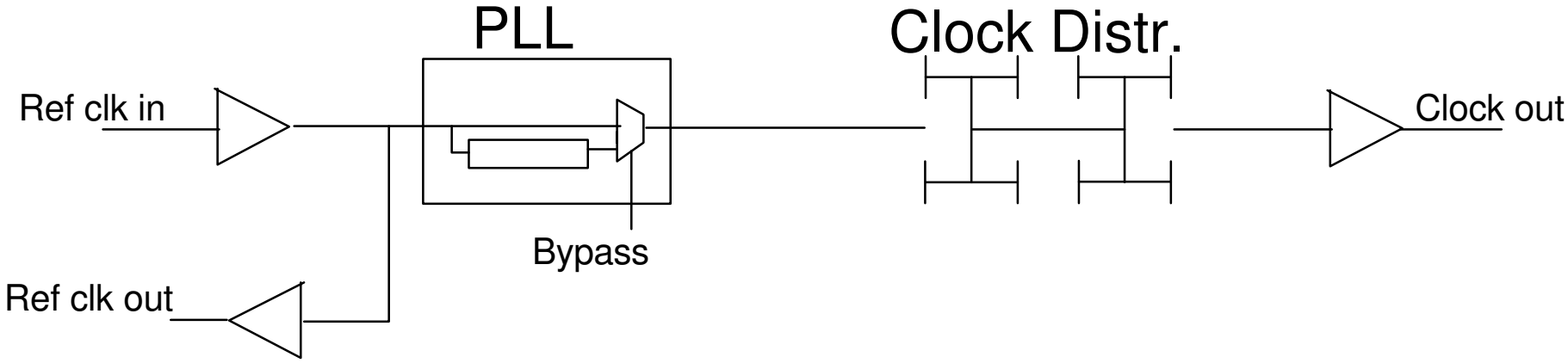
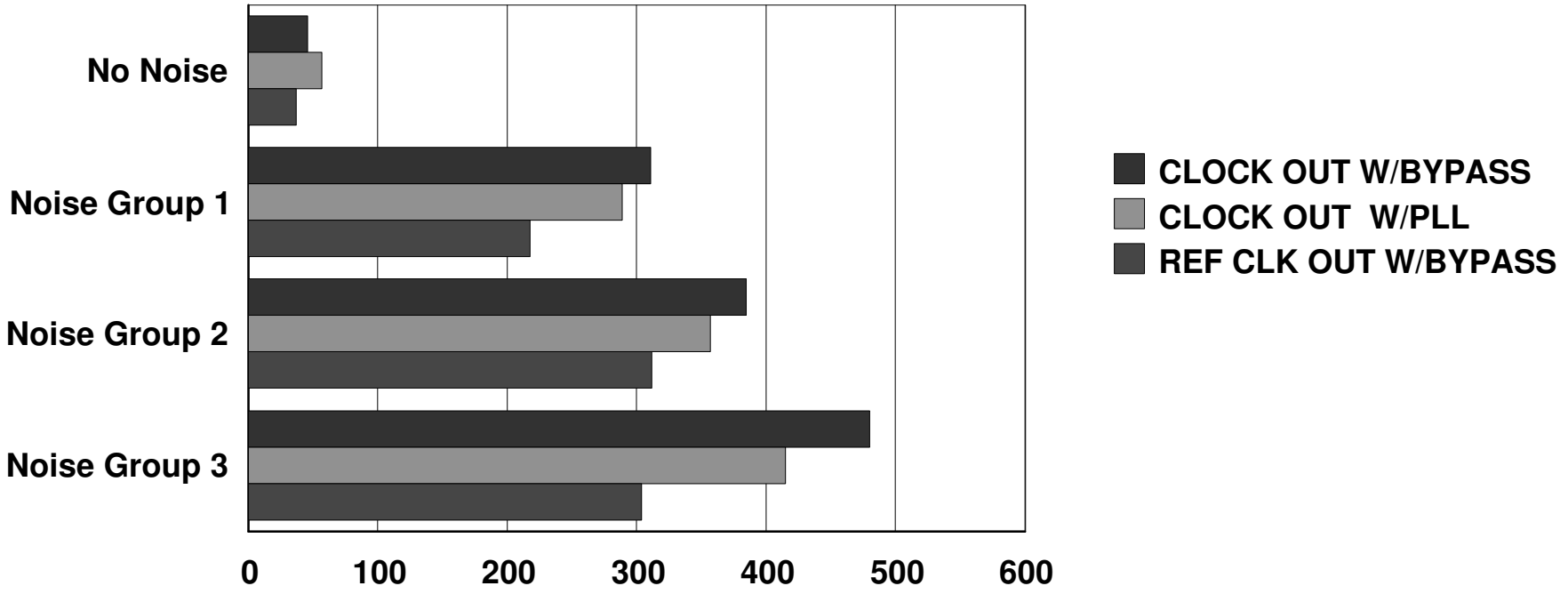
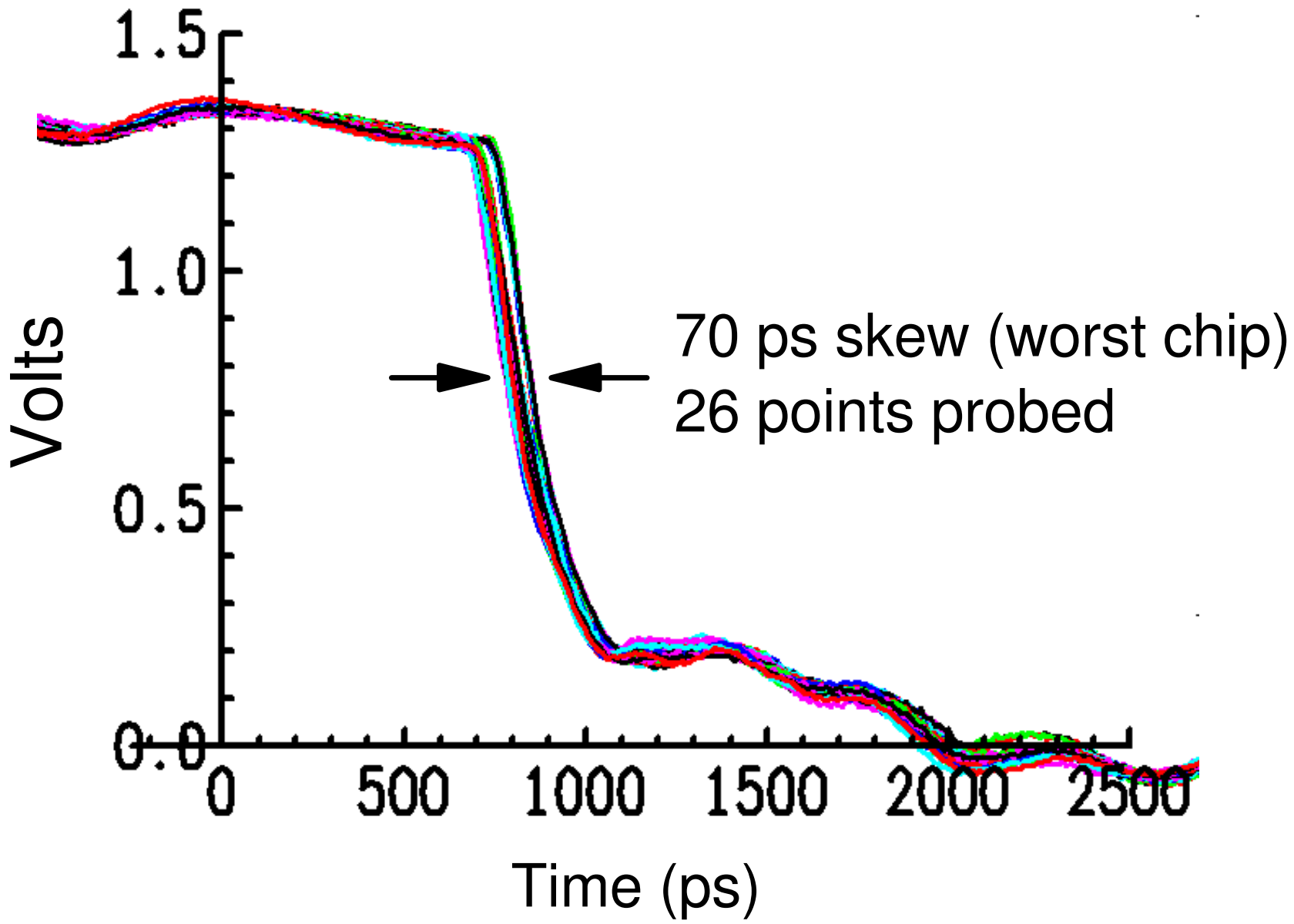


800 MHz Clock Jitter



Measured Clock Skew



Test Chip contains product like I/O architecture

- Approximately 800 elastic I/O signals
- Approximately 1400 synchronous I/O

Elastic I/O performance

Voltage	A5 Pattern	OF Pattern
1.3	462	453
1.4	459	450
1.5	462	465
1.6	462	468
1.7	465	453

Synchronous I/O performance

Voltage	No Noise	FFFFFFFF	FFFF0000	F0000000
1.3	978	906	810	816
1.5	1098	1002	912	954
1.7	1128	1026	978	1032

L2 cache macro:

- 2 cycle access latency
- Row and column redundancy
- Array efficiency > 75%
- Includes ABIST

Wafer/Chip	MAX ABIST FREQ (MHz)	VDD (V)	CHUCK TEMP (deg C)
FY/4,7	1430	1.4	25
FY/7,7	1360	1.4	25
FY/7,4	1420	1.4	25
PY/5,4	1500	1.5	40

Measured Noise Results - Time Domain

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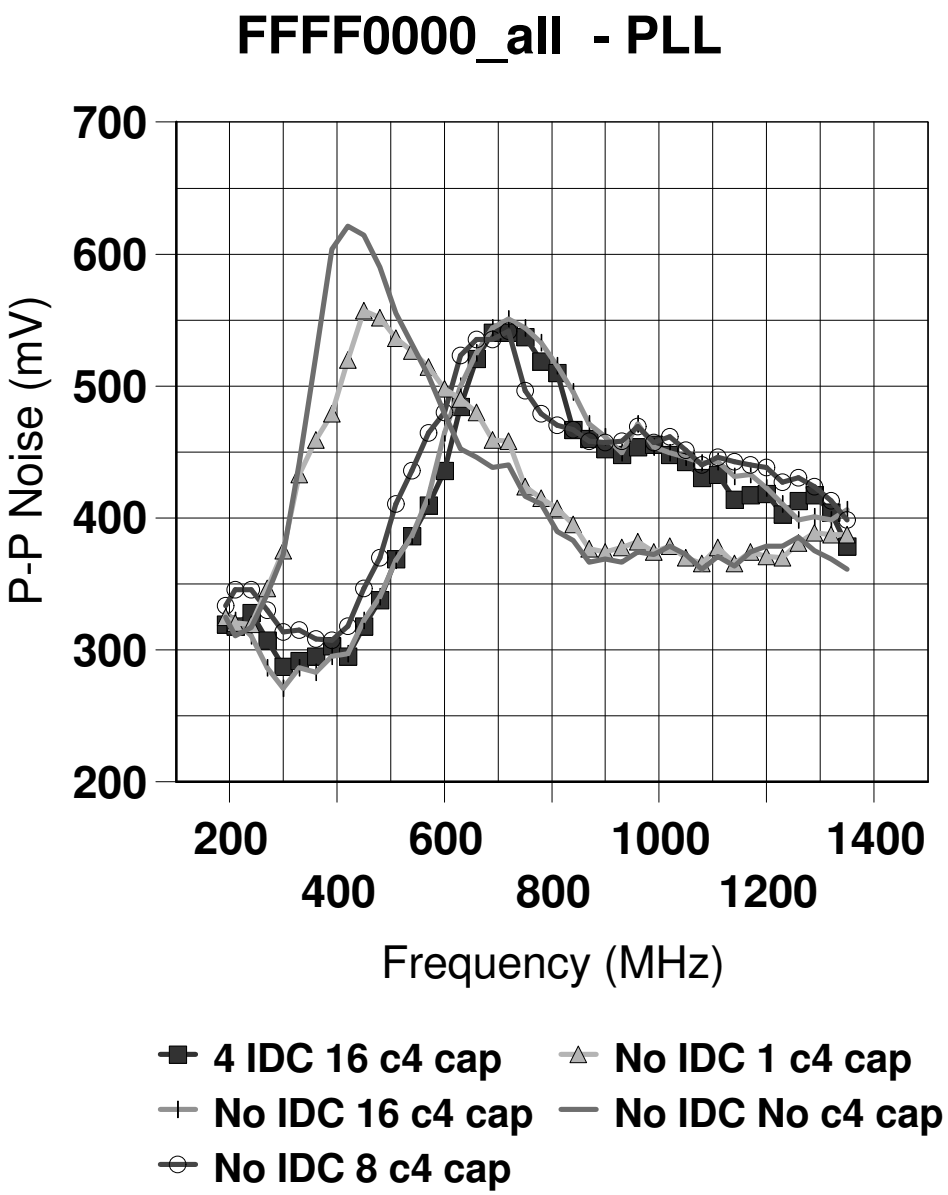

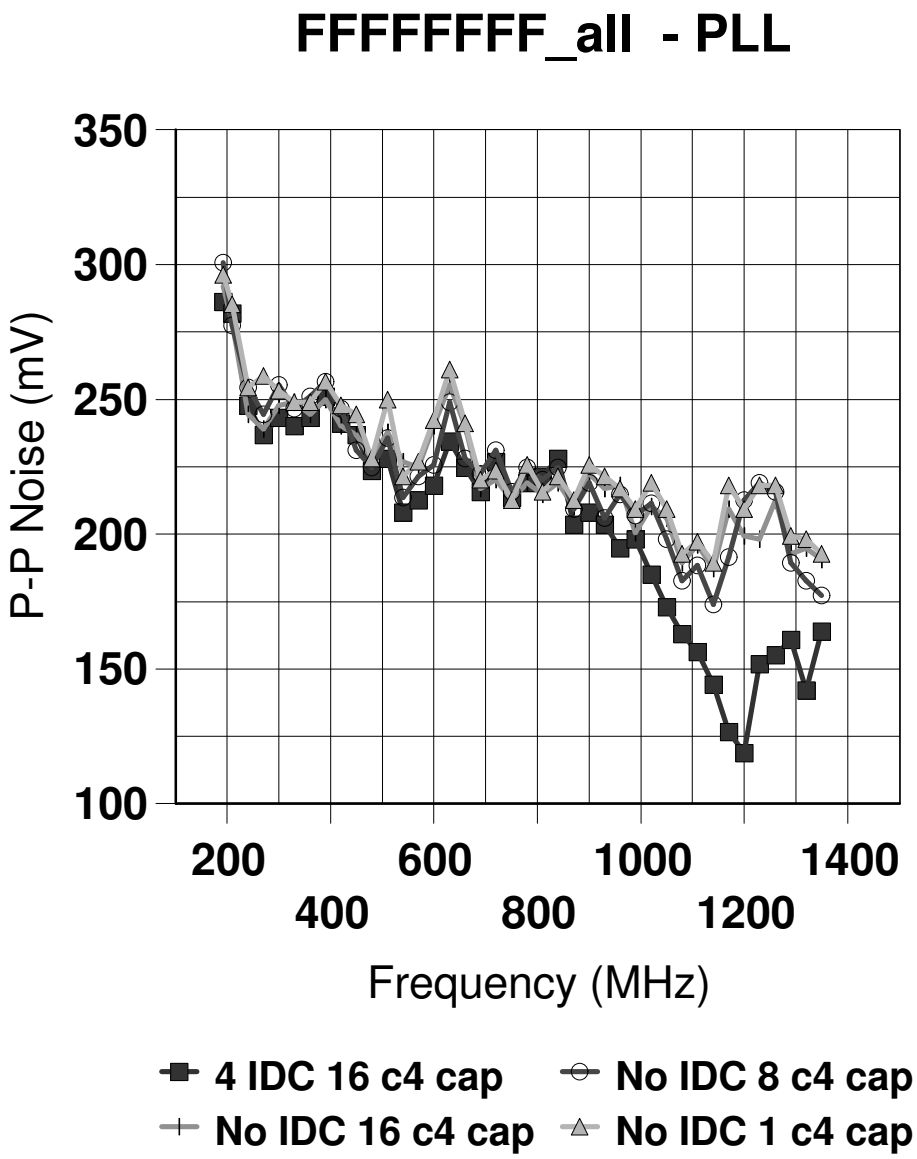

Measured Noise Results - Freq. Domain

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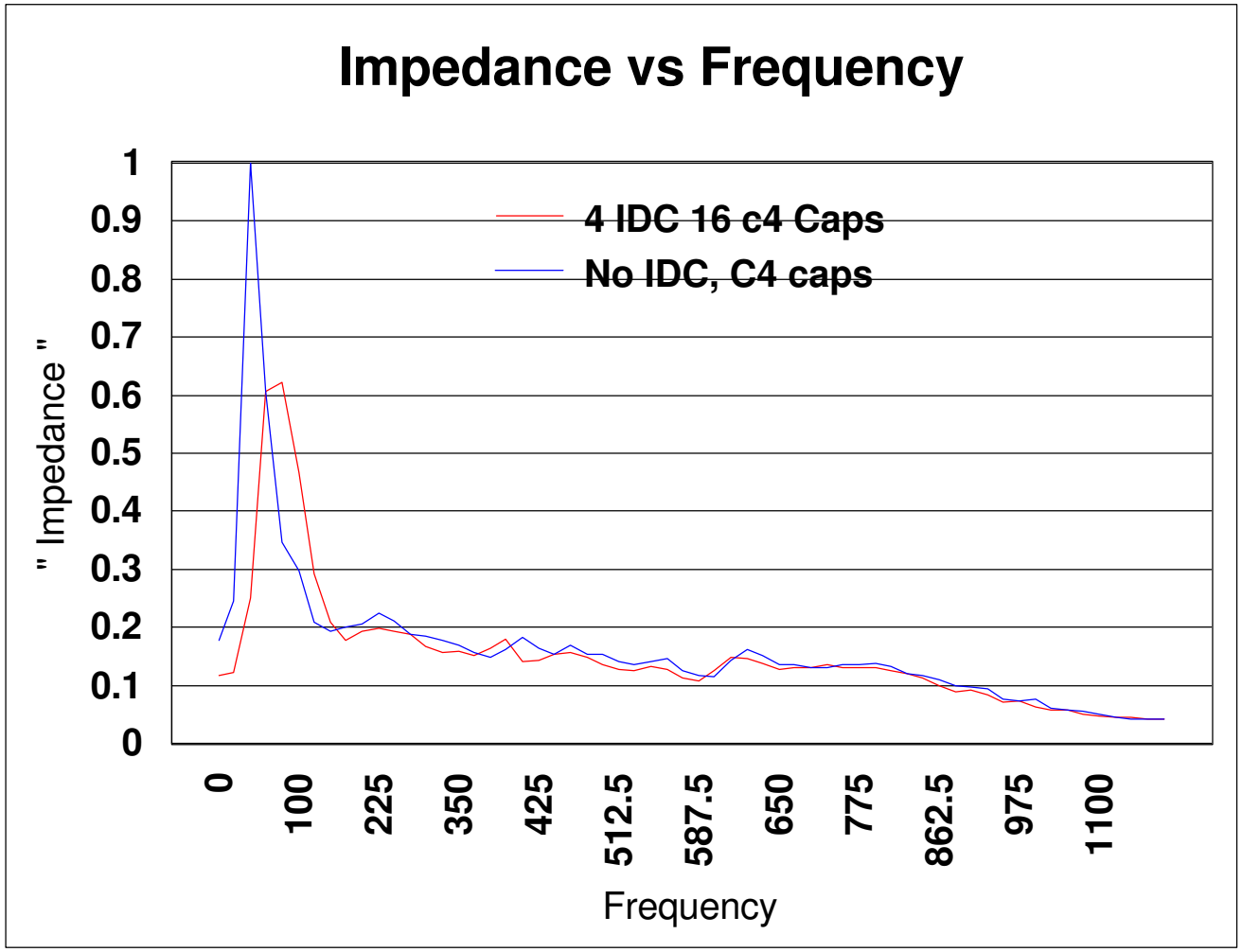
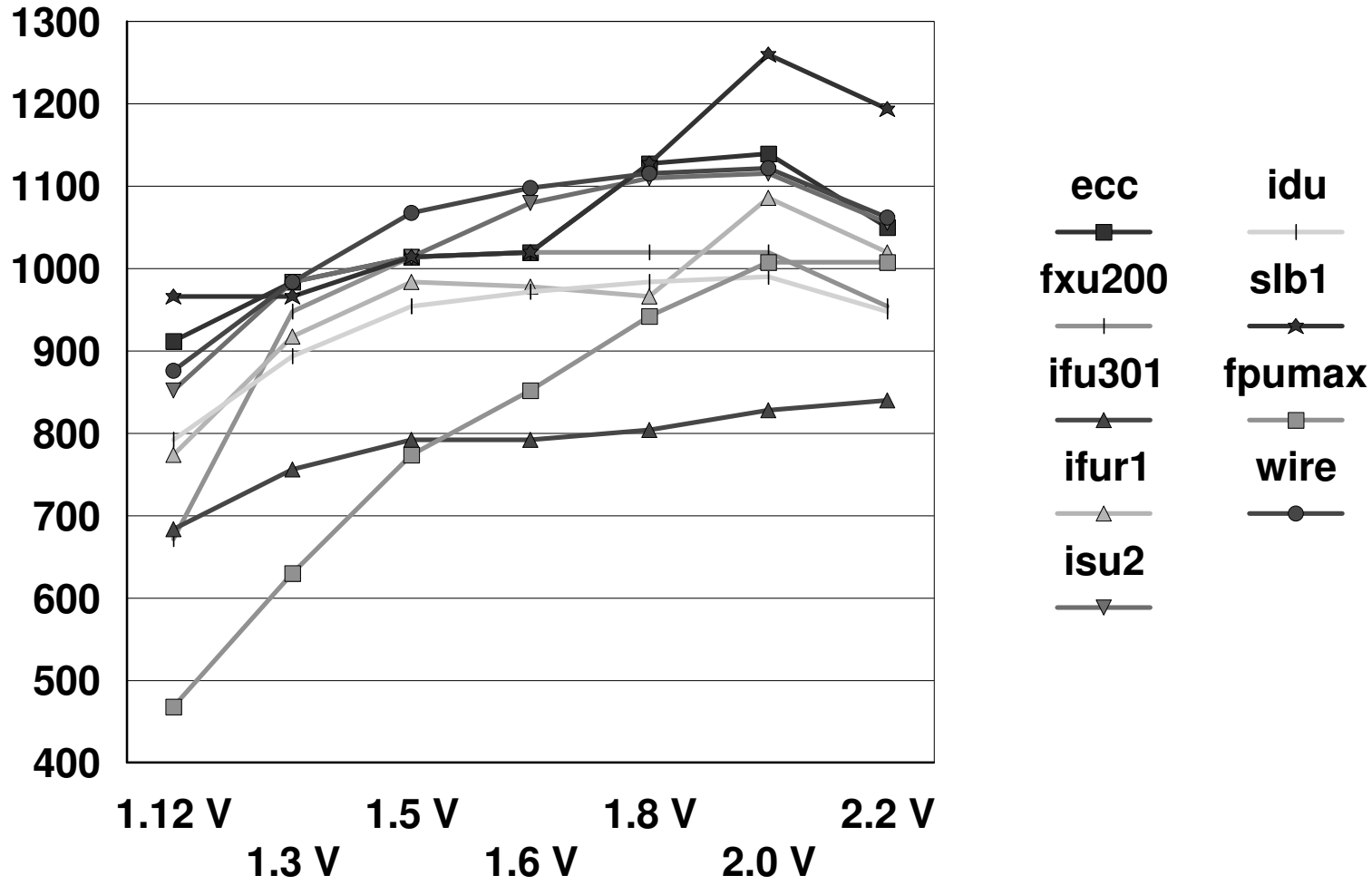
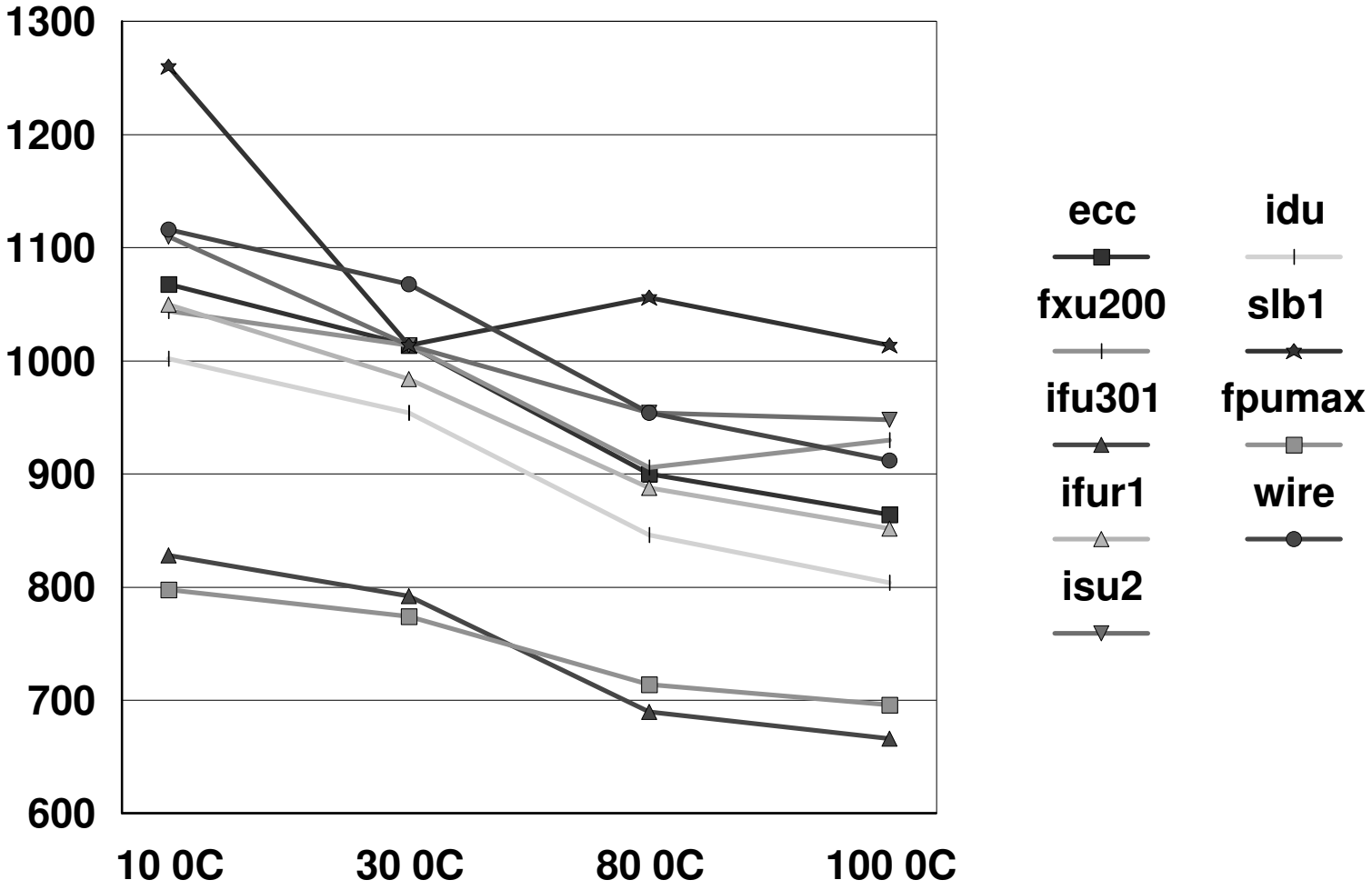


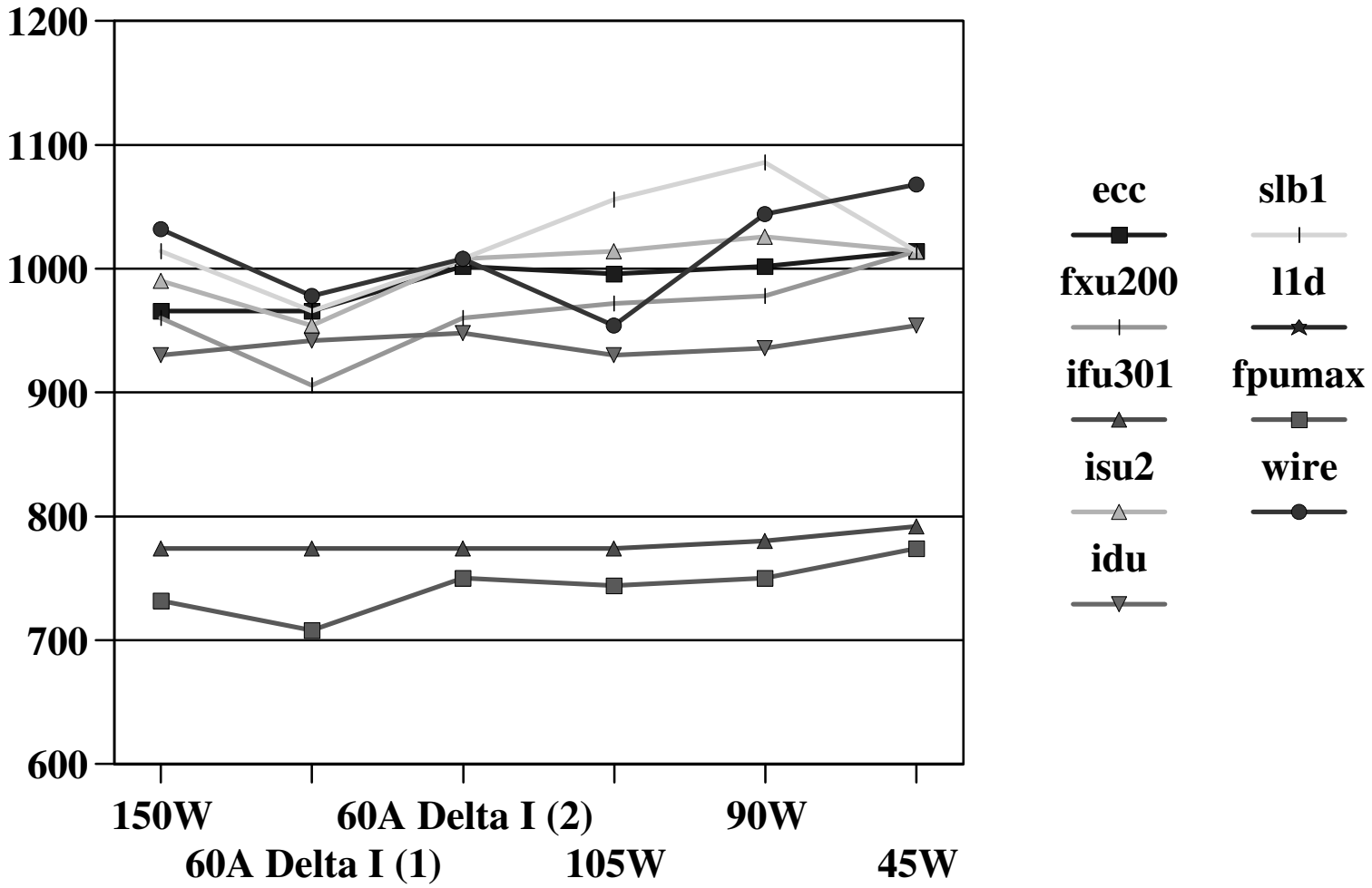
Voltage Schmoo



Temperature Schmoo



Noise Schmoo



Summary

We have demonstrated that the POWER4 Clock, I/O, array and power delivery designs support GHz operation

Significant portions of the POWER4 product design have been implemented and tested

The POWER4 service processor interface, manufacturing test and debug design has been implemented and tested

The POWER4 design team has built a product like chip utilizing the product design tools and methodology