



VelaTX™

Innovative 3D Architecture Coupled with Embedded DRAM Architecture

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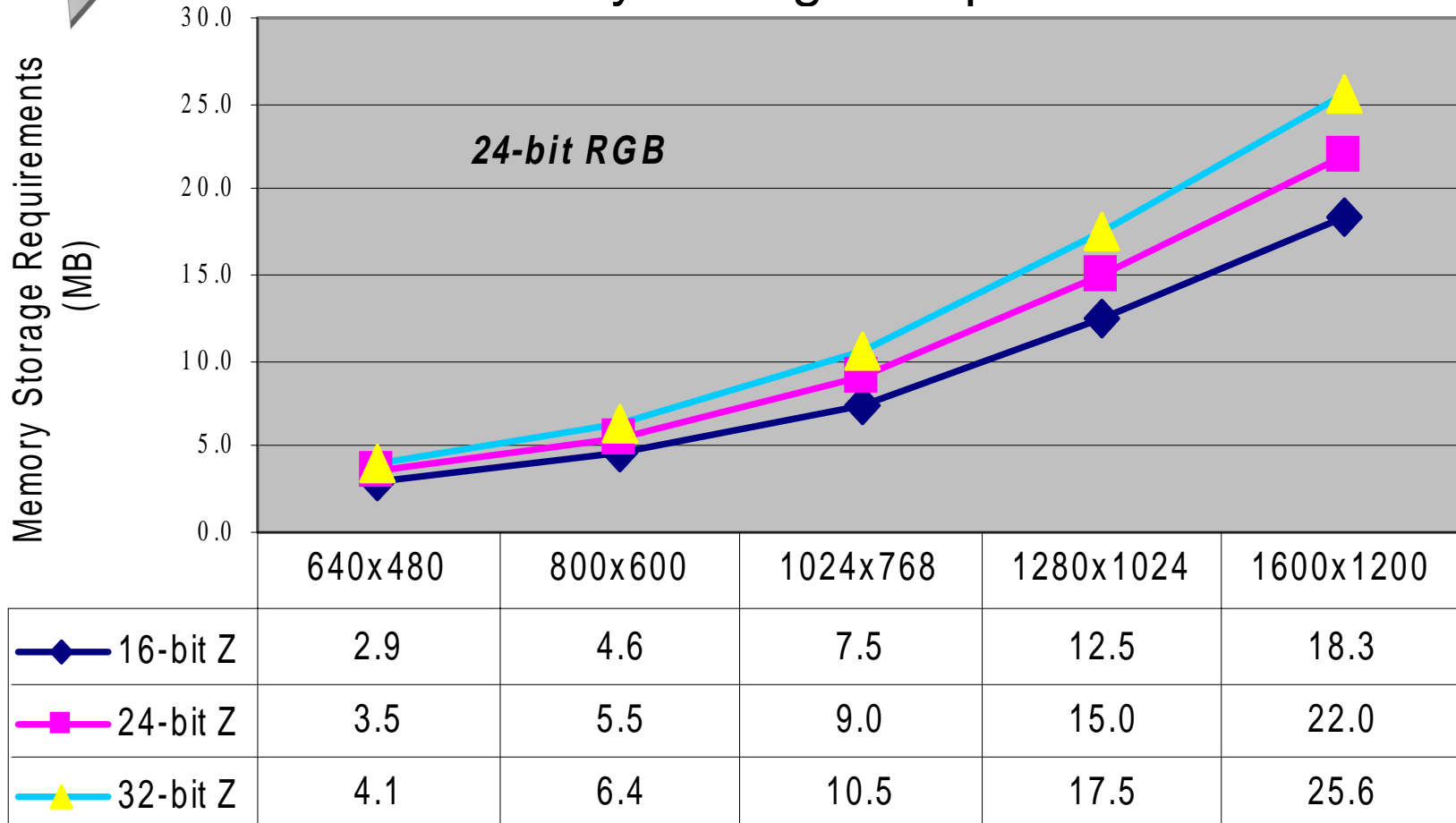


Problem Statement

- Traditional 3D graphic game engines architectures with external ram solutions can not meet the increased demand for higher visual realism.



Traditional 3D Graphics Engine (T3D) Memory Storage Requirements

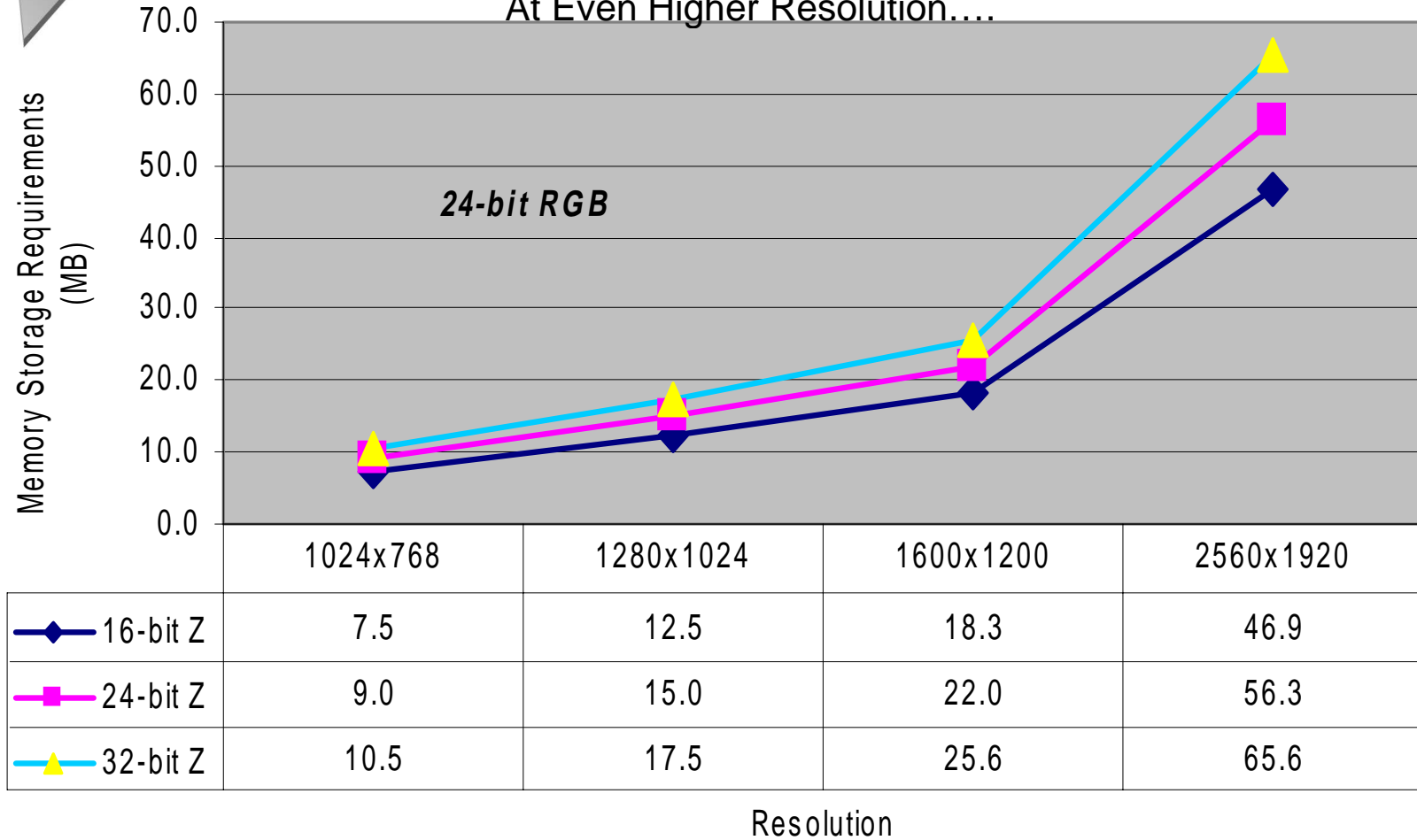


Note: No texture maps, polygon lists



T3D Memory Storage Requirements

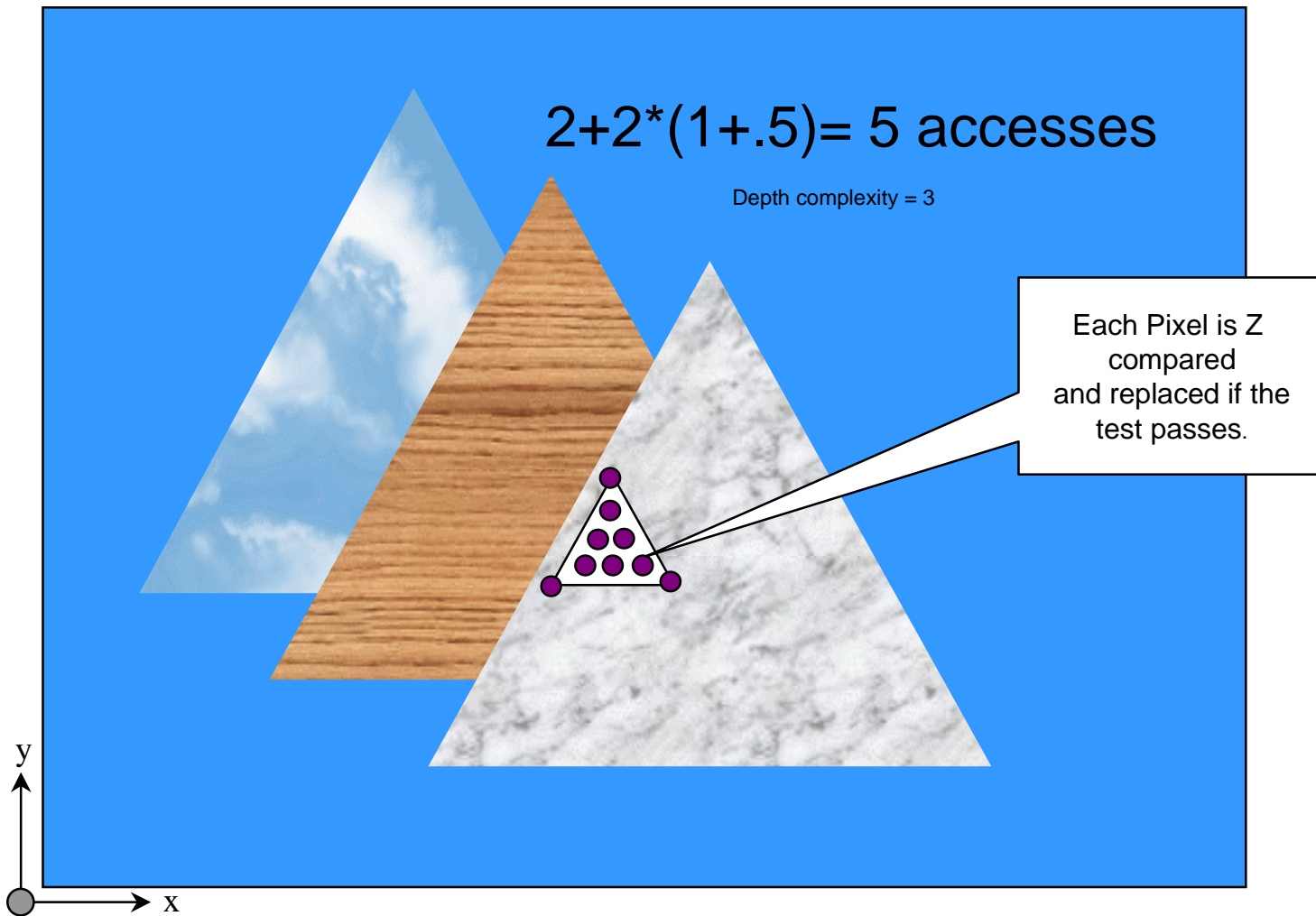
At Even Higher Resolution....



Note: No texture maps, polygon lists



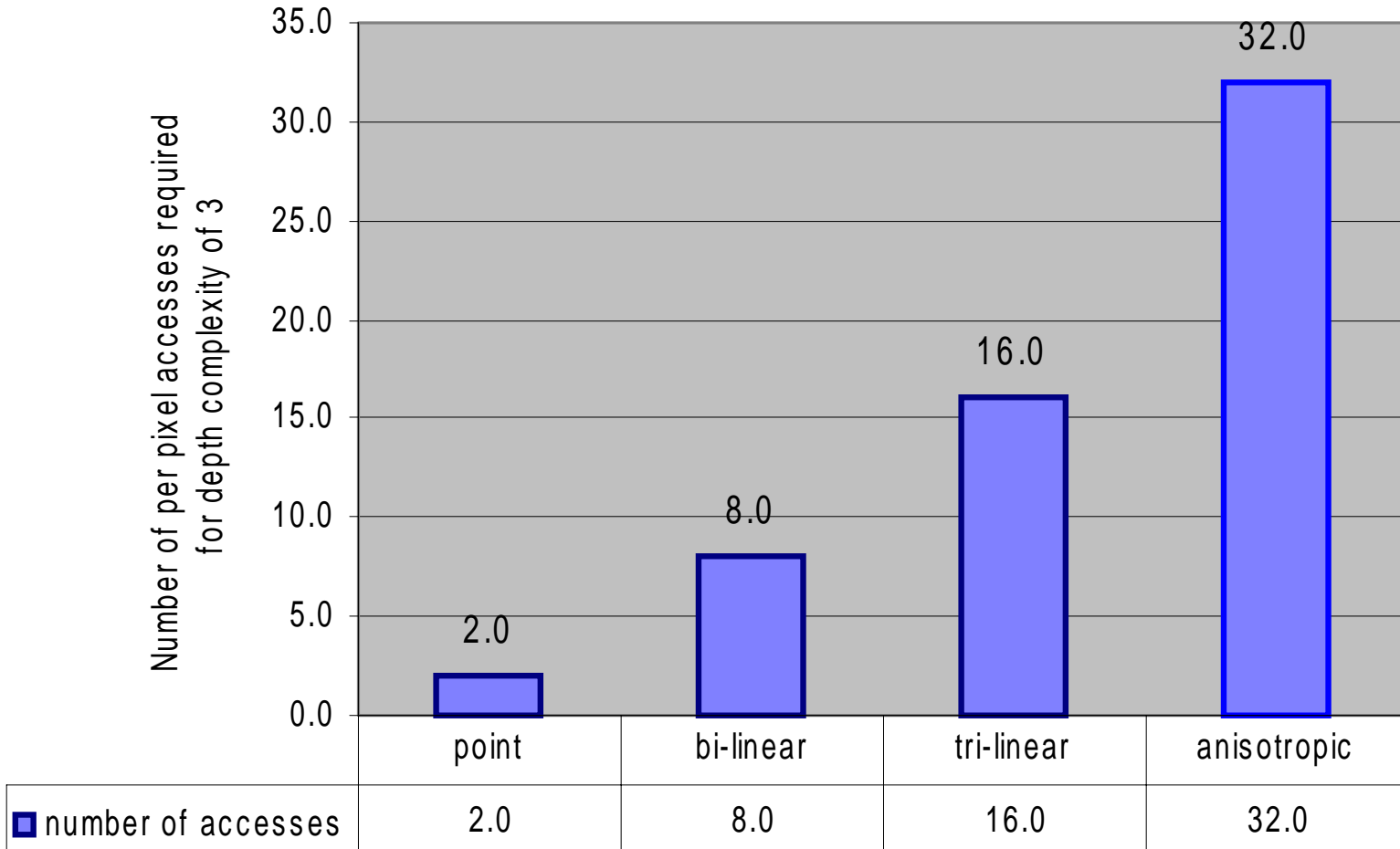
Traditional Frame Buffer access method





Number of per pixel access of Various Filters

$$(1+2(.5))^{\text{filter reads}} = \text{total}$$



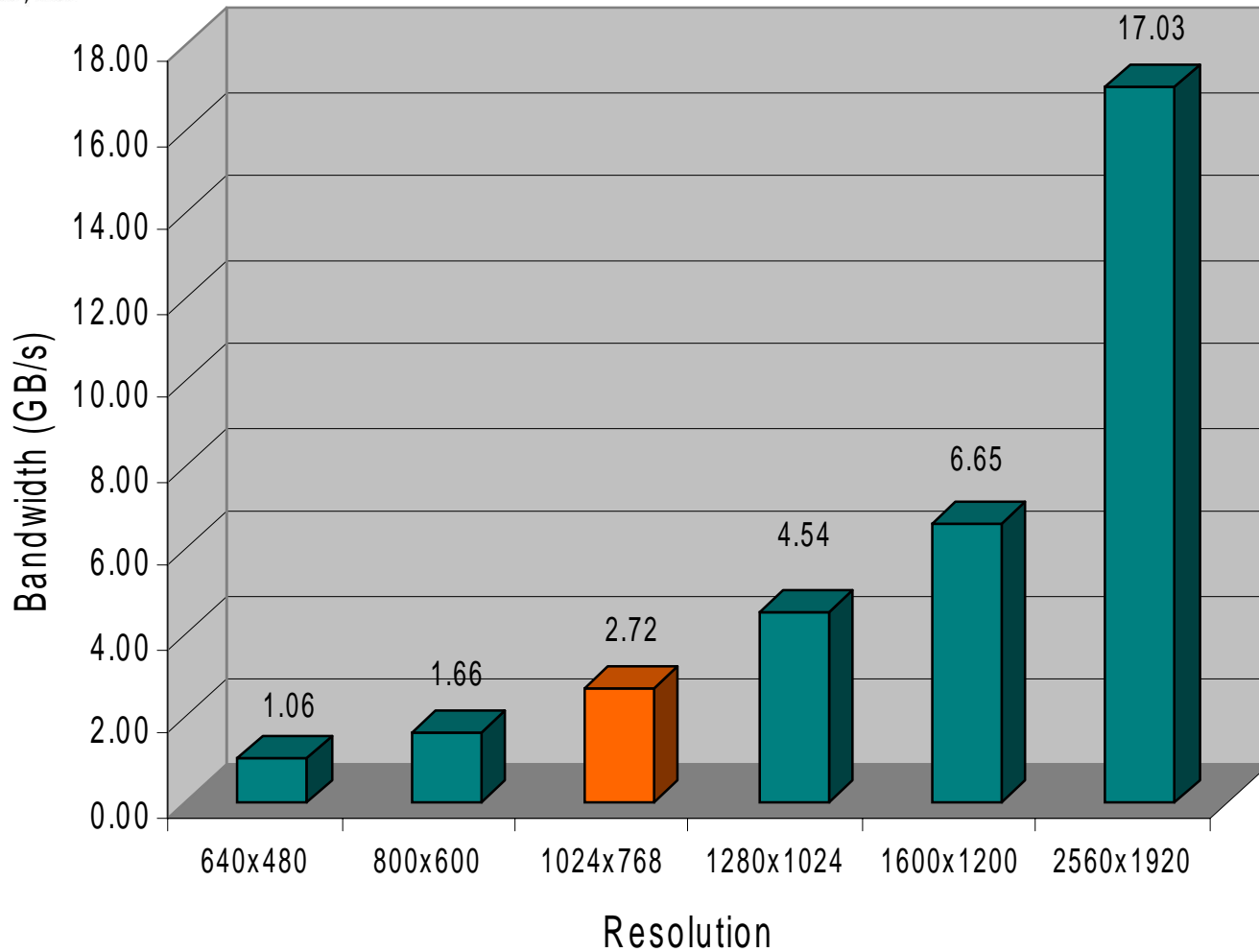
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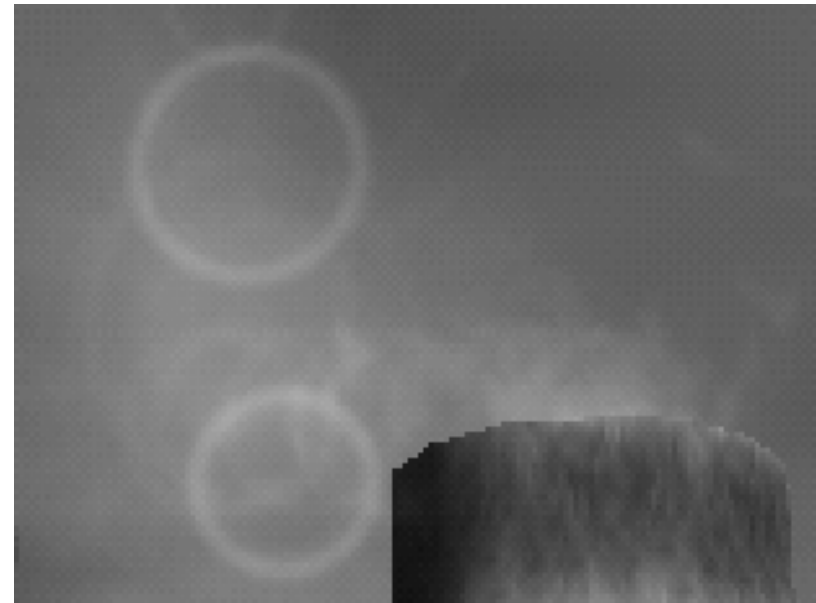
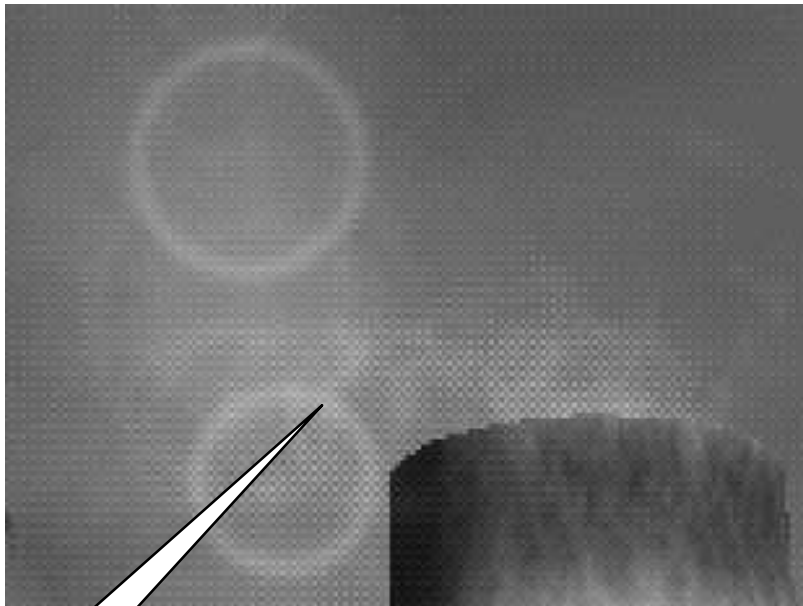
Summary of Bandwidth Requirements for T3D



Note: Trilinear Mipmapped, 24 bpp texel, 24-bits Z, 60 fps, Depth Complexity=3



T3D Transparency dither artifacts



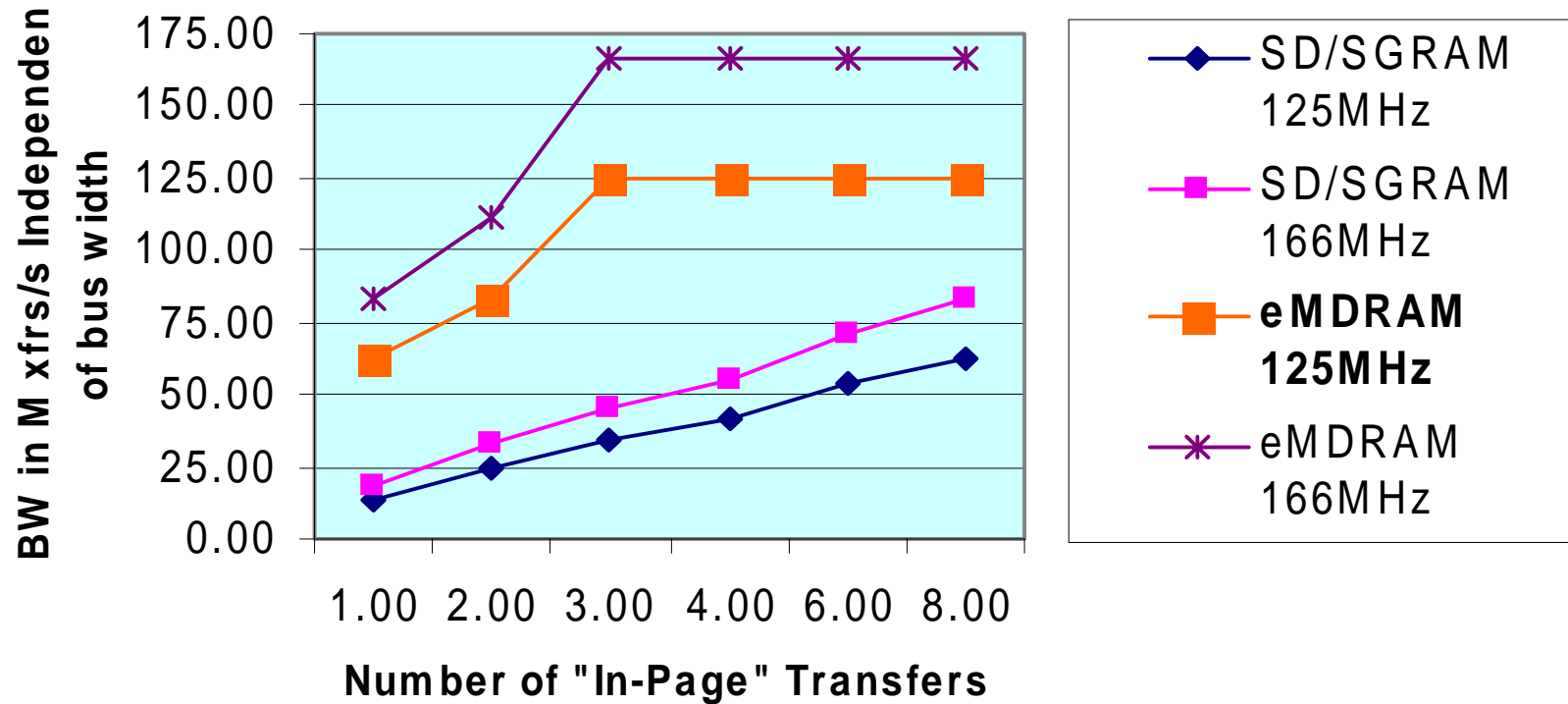
Note dither
pattern
effect

T3D Image

VelaTX Image

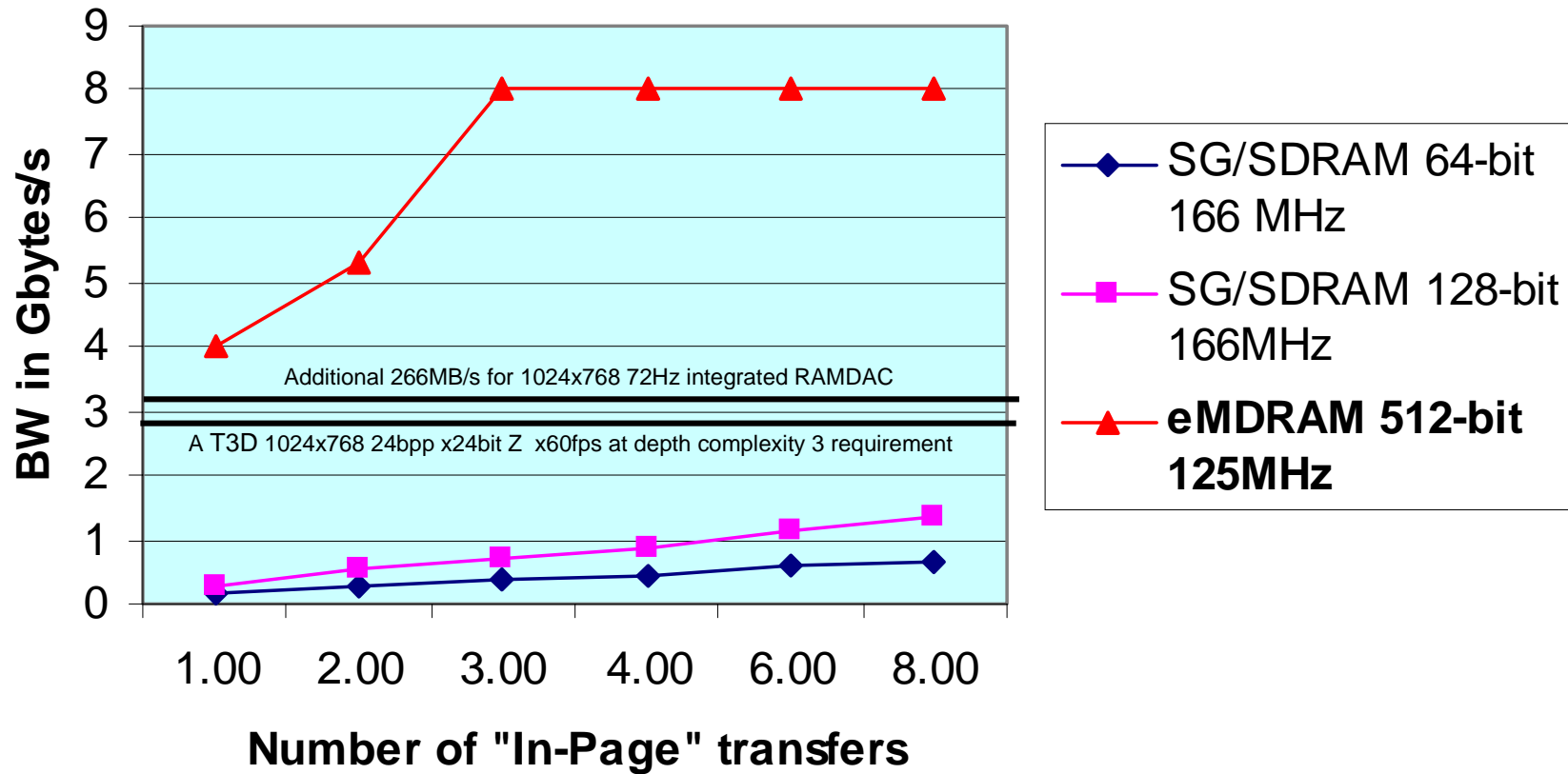


Comparative memory transfer rates



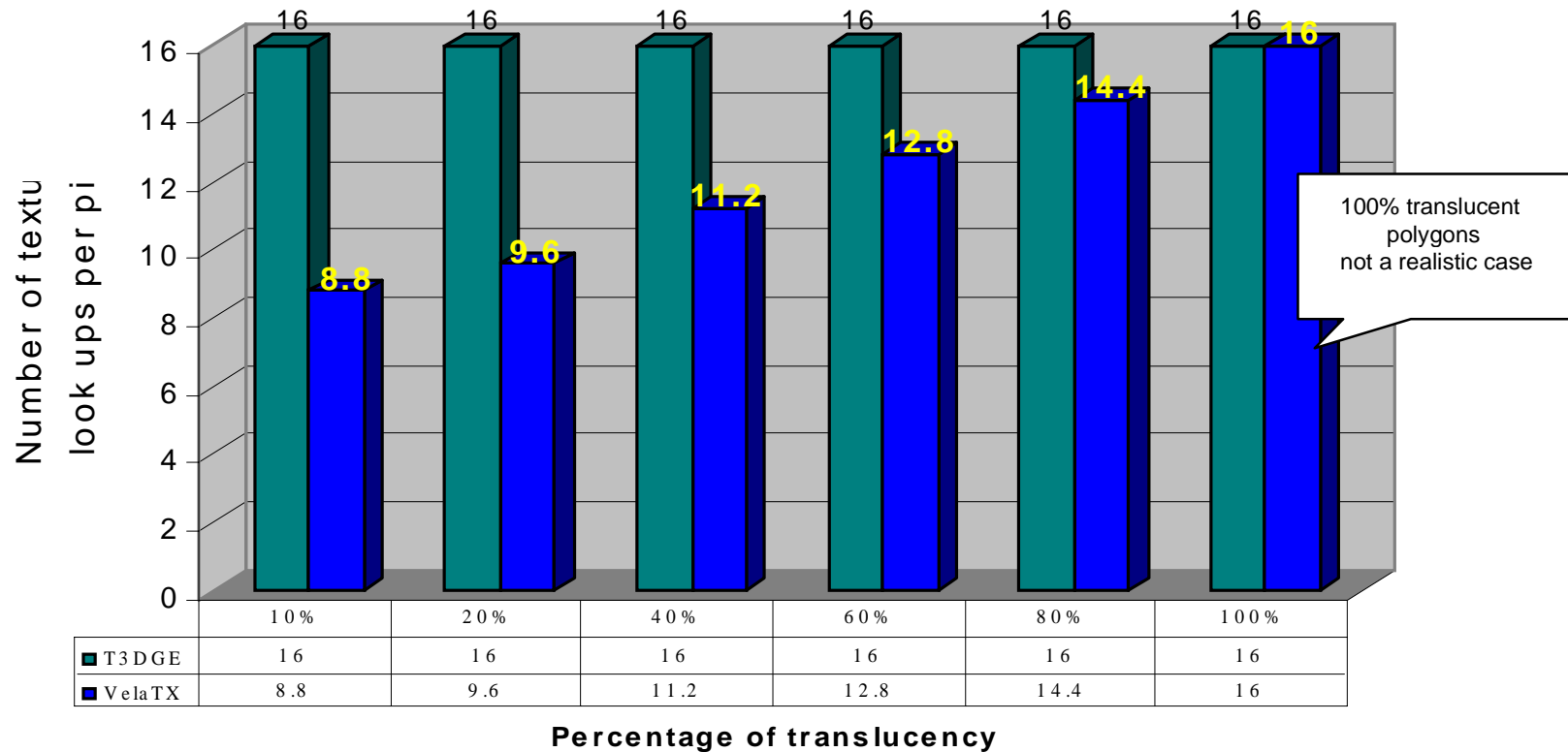


Sustained Bandwidth Comparison for some implementations





Texture look-ups at depth complexity of 3 for various levels of Transparency

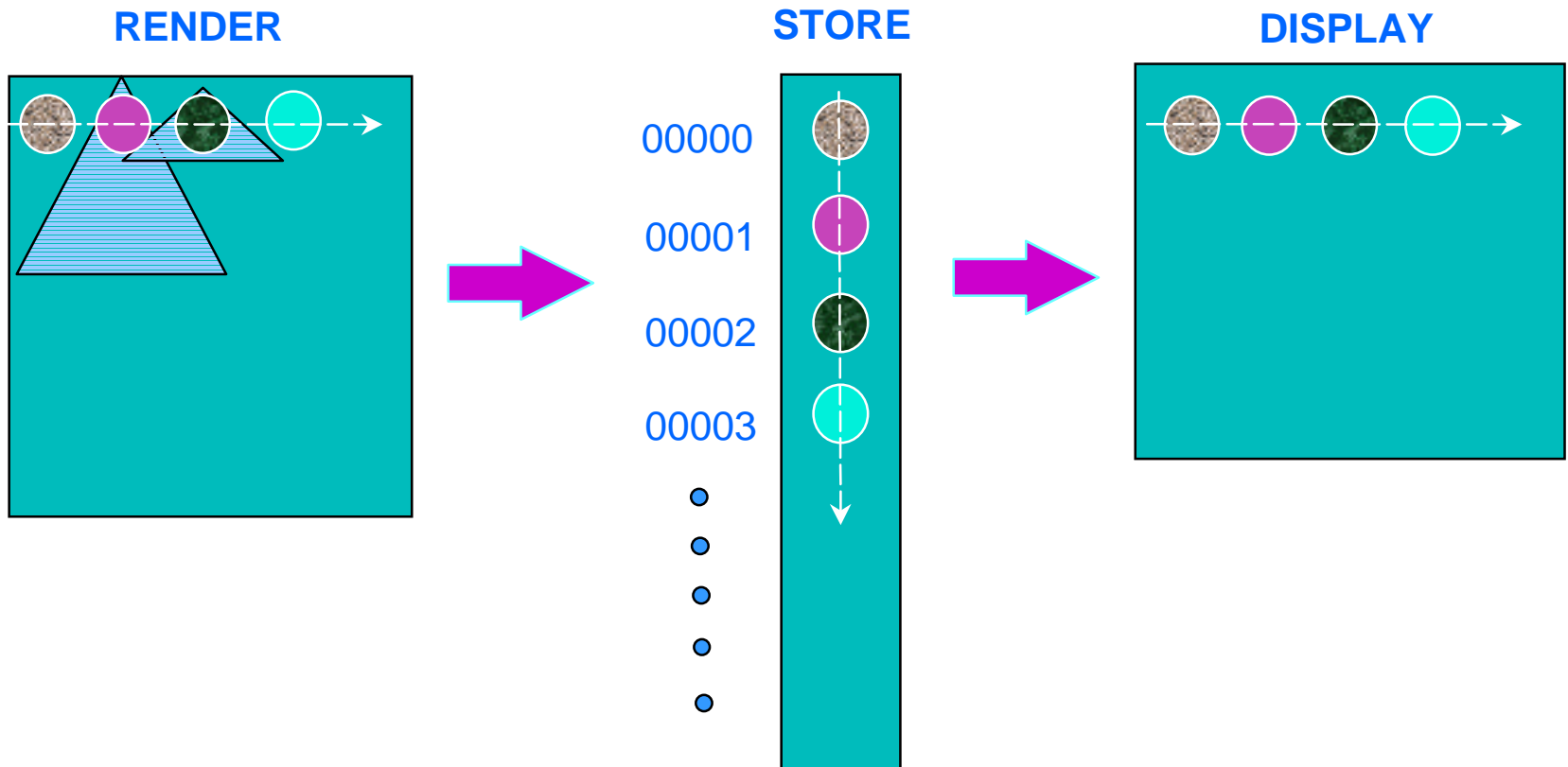


Note: Assumes no game ordering of transparent polygons.



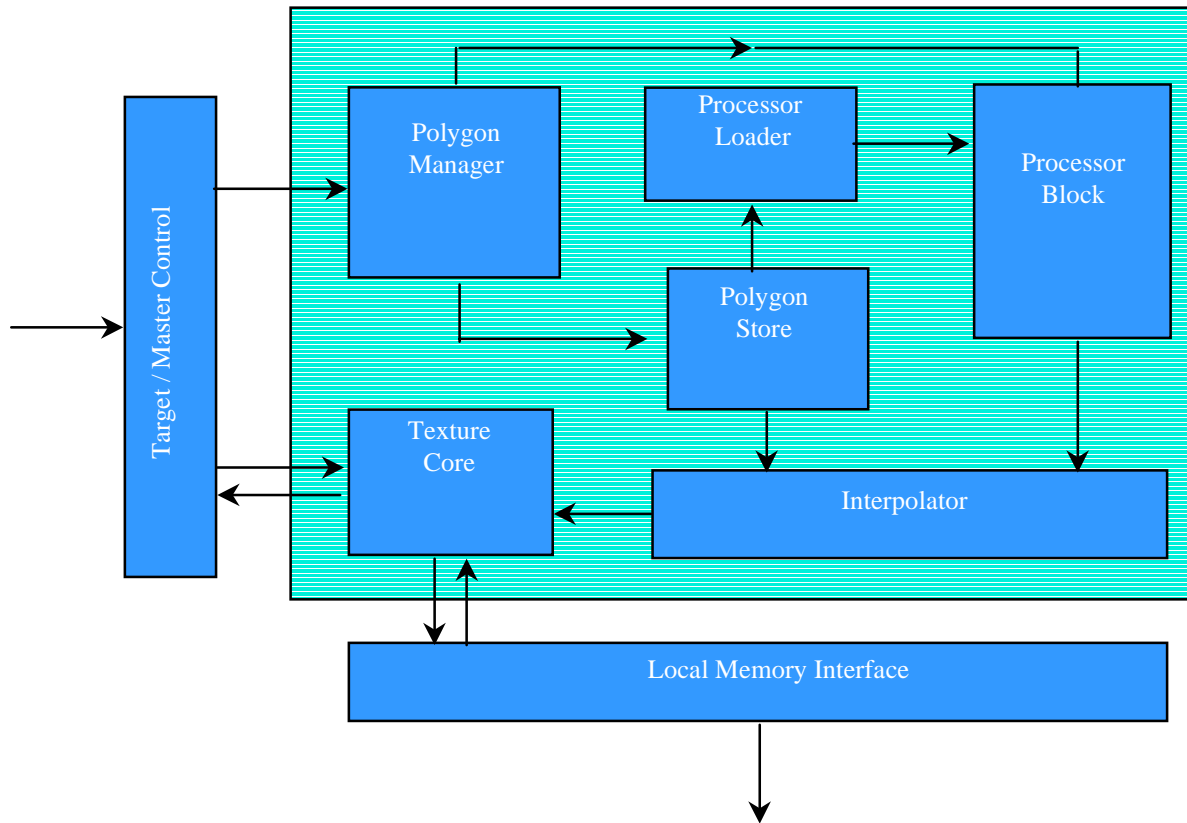
PixelSquirt™

Screen Order/Linear Frame Buffer Rendering



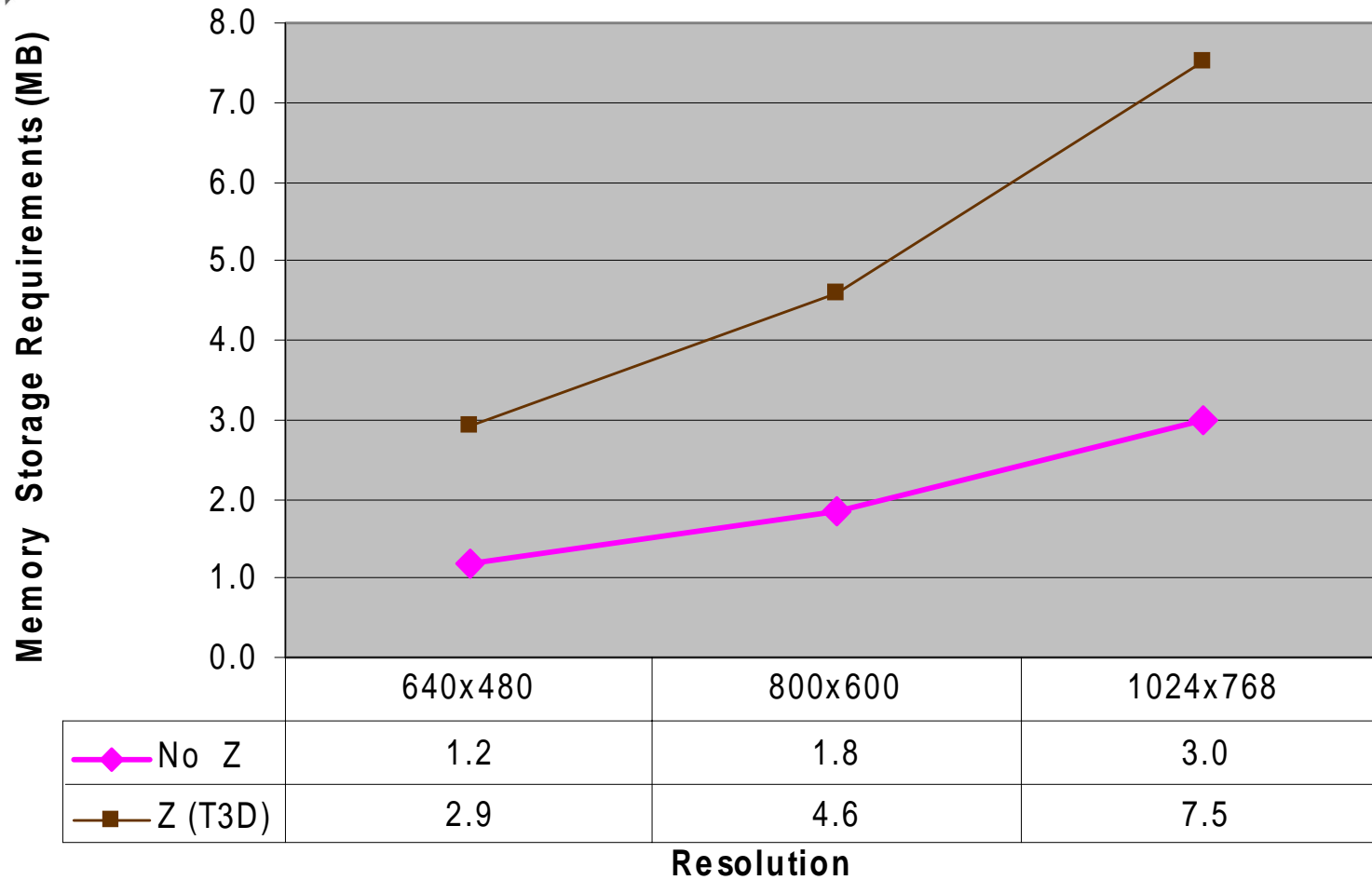


Pixel Squirt 3D core





Z Elimination savings over T3D Z storage

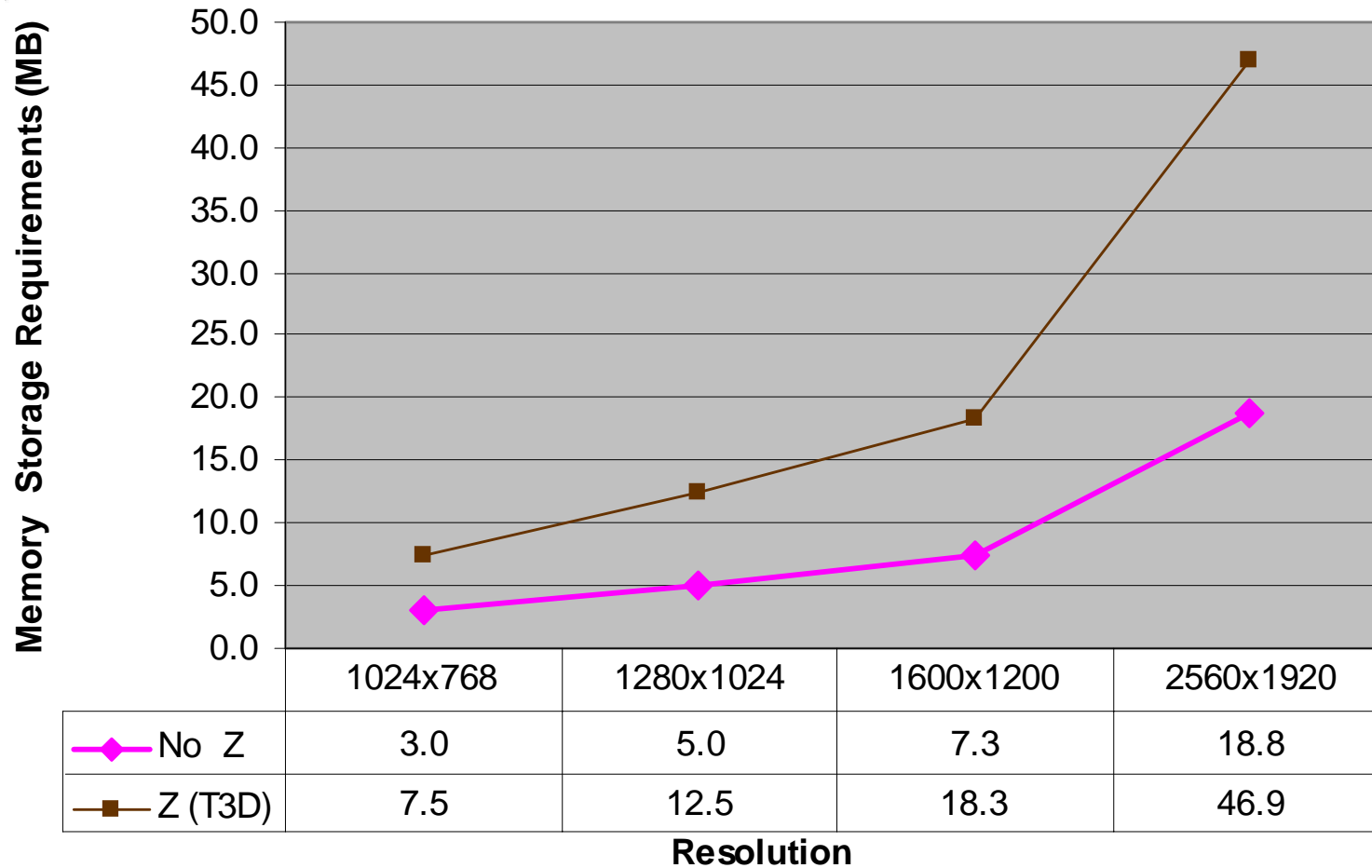


Note: 16 bits per pixel, 24 bit Z, double buffered

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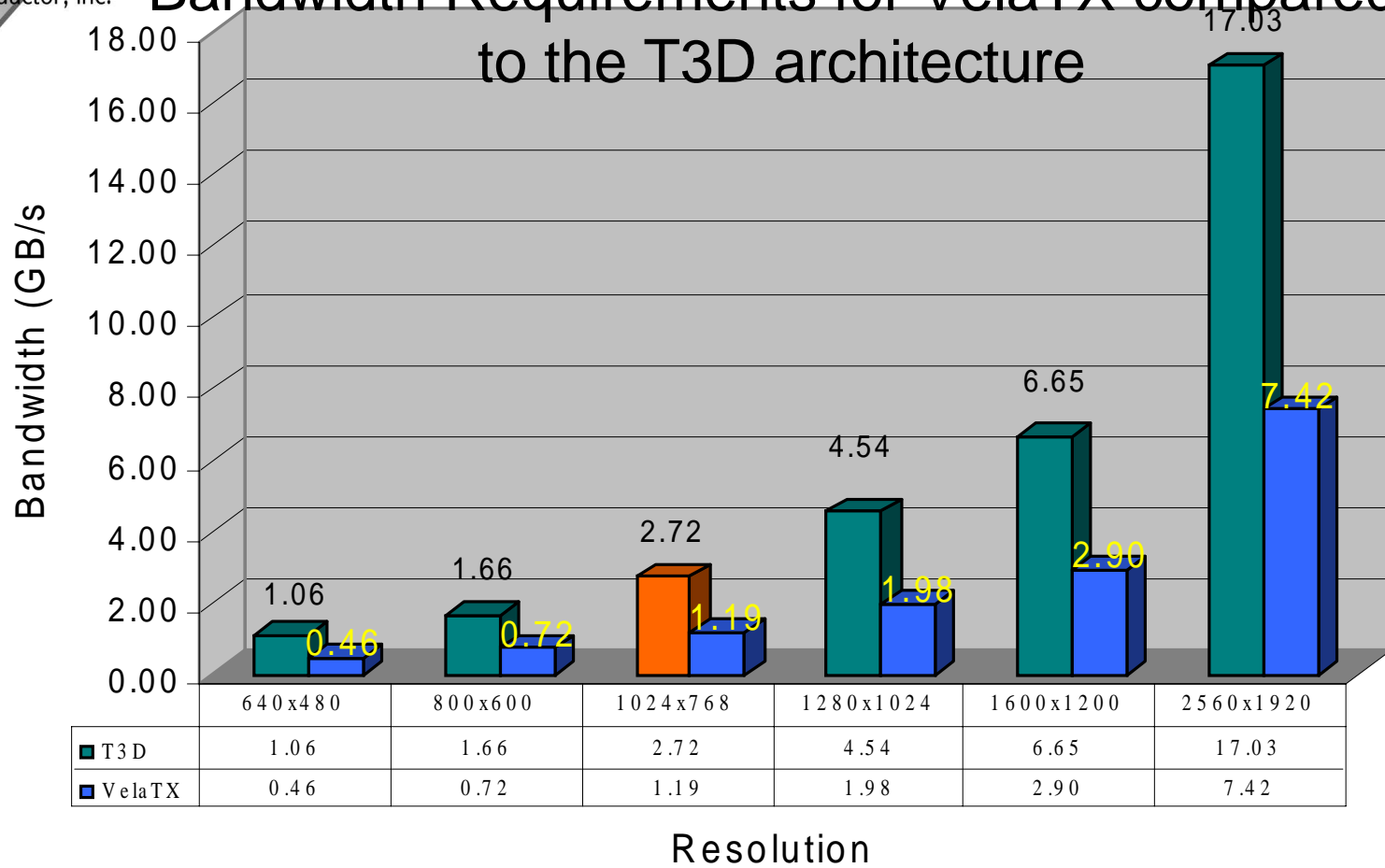
Z Elimination savings over T3D Z storage (at even higher resolutions)



Note: 16 bits per pixel, 24 bit Z, double buffered



Bandwidth Requirements for VelaTX compared to the T3D architecture

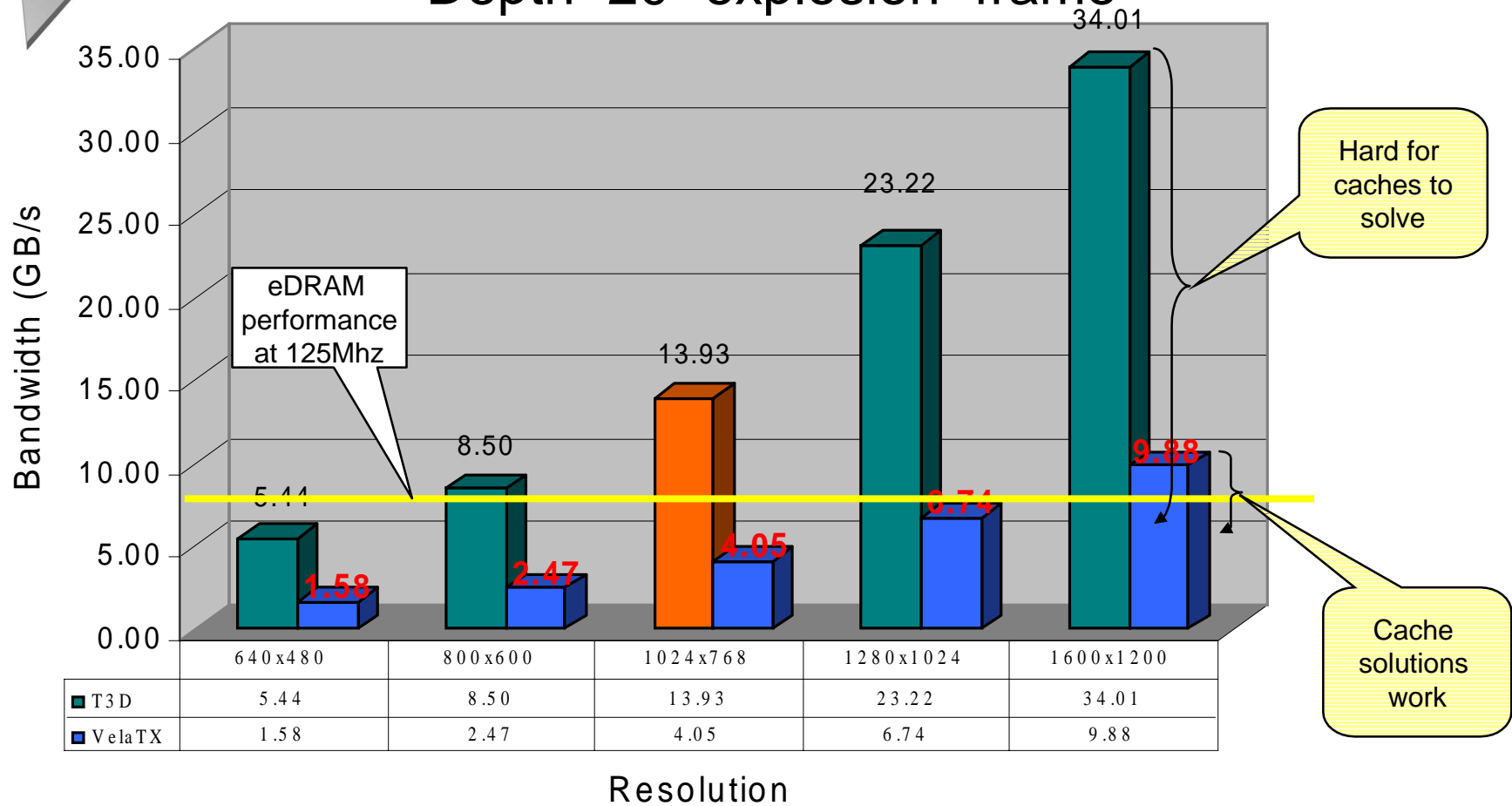


Note: Trilinear Mipmapped, 24 bpp texel, 24-bits Z, 60 fps, Depth Complexity=3, 50% translucency

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Bandwidth Requirements to handle the Depth=20 "explosion" frame

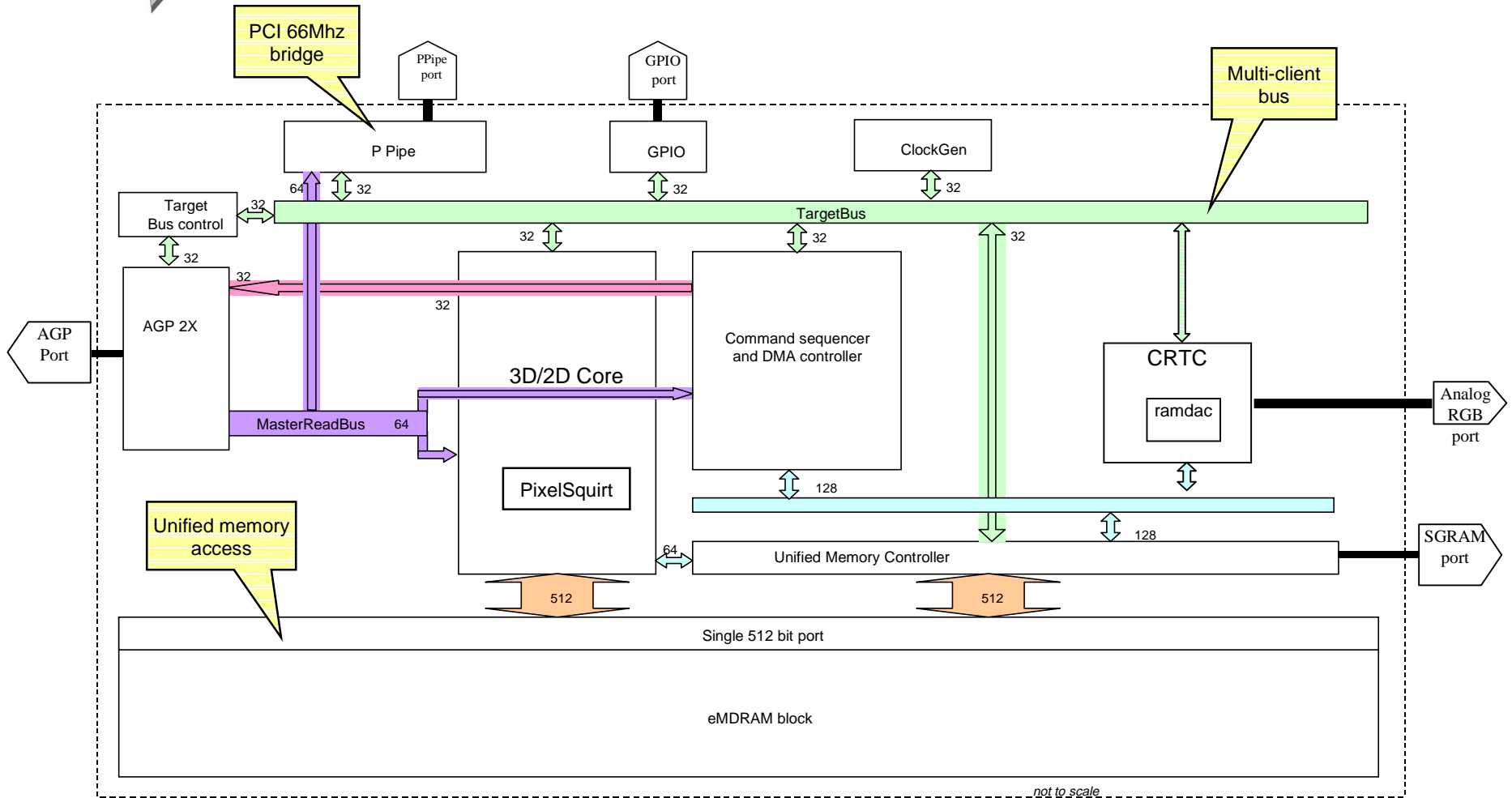


Note: Trilinear Mipmapped, 24 bpp texel, 24-bits Z, 60 fps, Depth Complexity=20, 50% translucency

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VelaTX™ Internal Block Diagram





Summary

- **3D is fundamentally memory storage and bandwidth intensive**
- **T3Ds hit the wall at 1024x768, true color, 60FPS, and increasing depth complexity and texture filters.**
- **Attack the problem from both sides**
 - **Pixelsquirt architecture eliminates the Z portion of the storage problem**
 - **Pixelsquirt architecture reduces the texture bandwidth demand**
 - **eMDRAM architecture increases the texture bandwidth supply**