SA-1500:
A 300 MHz RISC CPU with Attached Media Processor*

Prashant P. Gandhi, Ph.D.

StrongARM and Bridges Division
Computing Enhancement Group
Intel Corporation
Santa Clara, CA 95052

Prashant.Gandhi@intel.com

*SA-1500 was designed by Digital Semiconductor's Palo Alto Design Team.

Outline

- High Level Overview
- System Architecture
- SA-1500 Architecture
- Programming Model
- Companion Chip for Video
- Summary

High Level Overview
Design Goals

- High Performance for Multimedia Applications
- Flexible, General Purpose Architecture
- Easily Targeted for Different Market Segments
- Lower Cost for High Volume
- Low Power

High Level Overview
Specifications

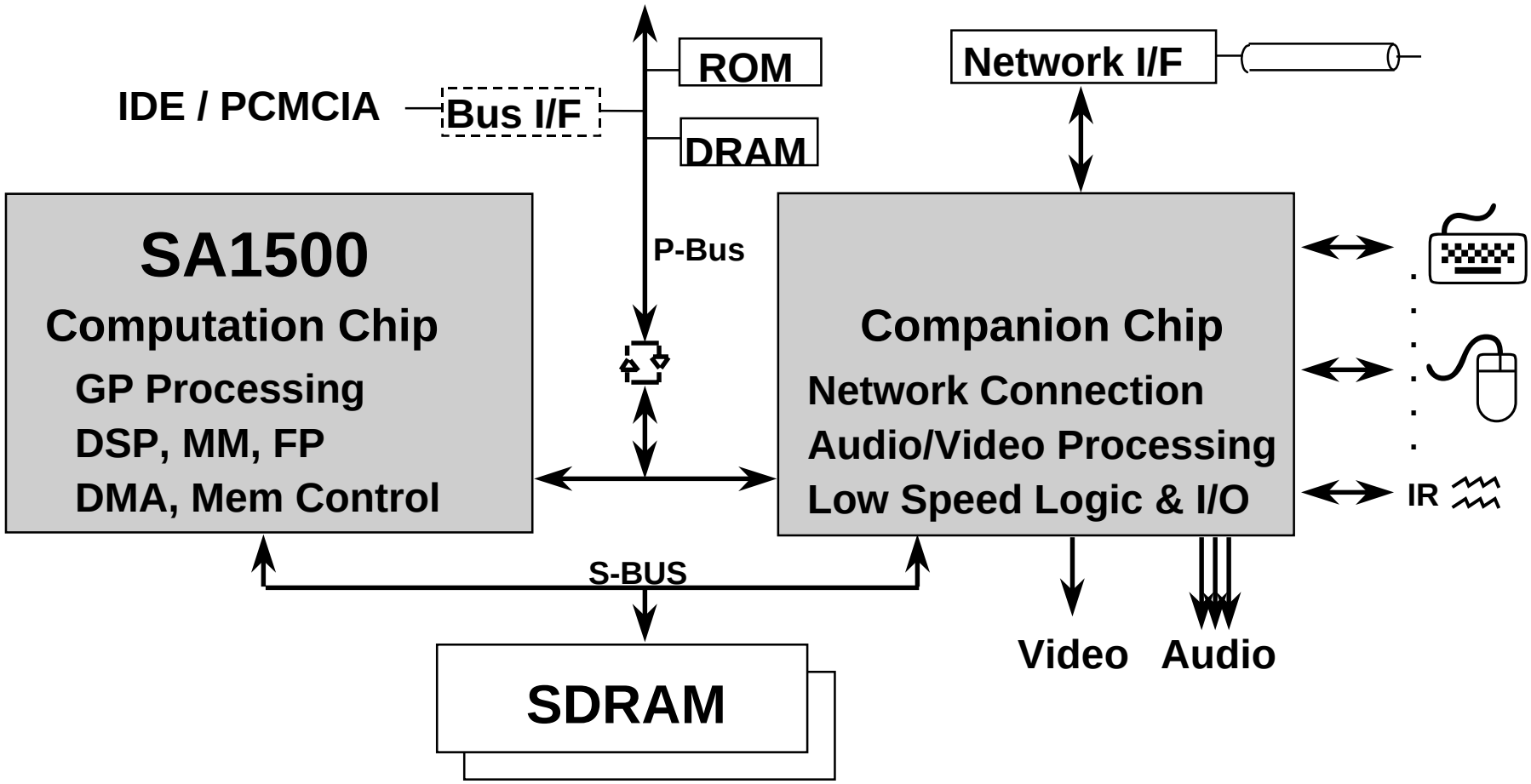
FEATURE	DESCRIPTION
Technology	0.28 micron CMOS
Transistor Count	3.3 Million
Clock Frequency	200-300 MHz
Die Size	60 mm^2
Power Consumption	<0.5 W @ 100MHz <2.5 W @ 300MHz
Voltage	Internal: 1.5-2.0V I/O: 3.3V
Packaging	240-pin MQFP 256-pin PBGA
Clocking	Dynamic clk freq. switching

High Level Overview
Performace Target

- **Replace Microprocessor and DSP-HW in high-volume applications**
- **Numeric and General-Purpose Processing**
  - Multimedia, DSP, and FP Applications
  - MPEG-2 MP@ML with power to spare
  - Modembank and multi-channel voice over IP
  - Video conferencing
- **Soft/scalable architecture**
- **High sustained memory bandwidth**
- **High multimedia code density**
- **Ease of programming**

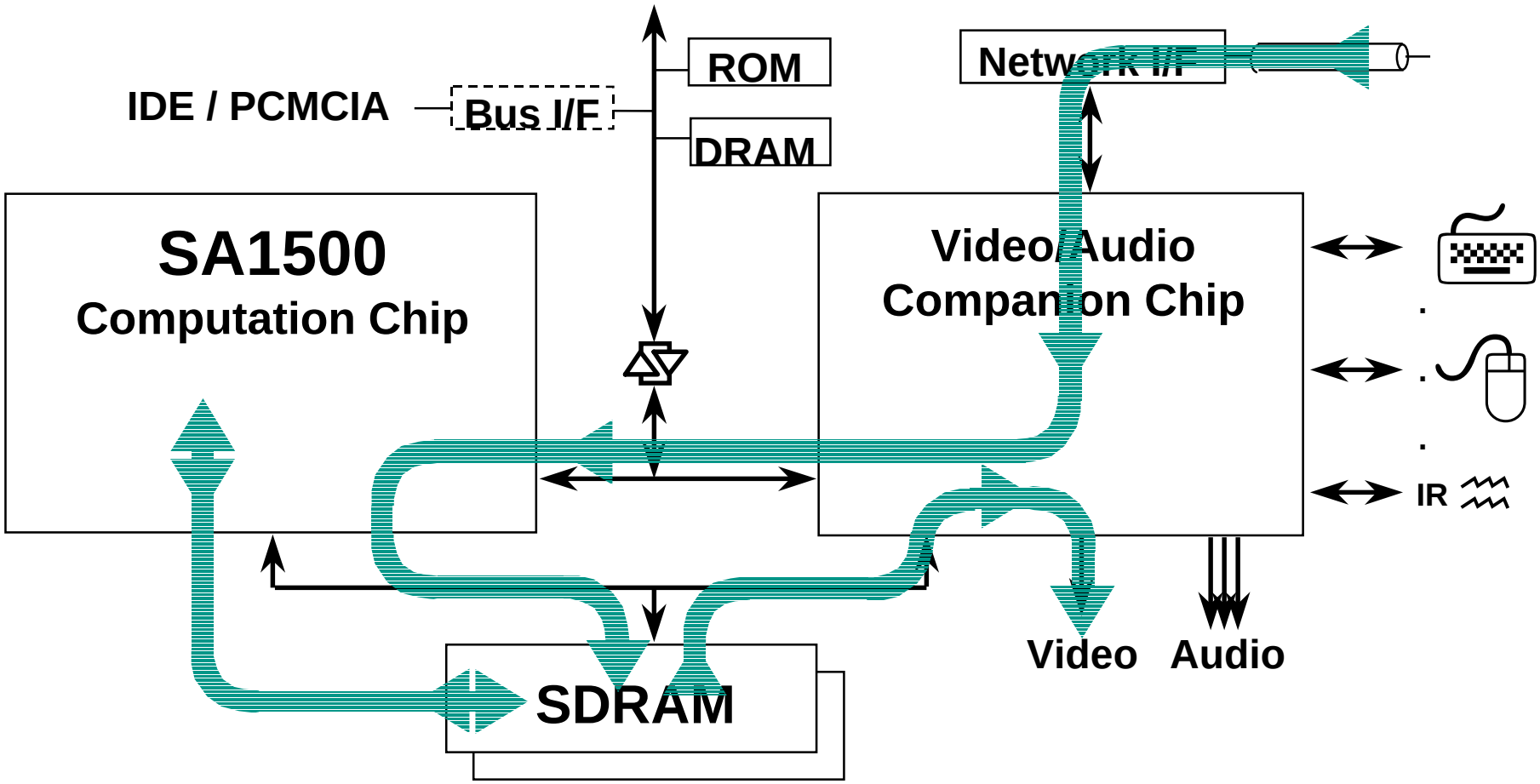
High Level Overview

The System



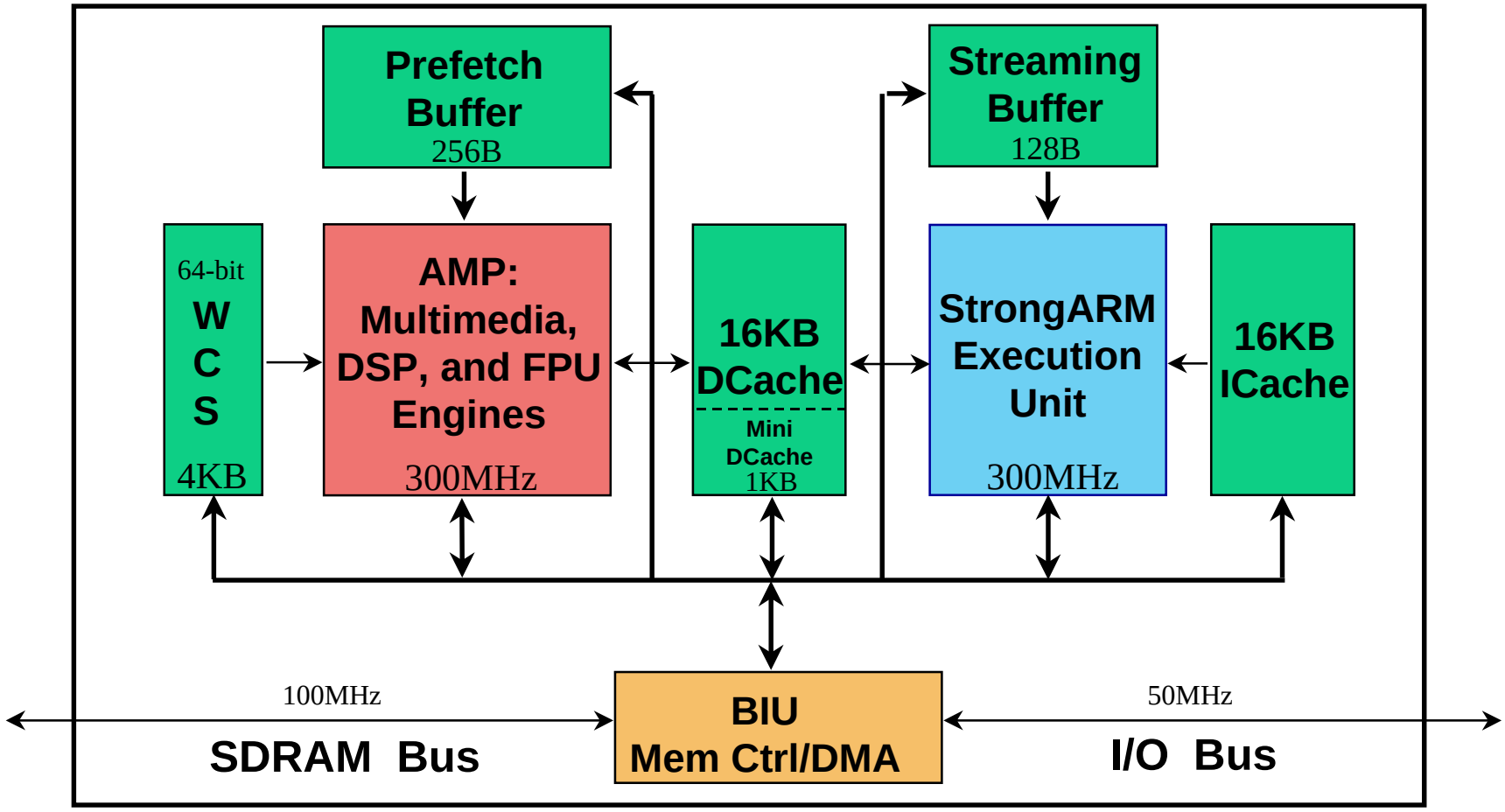
High Level Overview

The System - Data Flow



SA-1500 Architecture

Processor Block Diagram



WCS = Writable Control Store

SA-1500 CPU Attributes

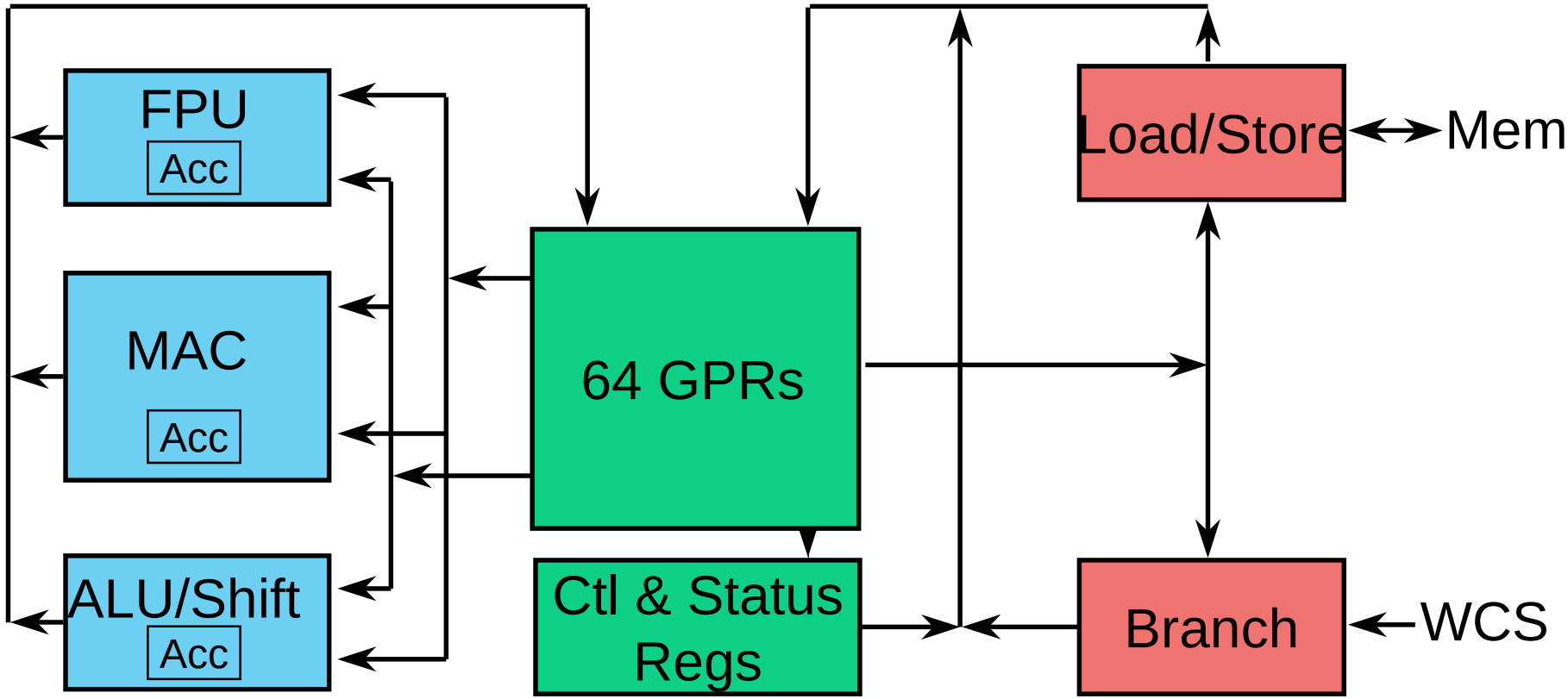
- **Semi-autonomous dual-processor CPU**
  - Master-slave during invocation of AMP
  - Autonomous execution thereafter
- **Non-homogeneous instruction set**
  - 32-bit ARM instructions
  - 64-bit Long Instruction Word (LIW) AMP instructions (Arith || Mem/JMP)
- **Single-instruction Multiple-Data (SIMD) AMP Processing**
  - single-FMAC (32-bit), dual-IMAC (18-bit), quad-SAD (9-bit)
- **Memory Architecture**
  - Shared external memory
  - Shared Data Cache and Write Buffer
  - Separate Instruction Caches (Icache for ARM, WCS for AMP)
  - Separate Stream (pre-fetch) Buffers

SA-1500 Memory Controller and Bus Interface

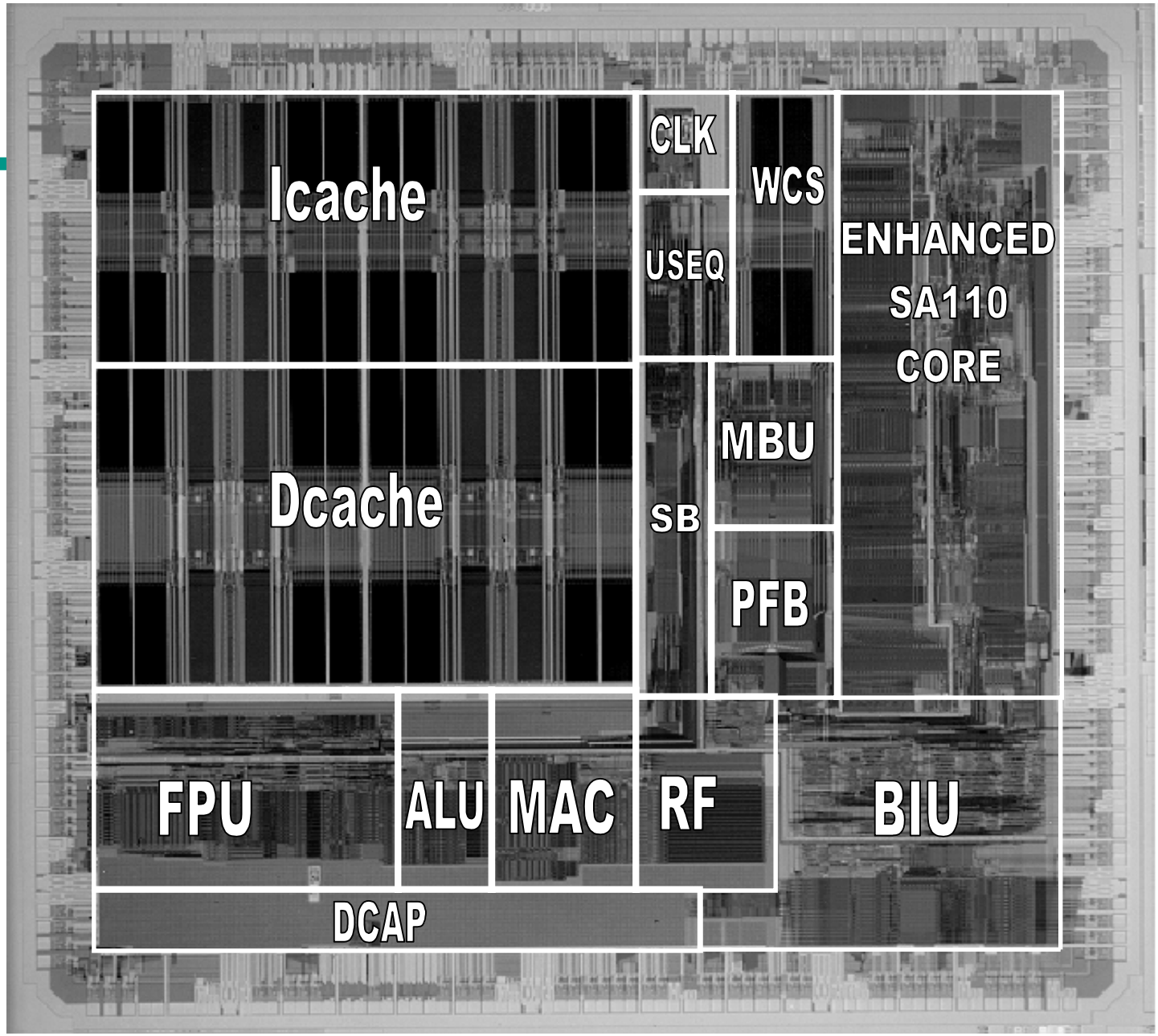
- **100 MHz SDRAM Memory Controller (SBUS):**
  - Programmable bus clock
  - 32-bit mode
- **50 MHz General I/O Bus (PBUS):**
  - Programmable bus clock
  - Direct Connection to:
    - *PC-style I/O devices*
    - *ROM/SRAM/DRAM/Flash*
    - *Bus adapter to PCI, PCMCIA*
- **DMA controller with 15 descriptor-based channels**

StrongARM

AMP Block Diagram



SA-1500 Chip Micrograph



SBD

Processor Features

StrongARM

- 32 bit RISC, ARM V4 Architecture
- 16K Icache, 16K Dcache, Write buff
- High Code Density
- All Instructions Conditional
- Operand Shift Support for ALU Inst
- Powerful 32 x 32 + 64 -> 64 MAC

AMP

- Dual Issue instructions
  - 1x SIMD Arithmetic (ALU, MAC, FPU)
  - 1x Memory or Branch
- Dual personality
  - *coprocessor or parallel processor*
- Variety of Register DataTypes
  - 8/9b, 16/18b, 32/36b, 32-bit FP
  - 64 registers (36 bits wide)
- Fully Pipelined Operations
- 512-instruction WCS

AMP Operations

- **Fully pipelined**

  ***Arithmetic* operations**

- **ALU/MAC/FPU Operations:**
  - 8b mul with scale/round/sat
  - 9b averaging, pack/unpack
  - 9/18b add, sub, motion estimation
  - 18/36b mul, mul-add, mul-sub with scale/round/sat
  - 32/36b add, sub, shift, logical
  - Single Precision FPU: mul-add, mul-sub, div, sqrt

- **Fully pipelined**

  ***Memory and Branch* operations**

- **Load/Store/Branch Operations:**
  - Reg+Disp, Reg+Scaled-Index
  - Reverse-byte, replicate, texel loads
  - Transpose stores with auto-update
  - Single-inst compare and branches
  - Decrement and branch

StrongARM

SA-1500 Instruction Execution

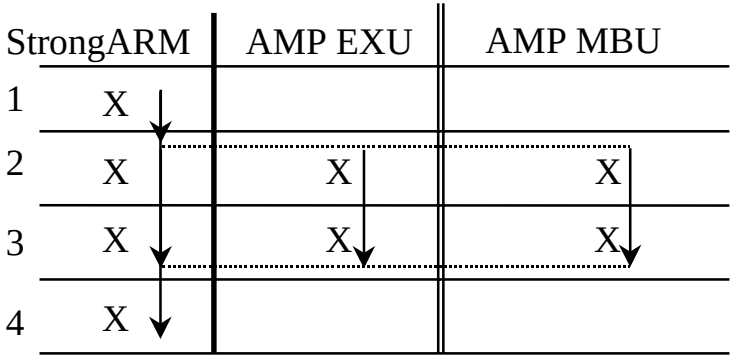
Parallel Method

- StrongARM “library call” to WCS entry
- USAGE:

  MPEG-II Decoding

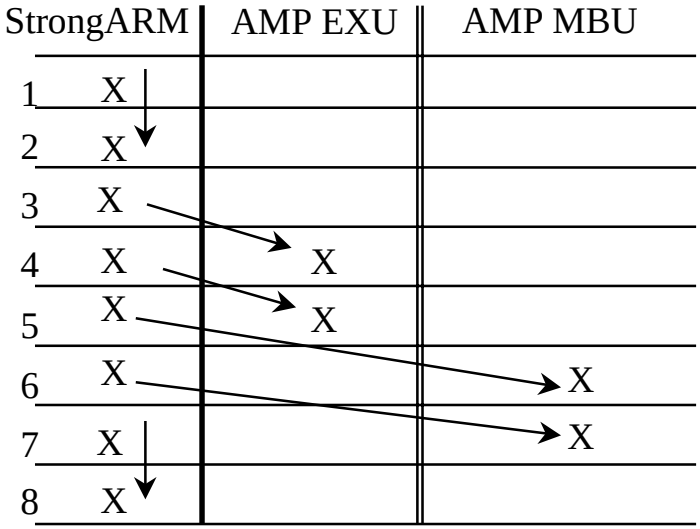
  3-D/Graphics Libraries

  Application-Specific Functions

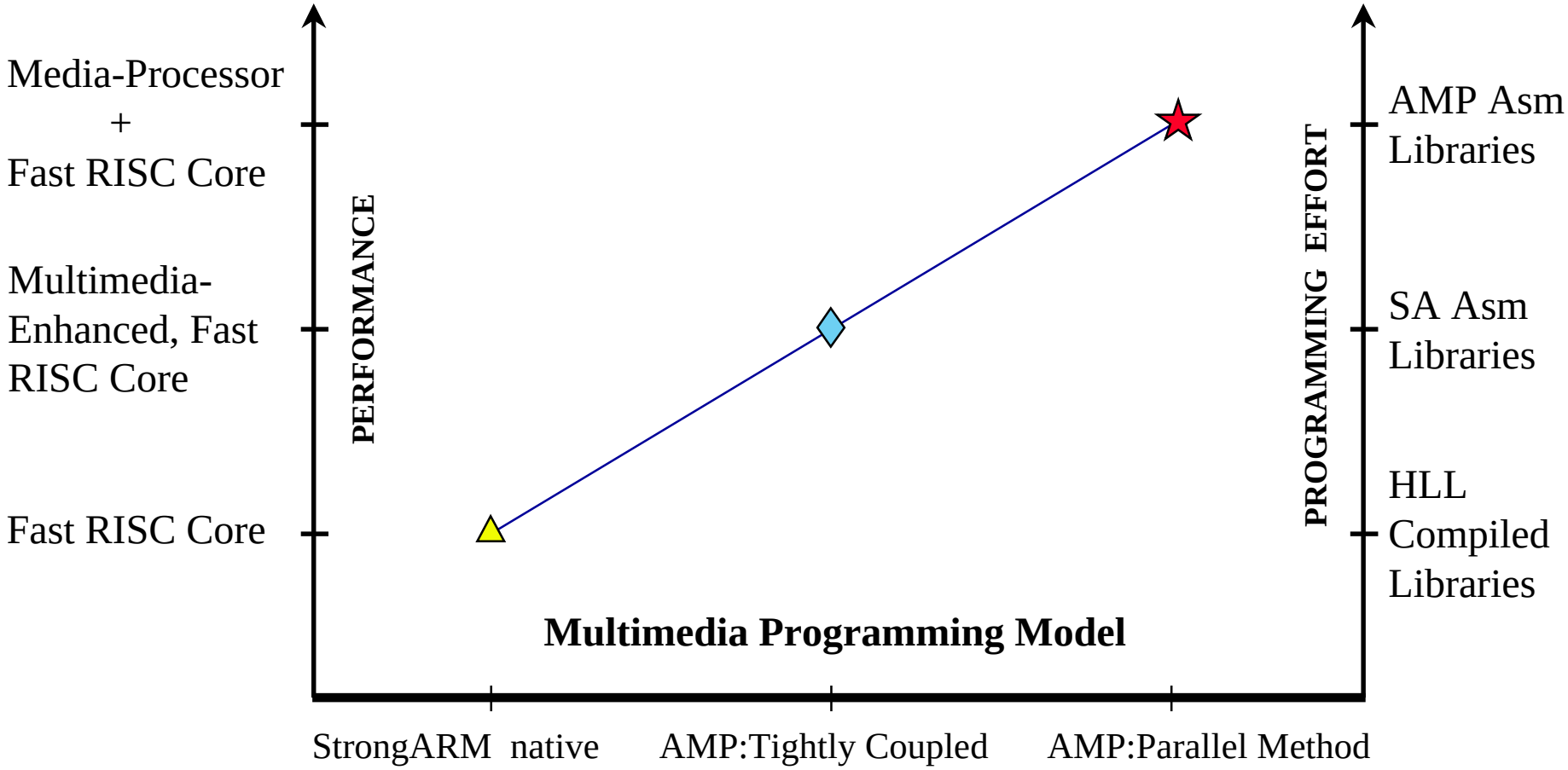


Tightly Coupled Method

- Issue an “Execute” or a “Memory/Branch” operation in StrongARM inst stream
- Supported by the C compiler



SA-1500: Programming Flexibility



Example of AMP Processing Flow

- **FIR Filtering:** $y(m) = \sum_{n=0}^{N-1} h(n)\, x(m-n), \quad m = 0,1,\ldots,M-1$
- **Assume: 16-bit data & coeff, N = 64, M = multiple of 128, dual-MAC processing**
- **AMP Processing:**
  - Prefetch data x[0:63] into PFB[0:63]
  - Load coefficients h[0:63] into registers L0-L31
  - Loop m=1:M/128
    - *Prefetch data x[m*64:m*64+63] into PFB[64:128]*
    - *Compute and store y[(m-1)*64: (m-1)*64+63]*
    - *Prefetch data x[(m+1)*64:(m+1)*64+63] into PFB[0:63]*
    - *Compute and store y[m*64: m*64+63]*
  - Update FIR states x[0:63]

Multimedia Processing

- **MPEG-2 Decode**
  - Main Level/Main Profile: 720x480x30FPS
  - Processor Load Balancing:
    - *StrongARM: All processing above MacroBlocks (coded in C)*
    - *AMP: MacroBlocks down (hand-coded)*
  - Audio processing using FPU
- **Modembanks**
  - Can Support multiple modems (V.34 or V.90)
- **Video Conferencing**
  - H.324
- **Voice over IP**
  - Can support multiple digital voice channels (ITU G.72x plus echo cancellation)

StrongARM

Example Application: MPEG-2 decode

Transport Stream De-multiplex

- Companion chip: Filters transport stream
  Adds timestamps for synchronization
  Tags packets, DMA's into SDRAM
- StrongARM: Splits stream into components

Audio Decoding: *Decodes MPEG 2 audio in software*

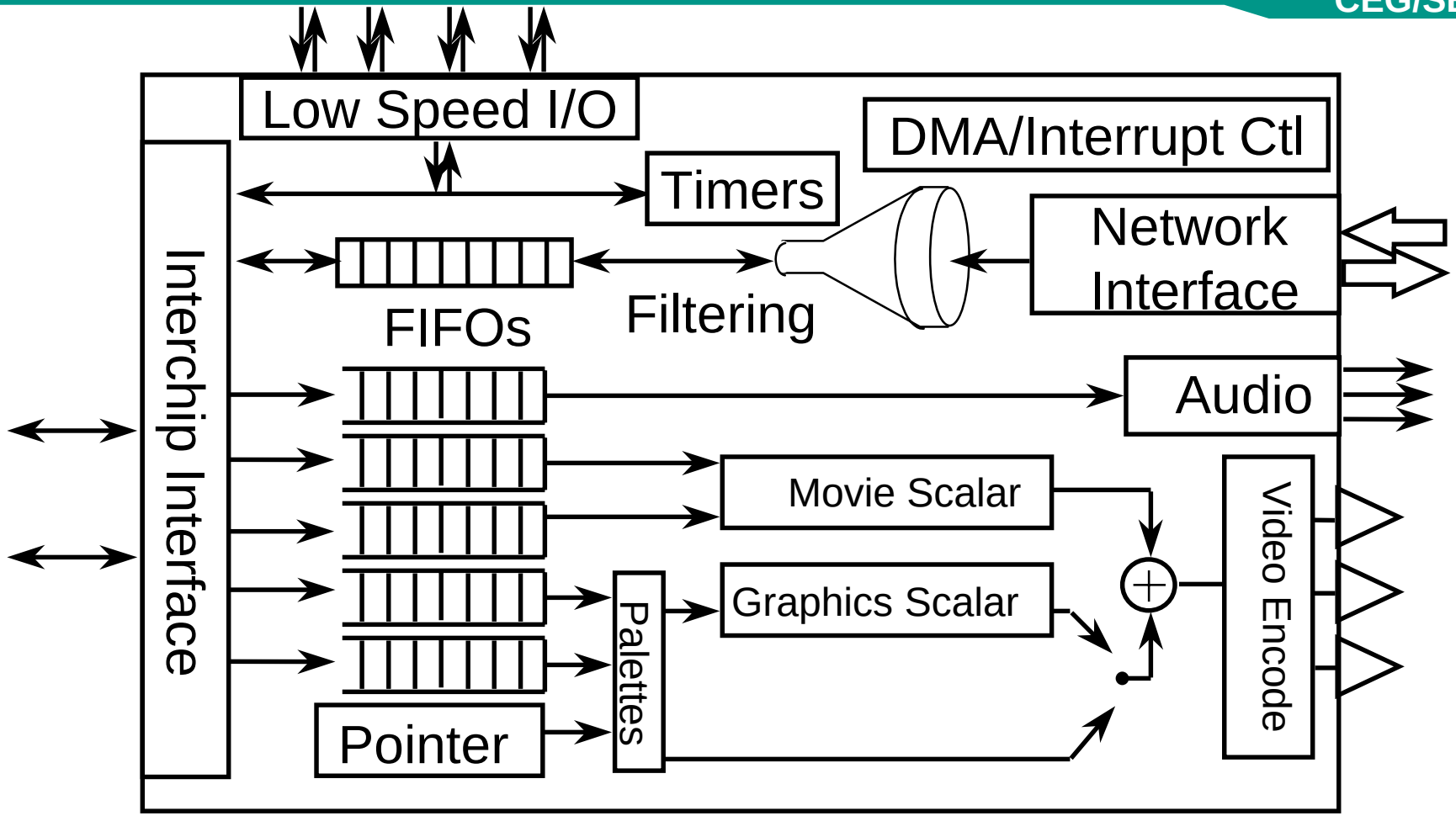
- StrongARM: Control, bitstream parsing, dequantize, float
- AMP : IDCT, windowing, fix pt cvt, store
- Companion chip: Formats, drives external DACs (x6)

Video Decoding: *Can decode full MPEG-2 MP@ML in software*

- StrongARM: Control, bitstream parsing, VLC decoding
- AMP : Dequantize, IDCT, motion-reconstruction
- Companion chip: Scaling, mixing with overlay data Pan & Scan

StrongARM

Companion Chip: Architecture



Companion Chip: Video/Network

- **Flexible Network Interface w/ Packet Filtering**
  - up to155 Mbit receive and transmit channels
- **ITU601Digital Video Generation System**
  - Movie Stream and Palletized Graphics
  - Up/down horizontal scaling (320 tap filter)
  - Palletized Cursor/Pointer overlay
  - Variable mix of Movie and Graphics
  - On chip fully programmable pixel clock VCO/PLL
- **Digital Video Output**
  - NTSC, PAL encoding, or direct monitor drive
  - Macrovision(tm) Anti-taping Option
  - Composite, S-Video or RGB output

Companion Chip: Low Speed I/O

- Serial Ports
  - Up to 6 Channel Audio Output System
    Serial Digital Output to External DACs
  - IrDA + Generic Infra-Red Interfaces
  - Telephone Quality CODEC Interface for Audio Input
  - PS/2 Keyboard/Mouse Interfaces
  - Smart Card Interface
- IEEE1284 Parallel Port Interface
- General Purpose Timers
- Flexible Interrupt Controller
- General Purpose I/Os