MXi: A High Performance X86 Processor With Integrated 3D Graphics

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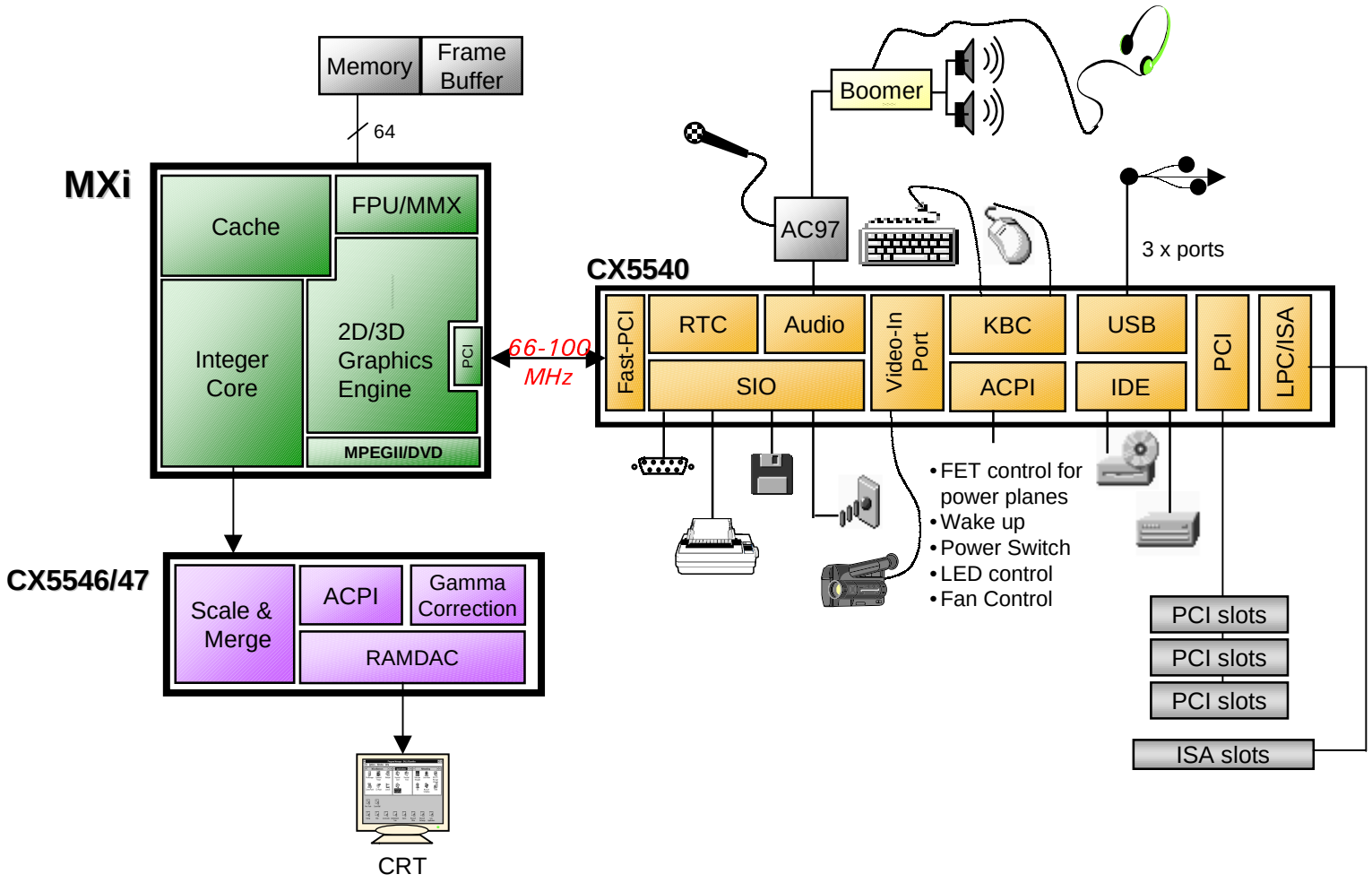
MXi Architectural Features

- **Next-generation Cayenne Core**
  - Dual-issue pipelined FP and MMX™
  - Optimized instructions for 3D graphics
  - 64 KB unified L1 cache
- **Integrated graphics subsystem**
  - Accelerated 2D/3D operations
  - MPEG2 motion compensation for DVD
- **Tightly coupled SDRAM interface**
  - Very low latency
  - Up to 16 simultaneously open banks

MXi System Solution



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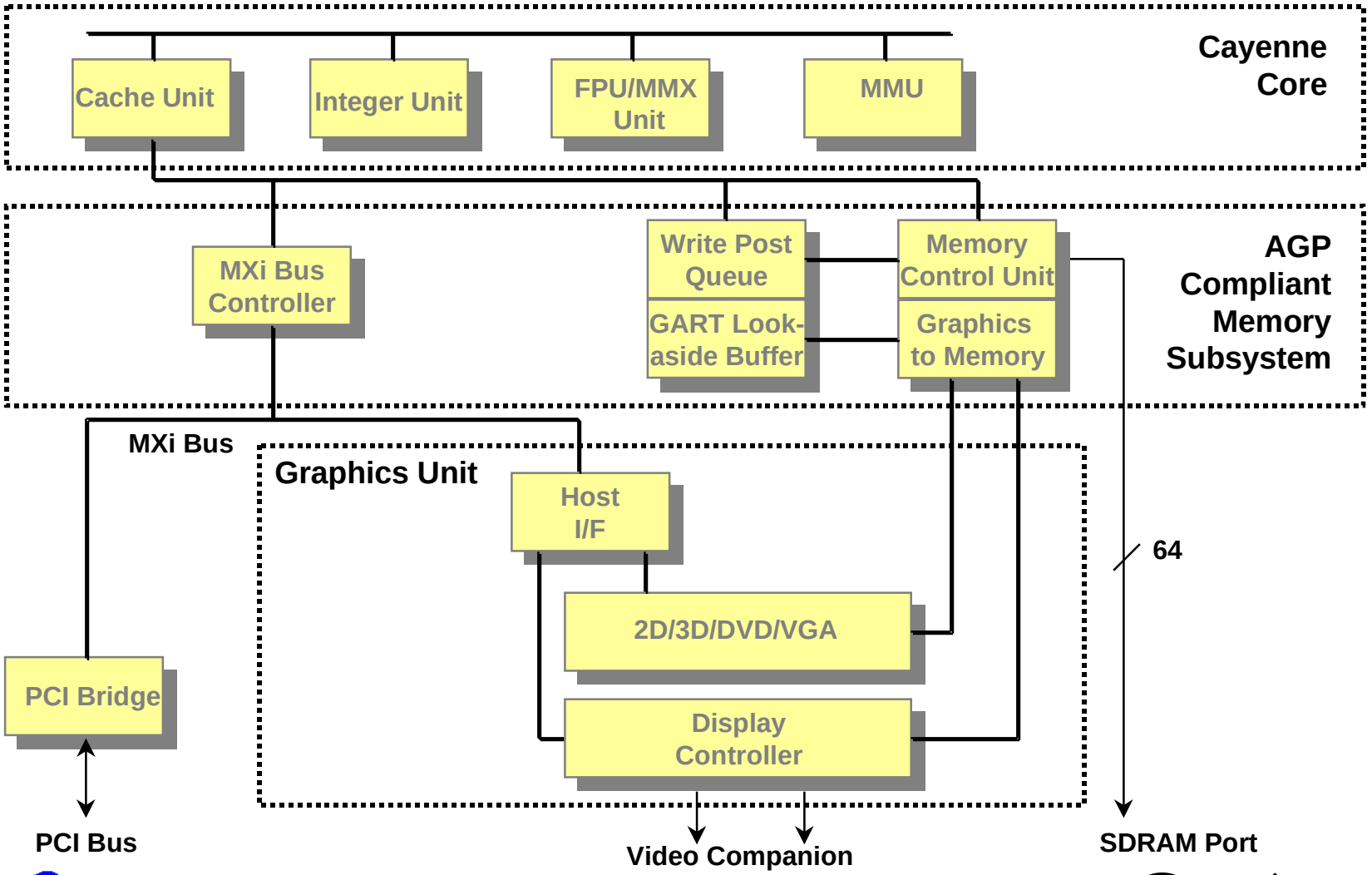
MXi Processor Block Diagram



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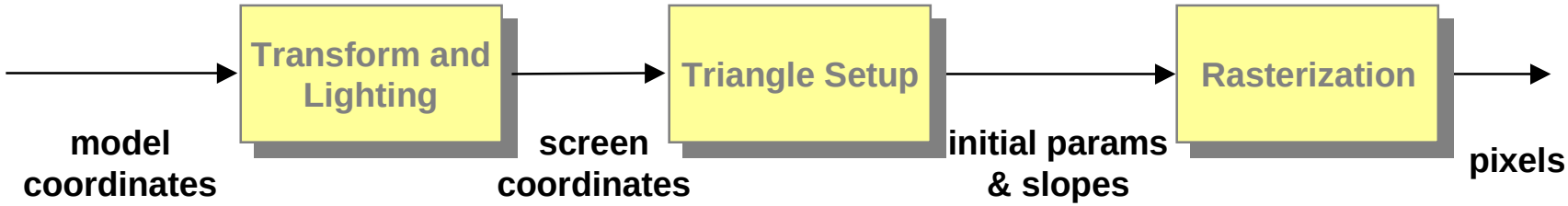
Basic 3D Pipeline

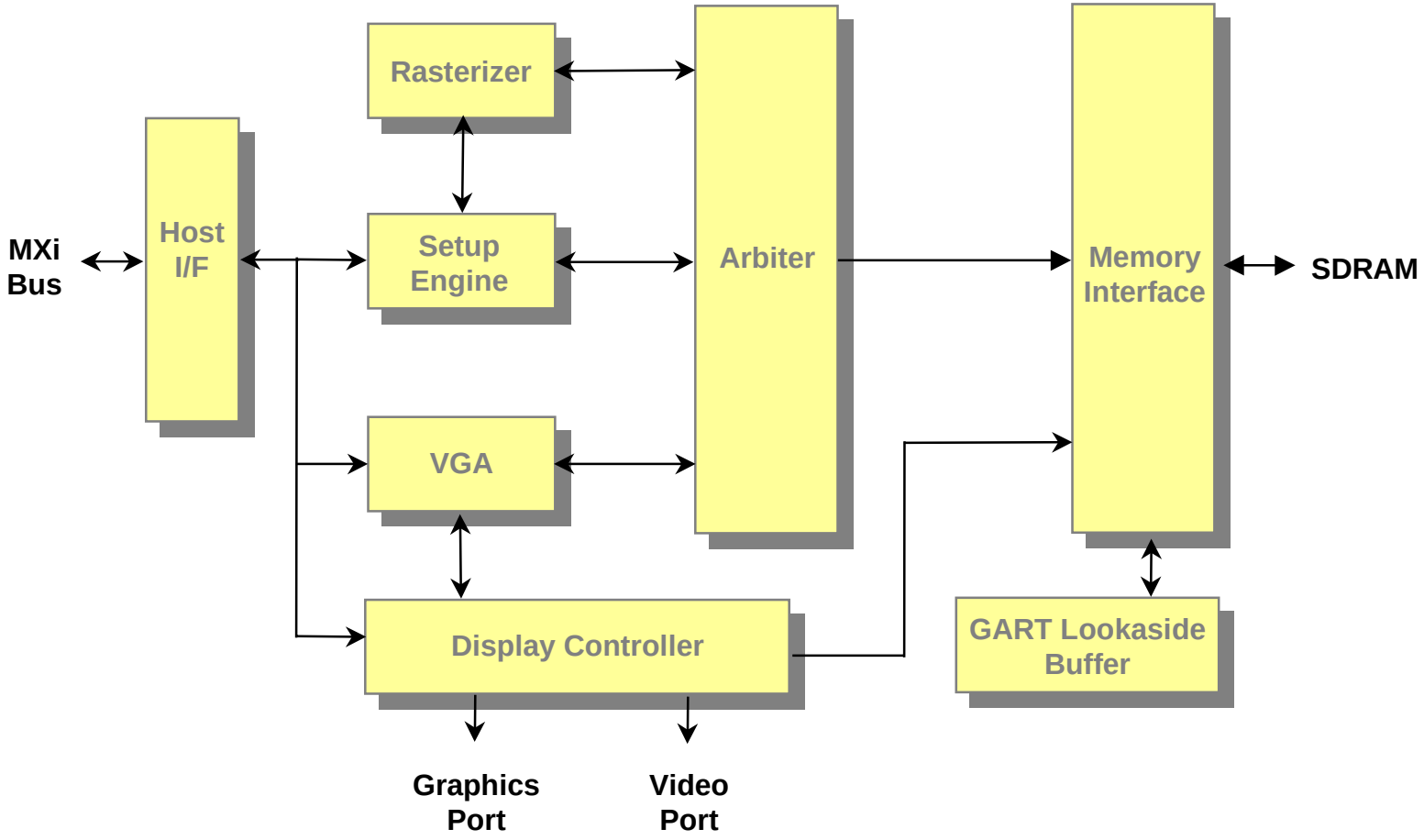


- **Cayenne Core handles transform and lighting**
  - Floating point intensive
- **Graphics Unit offloads remainder of pipeline**
  - Highly parallel computations
  - Data intensive
- **Workload split frees CPU bandwidth for application use**

3D FP Extensions

- **Two single-precision floating point results per operation**
- **Dual-issue, including floating multiply and add**
  - Up to 4x throughput on the inner loops of matrix multiplies and vector dot products
- **Reciprocal and 1/sqrt operations**
  - Perspective projection for transform
  - Vector normalization for lighting calculations
  - Significantly faster than division
- **Fully pipelined**

MXi Graphics Subsystem



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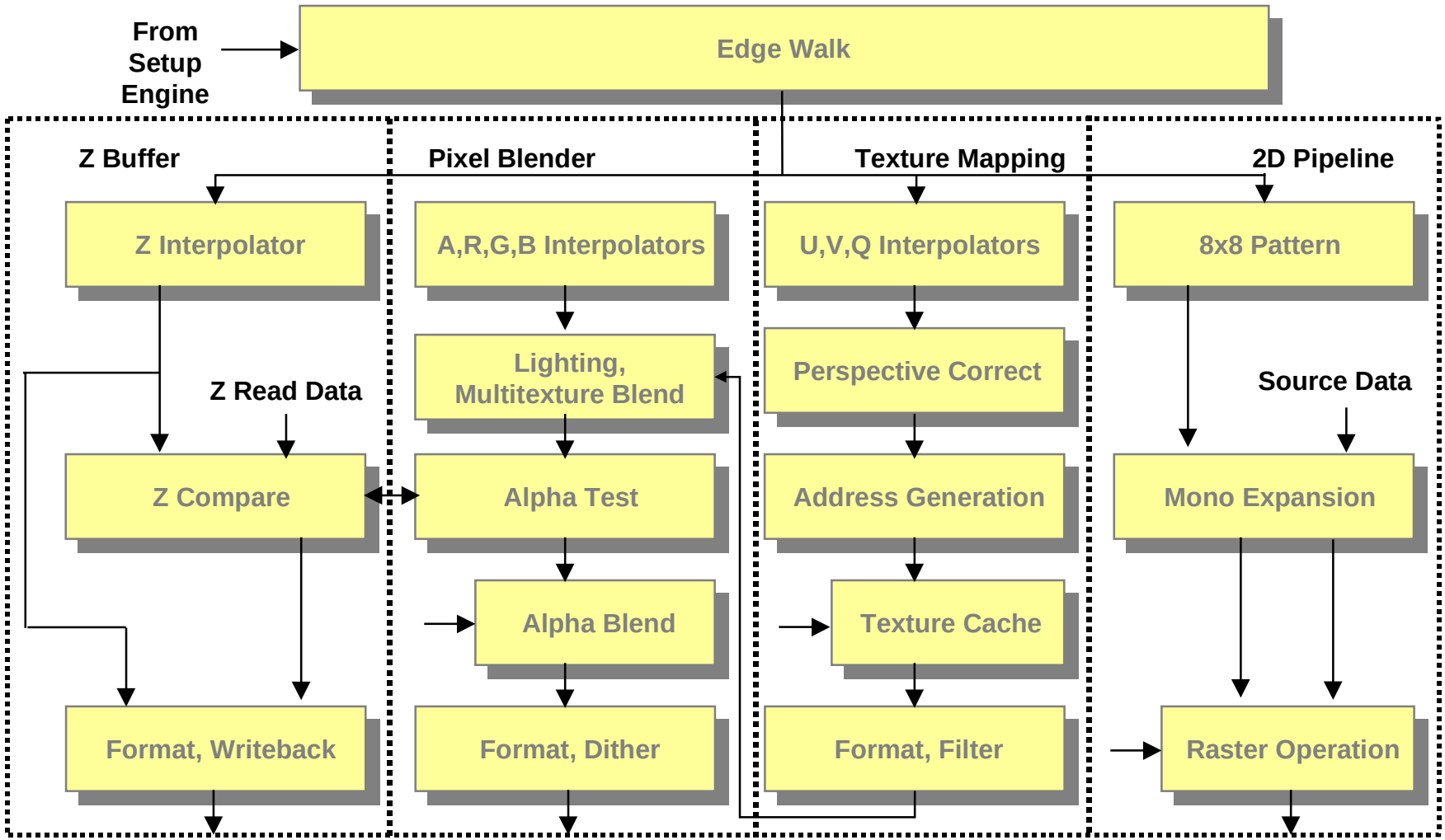
Graphics Setup Engine

- **Microcoded architecture for flexibility**
  - Permits optimization for changing APIs
  - Handles 2D and DVD operations in addition to 3D triangle setup
  - Pipelined multiply-accumulate
  - 2KB I-Cache, 2KB Scratchpad RAM
- **Specialized DMA engine**
  - Performs float-to-fixed conversion on incoming data
  - Handles vertex sorting
- **Maximizes concurrency with x86 core**
  - 64 entry command FIFO
  - Direct execution of display lists in memory

Graphics Rasterizer

- **Triangles, vectors, planar trapezoids**
- **High performance perspective-correct texture mapping**
  - 4KB, 4-way set associative texture cache; pipelined
  - Single cycle bilinear, dual-cycle trilinear filtering
  - Level Of Detail per-pixel MIP mapping
  - Dual textures with flexible blending options
  - Many texture formats, including palletized and YUV
- **8, 16, and 32-bit Z buffer**
- **Fog table support / simultaneous alpha & fog**
- **Also handles 2D and DVD operations**

Rasterizer Pipeline



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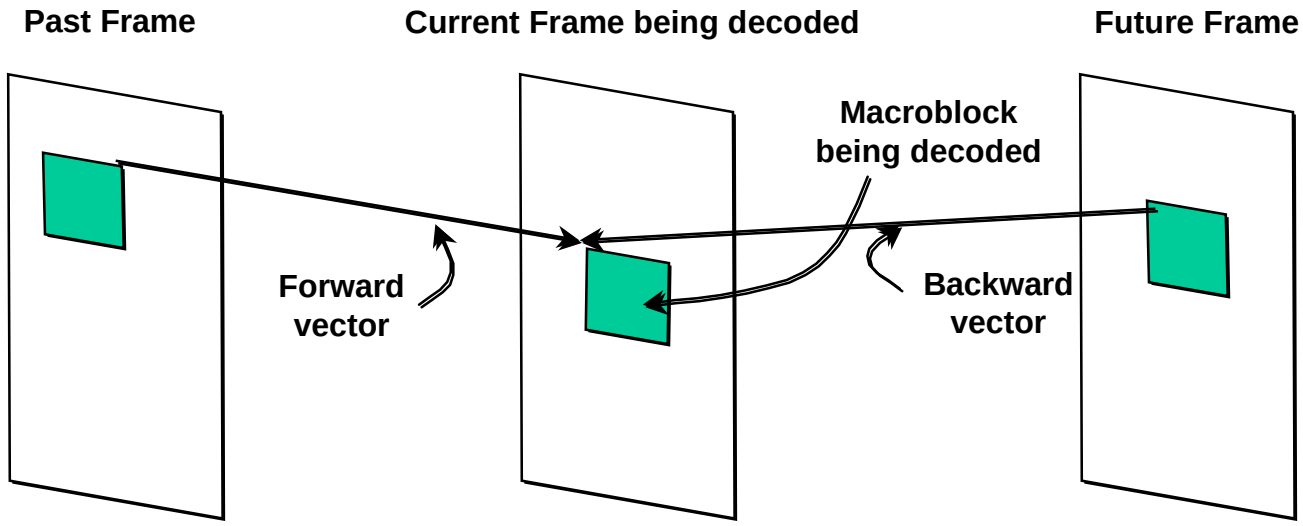
MPEG2/DVD Playback

- Consumer quality DVD playback based on Mediamatics™ MVCCA™ architecture
- Cayenne Core handles MPEG stream parsing, Huffman decode, and inverse DCT
- Graphics Unit handles motion compensation
- Display Controller supports planar YUV 420 surfaces
- Graphics Companion provides YUV to RGB conversion, scaling, and DVD subpicture support

Motion Compensation



- Each 8x8 macroblock in the decoded frame can reference past and future frames, plus an error term
- The Setup Engine parses motion vectors for an entire frame at a time

Graphics Performance

- **Maximize concurrency to deliver sustained frame rates**
  - CPU can queue large numbers of display lists
  - Setup Engine can queue 4-5 primitives for rasterizer
- **Graphics Setup Engine**
  - Operates at 1x, 2x, 3x, 4x SDRAM clock
  - Triangle setup is 300-400 clocks (~1M tri/sec)
- **Rasterizer**
  - Operates at SDRAM clock
  - 3D operations at one pixel per clock for single texture, one pixel per two clocks for dual texture
  - 133 Mpix/sec 3D, ~1 GB/sec 2D peak fill rate

MXi Statistics/Current Status

- ~10M transistors
- Die size ~100 mm2
  (National's own .18 um, 5 layer metal process)
- 320 PGA package
- Power: 15W typical
- Working silicon is in the lab
- Production 2Q99, General Samples 1Q99