Two Chipsets for DTV

Compliant with ATSC Standard

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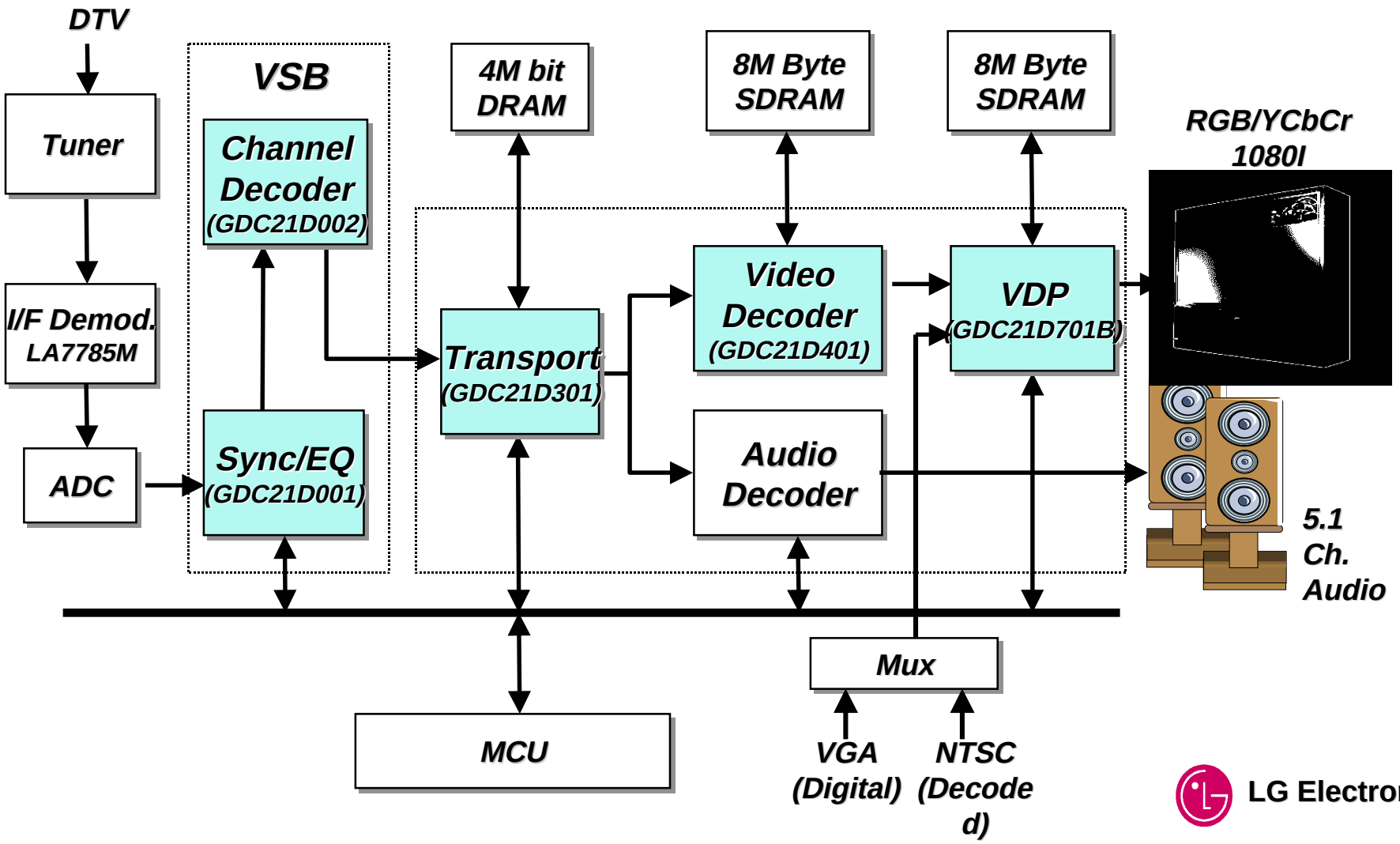
Introduction

- 1. st & 2. nd generation chipsets compatible with ATSC DTV standard
- Support 5 VSB modes : Terrestrial 8VSB and MMDS 2/4/8/16 VSB
- Transport demux having 16 bits interface with MCU
- MPEG2 MP@HL Video decoding including all 18 ATSC formats
- Video format conversion, any transmission to HD(1080I, 1. st gen.) or SD(480I/P, 2. nd gen.) display
- Seamless image format change

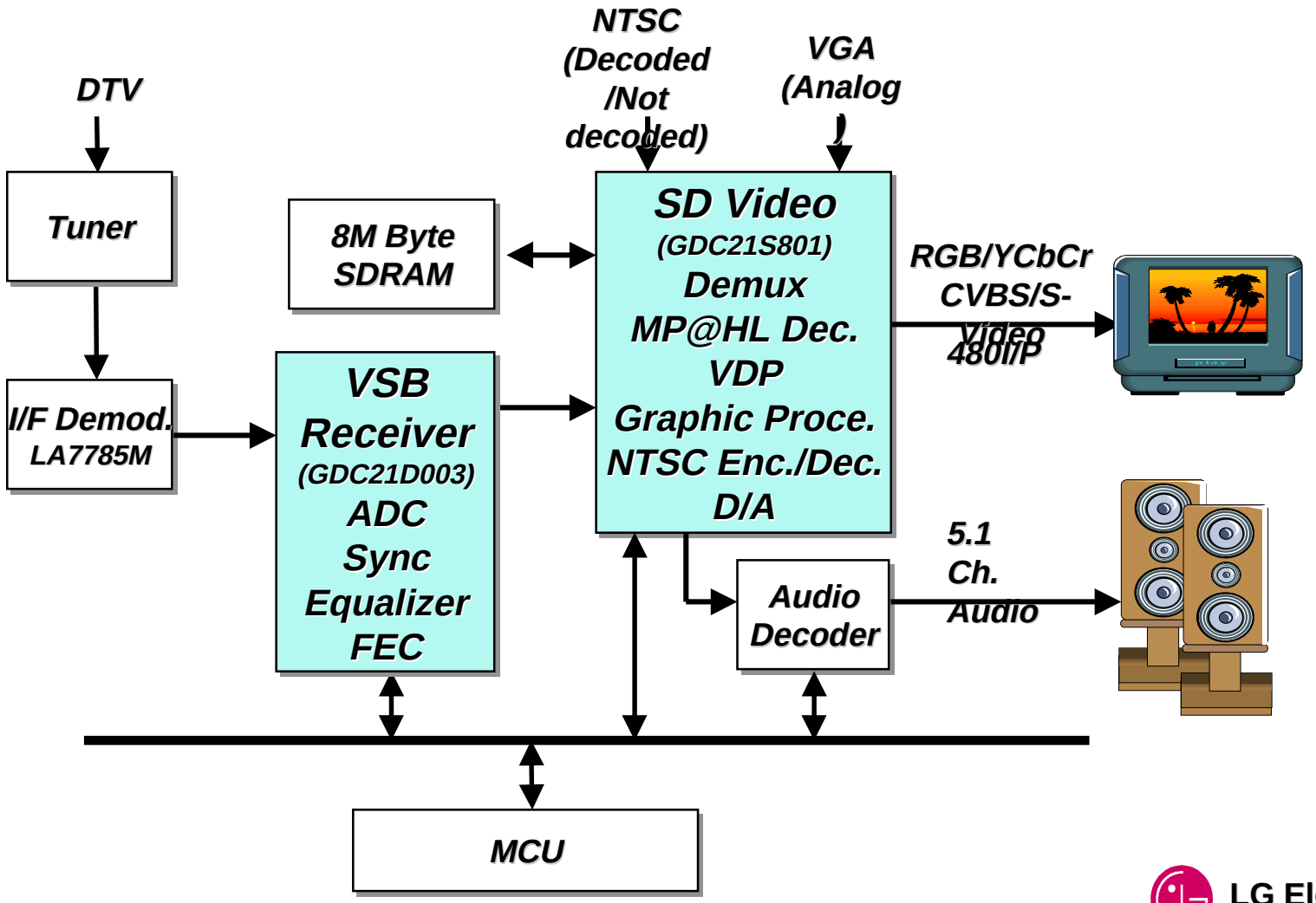
Chipset partitions

1. st Generation Chipset Partition(5 chips, HD)



Chipset partitions

2. nd Generation Chipset Partition(2 chips, SD)



Features of Video Chips

TP Decoder(1st Gen.)

- Byte-parallel/bit-serial MPEG-2 TS input
- Audio PES/Video ES output
- Identify 32 PIDs
- Extract DTS/PTS for video decoder
- PCR recovery
- Error code insertion for video
- 8/16-bit bus host interface
- Max. TS input rate : 80Mbit/s

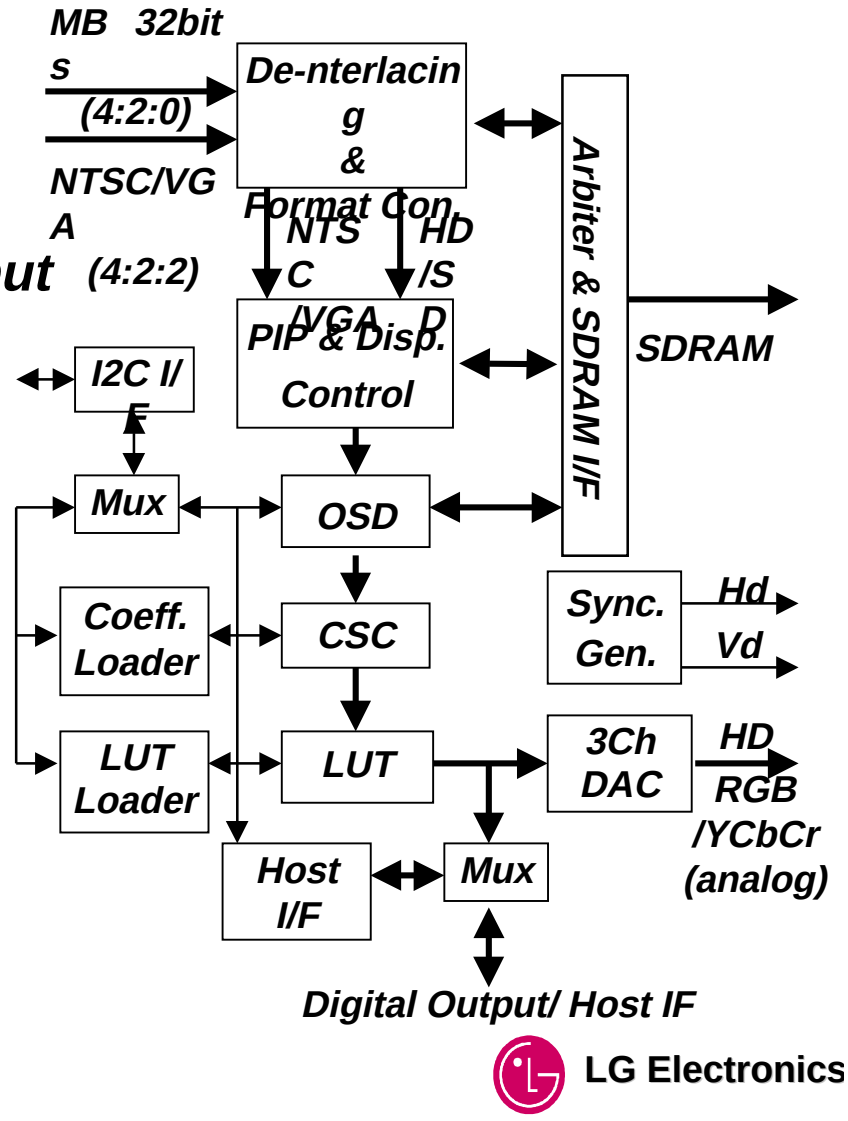
Video Decoder(1st Gen.)

- Decodable 18 input formats of ATSC standard
- Tricky mode decoding
- MB 4 pixel parallel output
- Decoding operation up to 54MHz
- 64bit Bus Mem. I/F (Four 1Mx16 SDRAM)
- Up to 81MHz asyn. Memory I/F

Features of Video Chips

Video Display Processor(1st Gen.)

- 18 ATSC formats, 480x768I/P(NTSC), 480x640P, 768x1024P(SVGA) input
- Analog/digital 1080 RGB/YCbCr output
- De-interlacing using 3 field memory for 480I input
- 9-tap horizontal peaking filter
- PIP/Multi-PIP/Zoom
- 2/4/16/256-colors/4-pixels OSD
- RGB/YCbCr Color Space Converter
- 8-bit custom controlled LUT
- Host I/F: 16 bit parallel or I^2C I/F



Features of Video Chips

Features of SD Video(2. nd Gen.)

- One-chip for TP, VD, VDP & NTSC
- MPEG2-TS/PES, DVD, DSS-SD(HD), & MPEG-1 Decoding up to 100Mbps
- EPG/SI(PAT,PMT,PSIP, etc) section filtering and CRC checking
- Identify 32 packet PIDs/table IDs
- PCR recovery
- PES layer audio output
- Down Conversion for HD stream
- Slice-based error concealment
- Tricky mode decoding
- Input picture formats : 18 ATSC /DSS(4:2:0), NTSC, VGA(4:4:4)
- Output picture formats : Analog RGB/YCbCr/CVBS/S-Video & Digital 480x852I/P, 480x768I/P
- 3-D de-interlacing using 3 field memory for 480I input

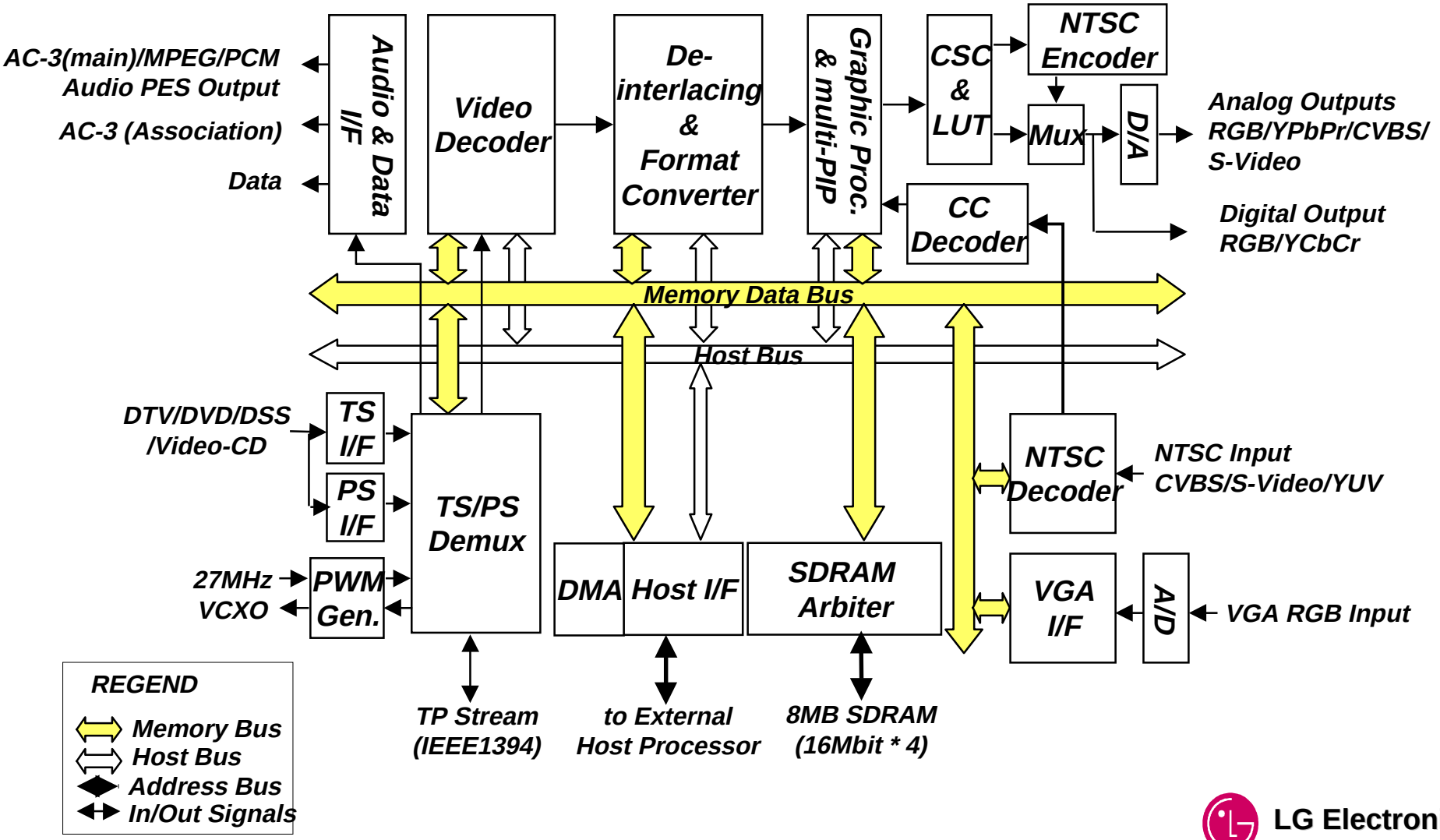
Features of Video Chips

Features of SD Video(2nd Gen.)

- Seamless image format change
- PIP/Multi-PIP/Zoom/D-window
- 4 layer full screen bit-map OSD (2/4/8bits color or 8bits blending)
- NTSC Decoder/Encoder
- Fully compatible with EIA-608 NTSC closed caption
- Analog VGA Interface(4:4:4)
  - 3-channel 10-bit A/D
  - RGB to YCbCr Color Space Converter
- Max. 600Mbits/s bandwidth at VGA main, DTV PIP, Dual prime decoding, and full screen OSD
- Video contents protection(V-chip)
- 16bits host interface
- 8MB SDRAM interface
- No dead-lock condition
- Boundary scan test (JTAG)
- 0.35μm /3.3V/352BGA

Features of Video Chips

Block Diagram of SD Video(2nd Gen.)



Features of VSB Chips

Sync/Eq (1st Gen.)

- Coherent & non-coherent AGC
- DC reduction
- Timing recovery
- Data segment sync and Frame sync recovery
- NTSC rejection comb filter
- Decision-feedback equalizer
- 64 tap FF & 192 tap FB Filter
- Phase corrector

VSB Ch. Dec.(1st Gen.)

- 4&8 states TCM decoder : L=16
- Slice prediction for phase corrector
- De-interleaver
- Reed-Solomon decoder(208,188)
- Error flag insertion on errorneous packet
- Tri-state parallel/serial MPEG-2 transport I/F
- Internal segment error counter

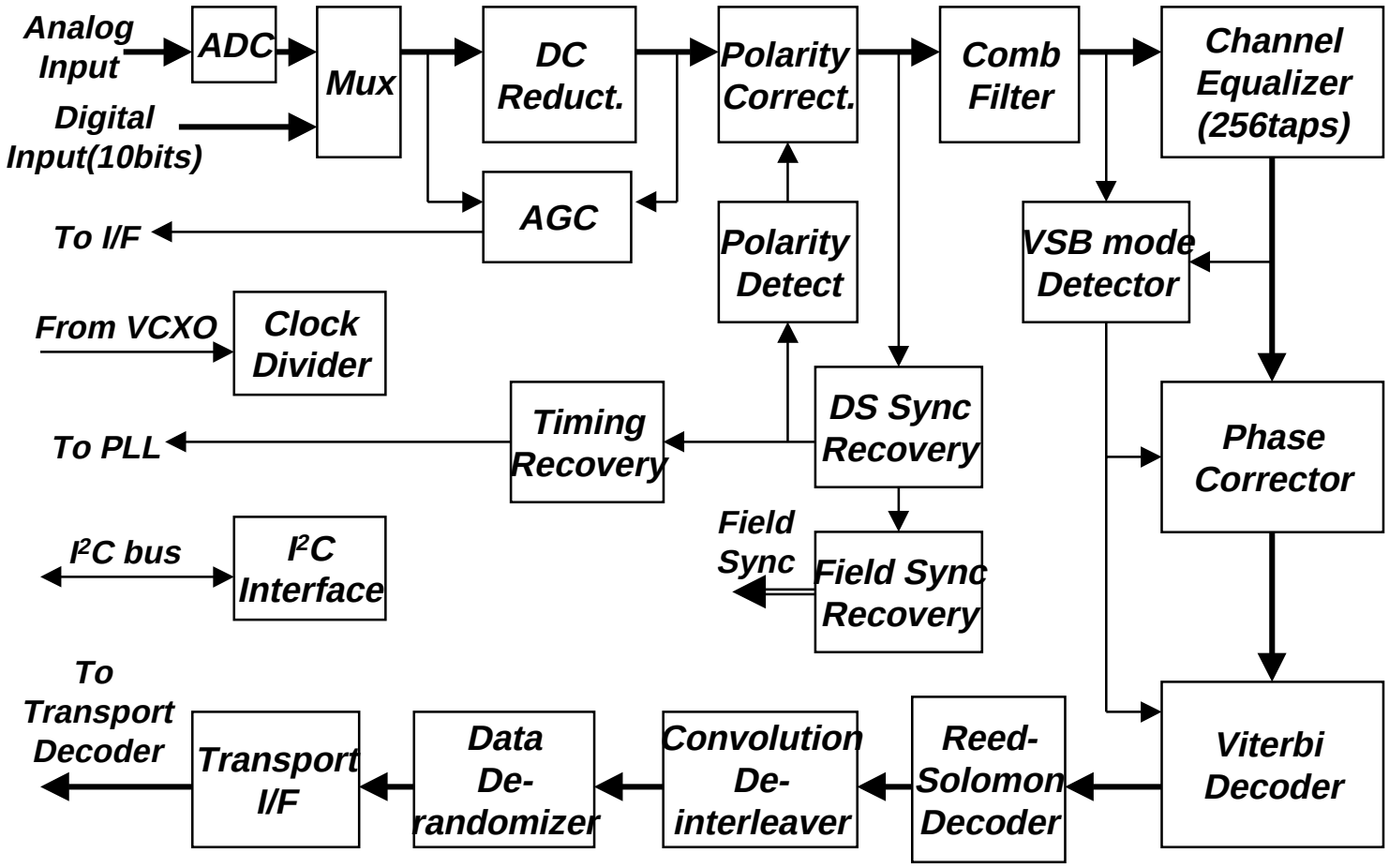
Features of VSB Chips

Features of 1 Chip VSB Receiver(2nd Gen.)

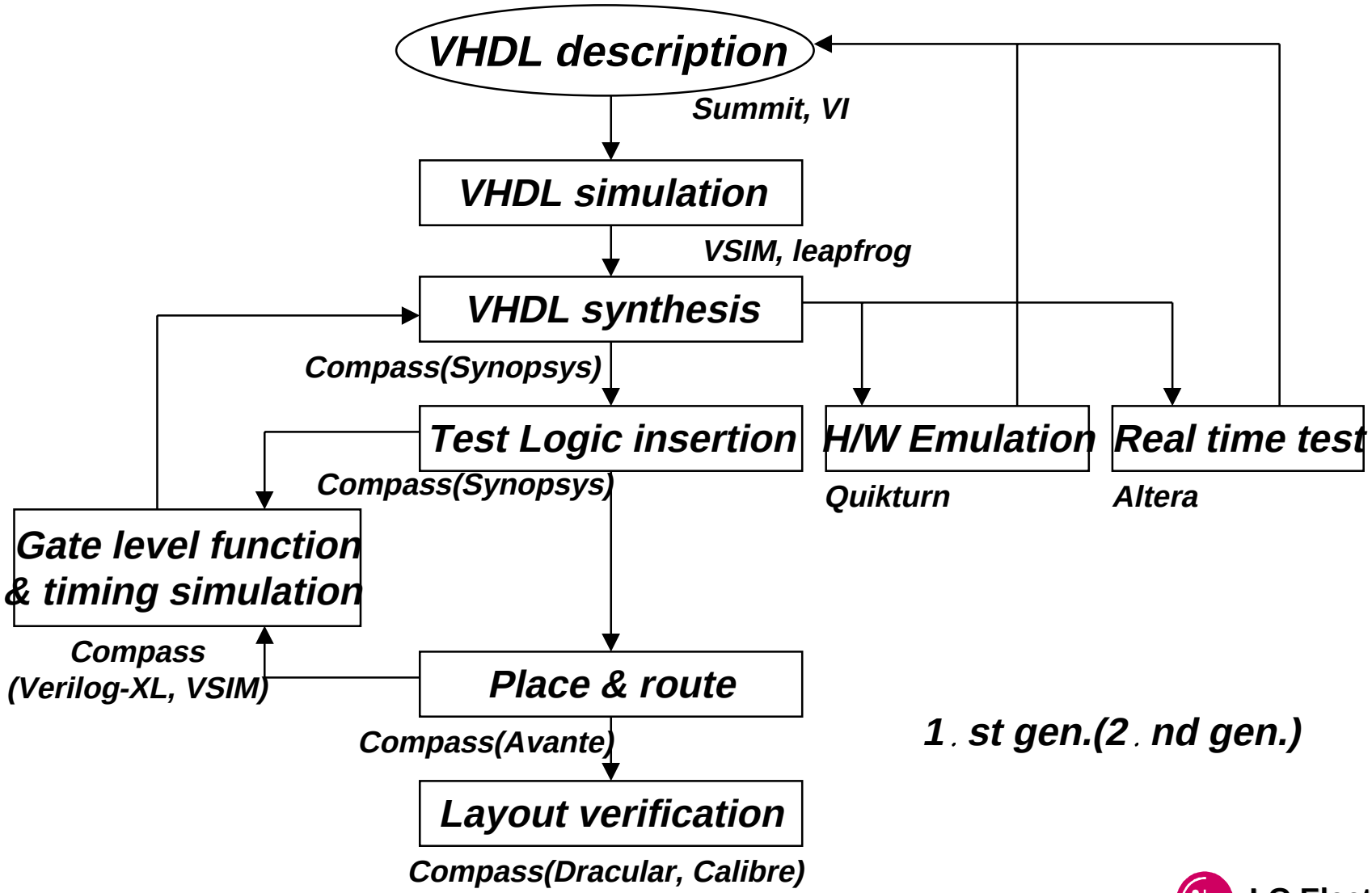
- 10bits differential ADC (1Vpp)
- Coherent & non-coherent AGC
- Modified DS/Frame sync recovery
- Auto NTSC rejection comb filter
- Enhanced VSB mode detector
- Decision-feedback and Blind(D-D mode) Equalizer
- 64 tap FF & 192 tap FB Filter
- Concurrent coefficients updating
- Monitoring equalizer coefficients
- Intelligent loop controlled Phase Corrector
- 4&8 states TCM decoder : L=16
- Error flag insertion on error
- Tri-state parallel MPEG-2 TP I/F
- Internal segment error counter
- I^2C bus Interface
- 0.35μm /3.3V
- 128pin HQFP

Features of VSB Chips

Block Diagram of 1 Chip VSB Receiver(2nd Gen.)



Design Methodology



1. st gen.(2. nd gen.)

Implementation of 1st Gen. Chipset

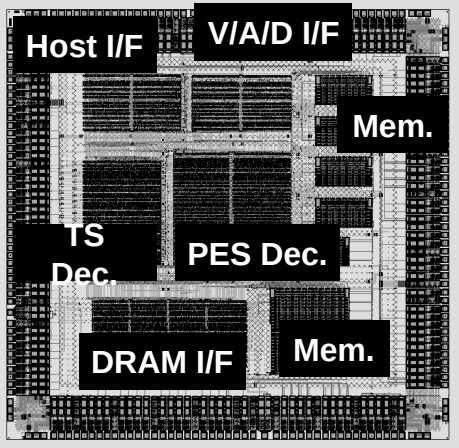
Summary of 1st gen. chipset implementation

Chips	TP	VD	VDP	Sync/Eq	VCD
Die size	6x6	13x12	9x9	12x12	10x9
Gate count(k)	50	250	520	230	200
Clock(MHz)	27	54, 81	54,65,75	10.76	10.76
Power(mW)	300	1500	3000	2500	500
Fab.	LGS	LGS	LGS	LGS	LGS
Technology	0.6u, TLM	0.6u, TLM	0.35u,TLM	0.6u, TLM	0.6u, TLM
Package	176 TQFP	240 HQFP	304 PQ2	160 PQ2	100 MQFP
Status	Q. S.	Q. S.	Revision	Q. S.	Q. S.

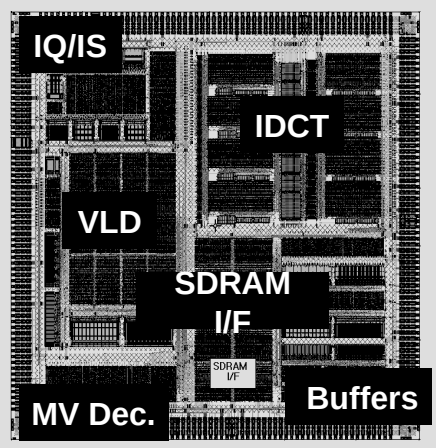
Implementation of 1st Gen. Chipset

Layout of 1st Gen Chipset

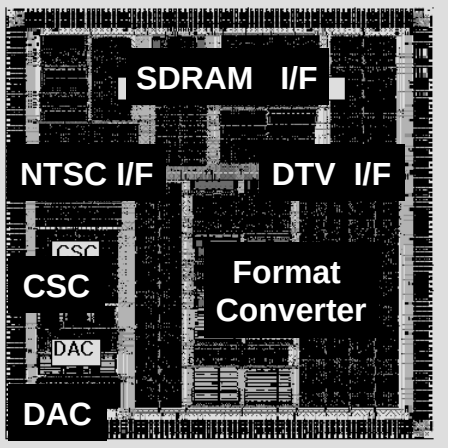
TP Demux



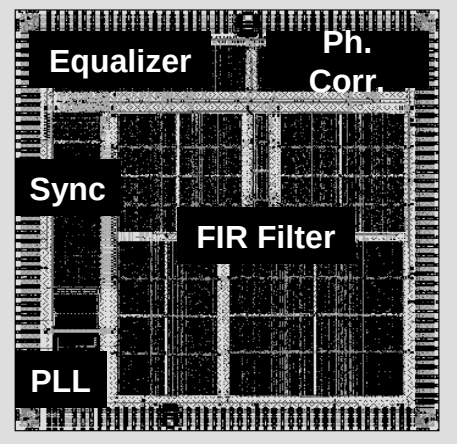
Video Decoder



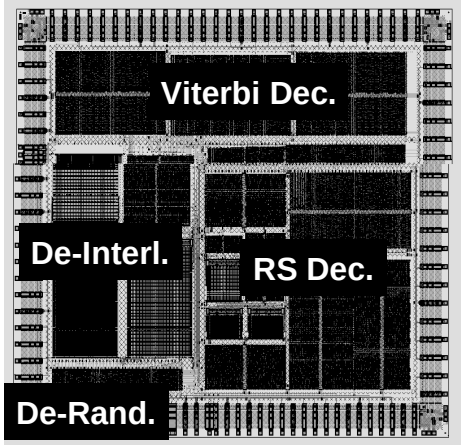
VDP



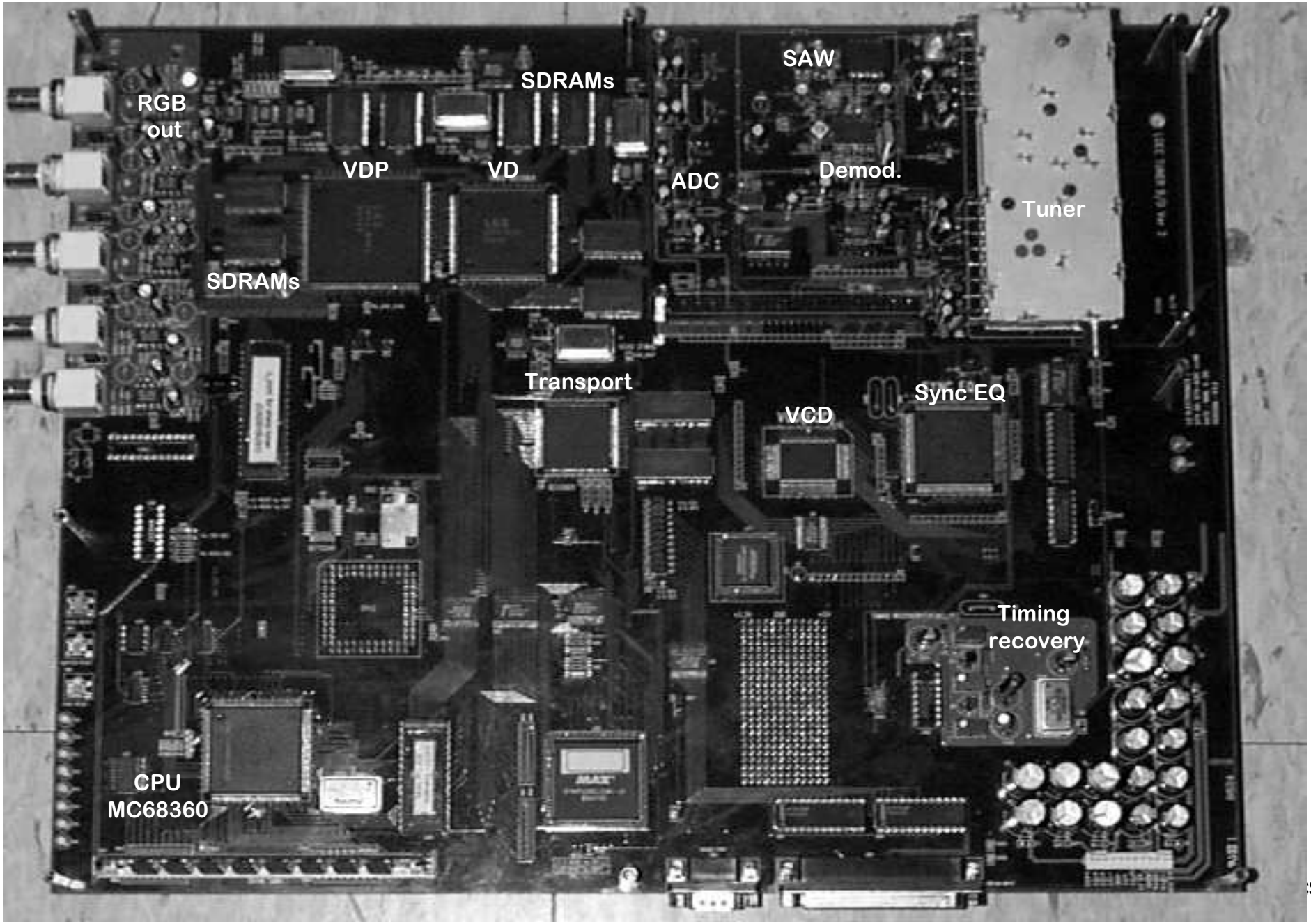
Sync/Eq



VCD



DTV Evaluation Board



Conclusions

- Implemented chipsets compliant with ATSC DTV transmission and video standard.
- Multiple system functions were included on chip to reduce ultimate system cost.
- Cost effective design using state-of-the-art ASIC technology is necessary to be supplied for consumer market.
- Overlapping and intensive design verification should be done to get successful chip functioning for large gate-sized chips.