

A Single-chip MPEG2 MP@ML Video Encoder LSI with Multi-chip Configuration for a Single-board MP@HL Encoder

T. Minami, T. Kondo, K. Nitta, K. Suguri, M. Ikeda,
T. Yoshitome, H. Watanabe, H. Iwasaki,
K. Ochiai, J. Naganuma, M. Endo, E. Yamagishi,
T. Takahashi, K. Tadaishi, Y. Tashiro,
N. Kobayashi, T. Okubo, T. Ogura and R. Kasai

Nippon Telegraph and Telephone Corporation

Outline

- Background
- Functionality of Video Encoder
- Key features
- Main architecture
- System configurations
- Chip specifications
- Summary

Trend of digital broadcasting

- MPEG2 International Standard in 1994
- Multi-channel digital broadcasting
 - United States in 1994
 - Europe in 1996
 - Japan in 1996
- HDTV digital broadcasting
 - United States in 1998
 - Europe in 1998
 - Japan after 2000

Background

Trend of MPEG2 video encoder LSI

- Three-chip MP@ML in 1995 (Mitsubishi)
- Two-chip SP@ML in 1995 (NTT)
- Single-chip SP@ML in 1997 (Phillips)
- Single-chip MP@ML in 1997 (NEC)
- Multi-chip MP@HL in 1997(C-Cube)
- Multi-chip MP@HL in 1998 (NTT)

Functionality of Video Encoder

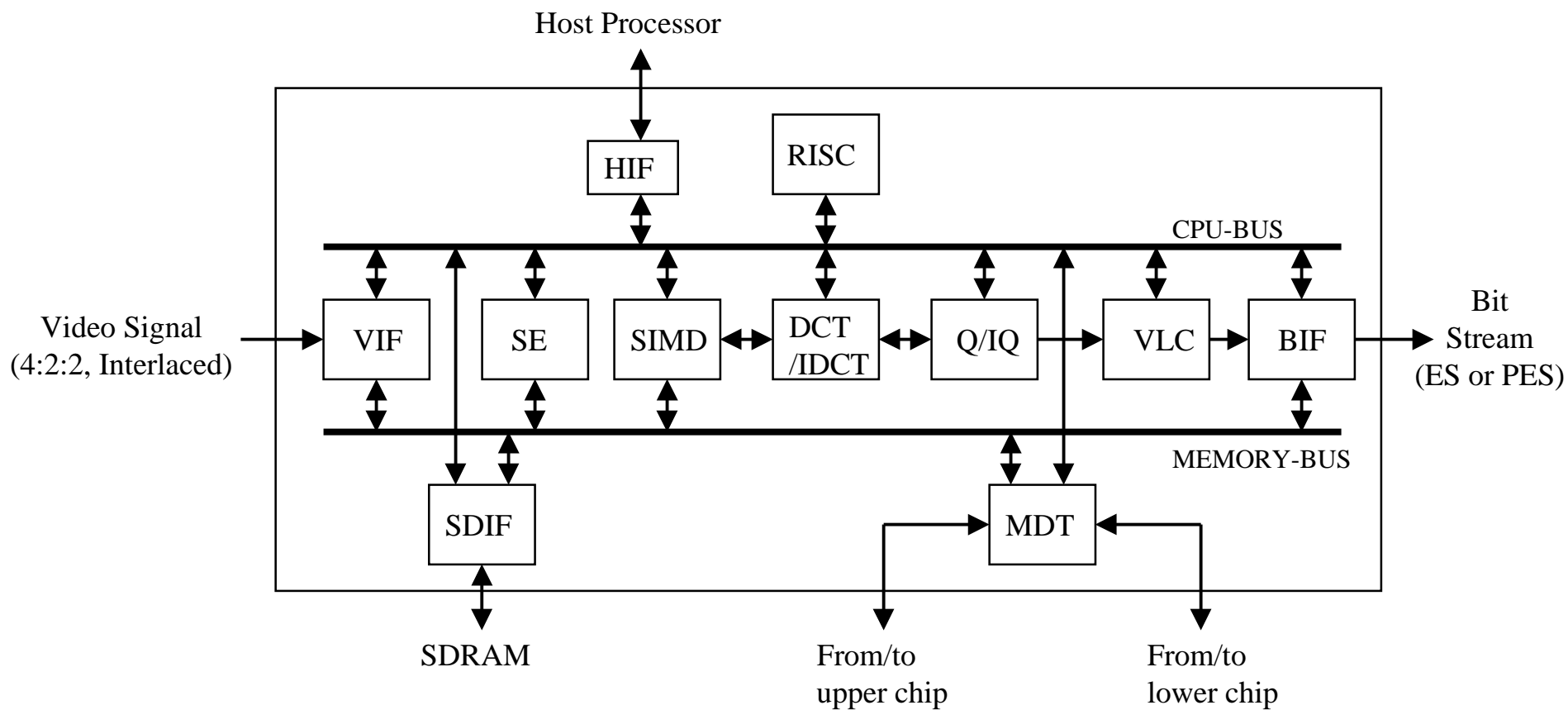
- Standard: SP@ML, MP@ML and 4:2:2Profile@ML with a single chip
MP@HL (4:2:0 or 4:2:2) with multiple chips
- GOP Structure: I, IP, IB, IBP, IBBP
- Frame Size: 720 x 480 (NTSC) or 720x 576 (PAL) with a single chip
max 2048 x 2048 with multiple chips
- Input: 4:2:2 Digital Component Signal (Interlaced)
- Output: Elementary Stream or Packetized Elementary Stream
MP@ML max 15 Mbps
MP@HL max 80 Mbps

Key features

- Inter- and intra-chip communication based on Flexible Communication Architecture (FCA)
 - Multi-chip MP@HL (4:2:0 or 4:2:2)
 - Improvement of a picture quality
- Wide-range motion estimation using hierarchical-telescopic and area-hopping search
- No peripherals except for SDRAM(s)

Main architecture

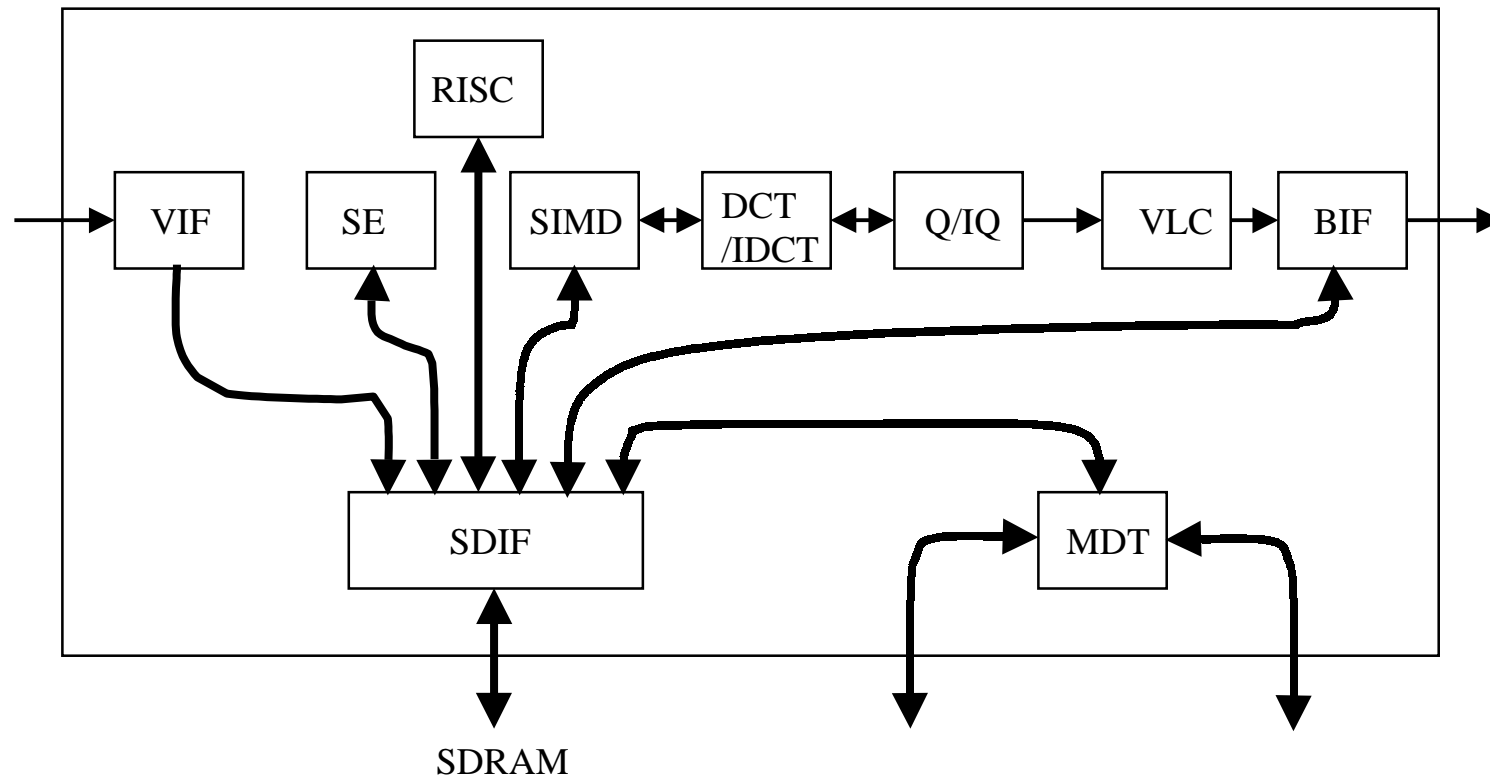
Block diagram



SE: Search Engine SIMD: Single Instruction Multiple Data stream processor
SDIF: SDRAM InterFace MDT: Multi-chip Data Transfer interface

Main architecture

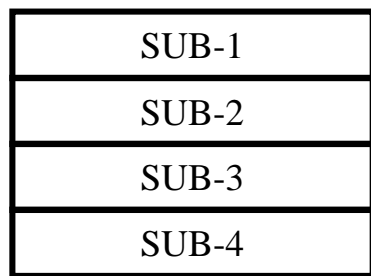
Flexible Communication Architecture (FCA)



Flexible data transfer via SDIF

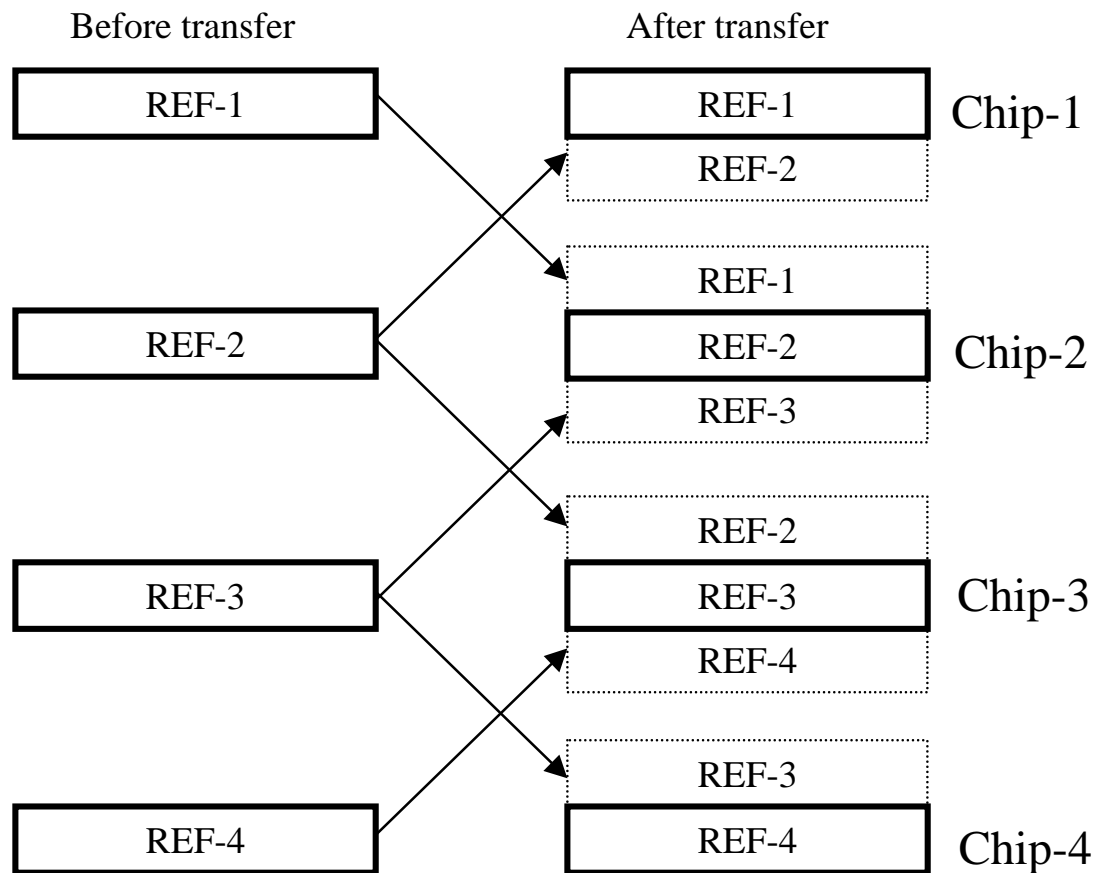
Main architecture

Inter-chip communication



SUB: Sub-picture
REF: Reference area

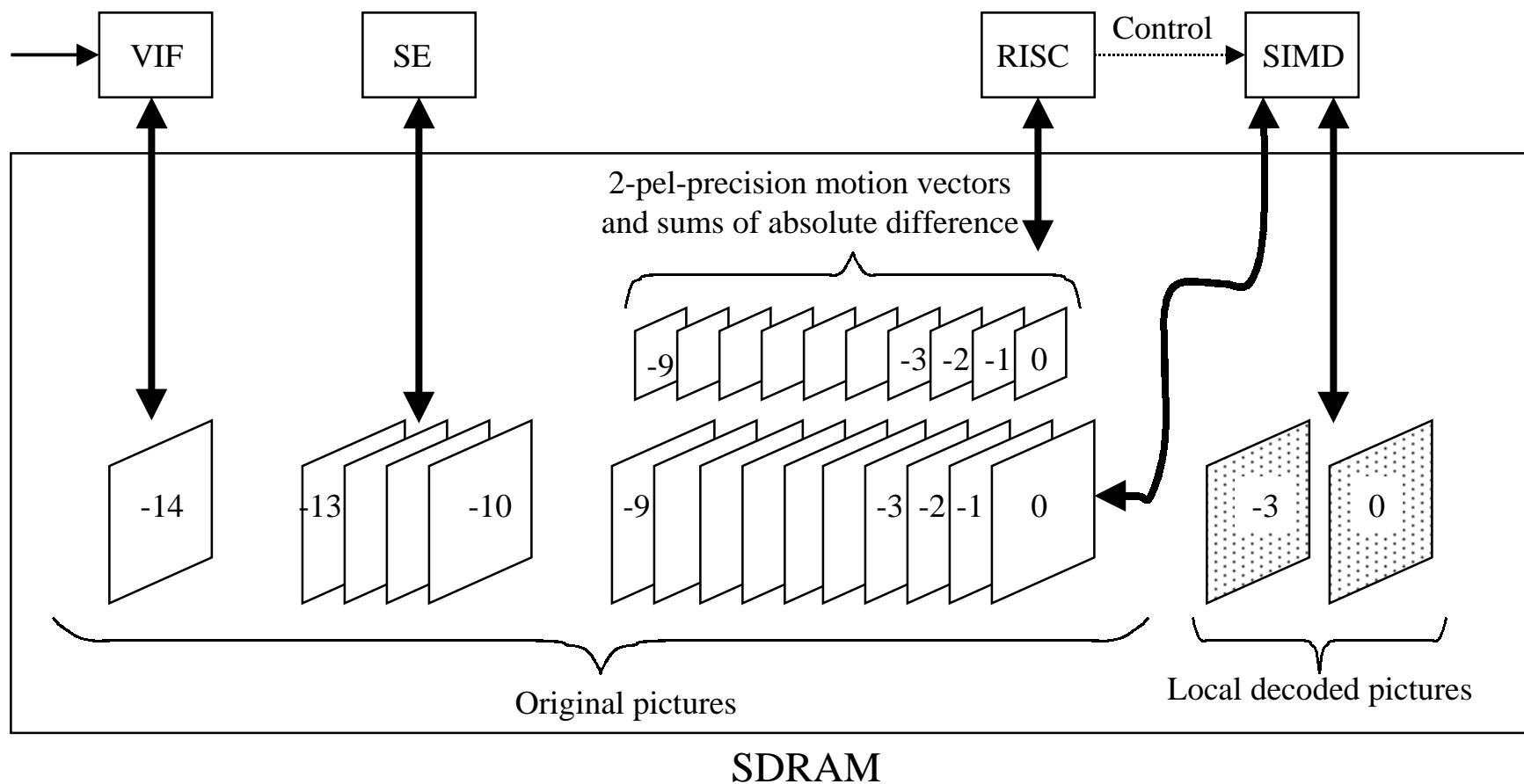
Horizontally split picture



Pixels transferred via MDT

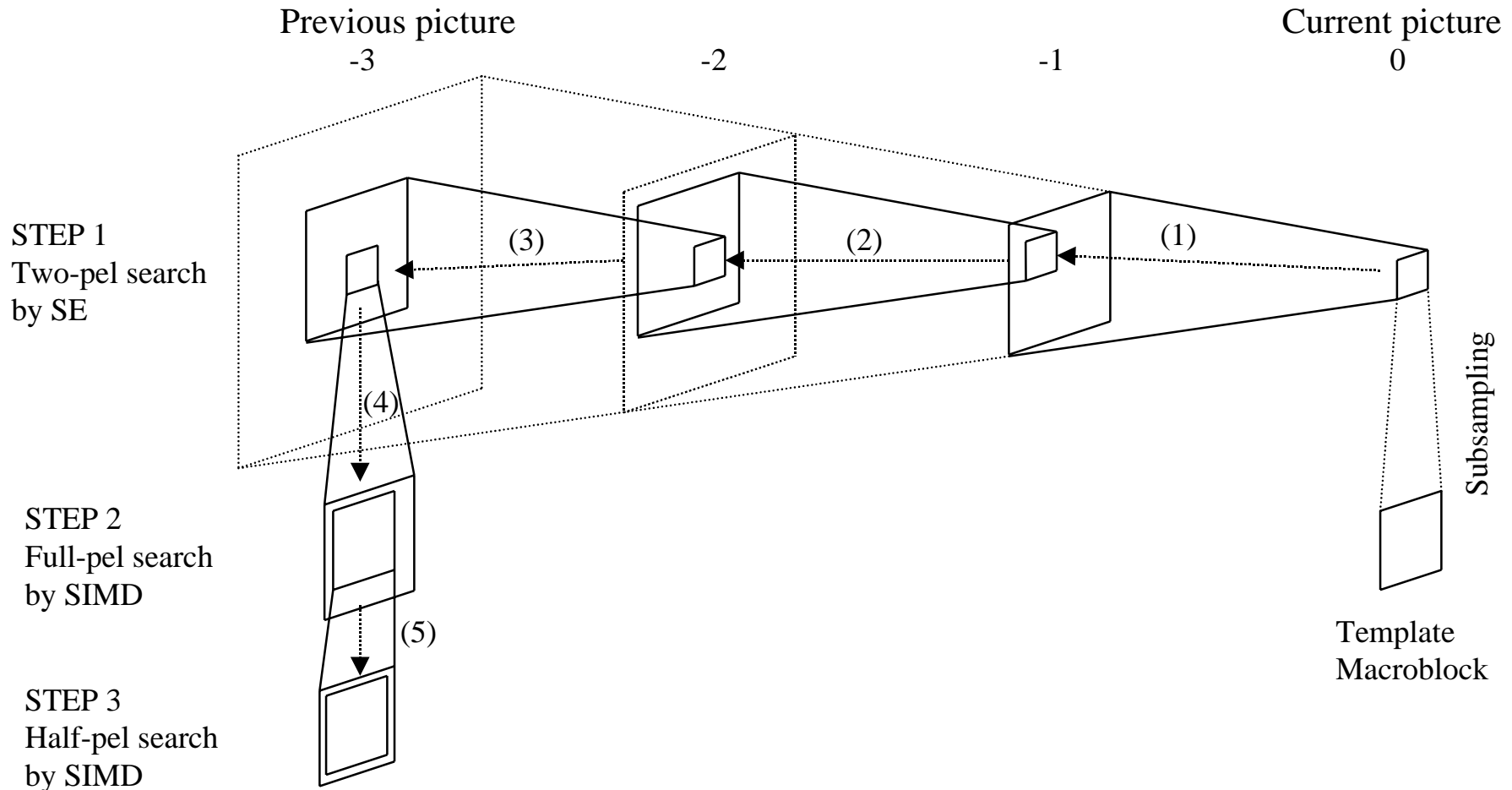
Main architecture

Intra-chip communication



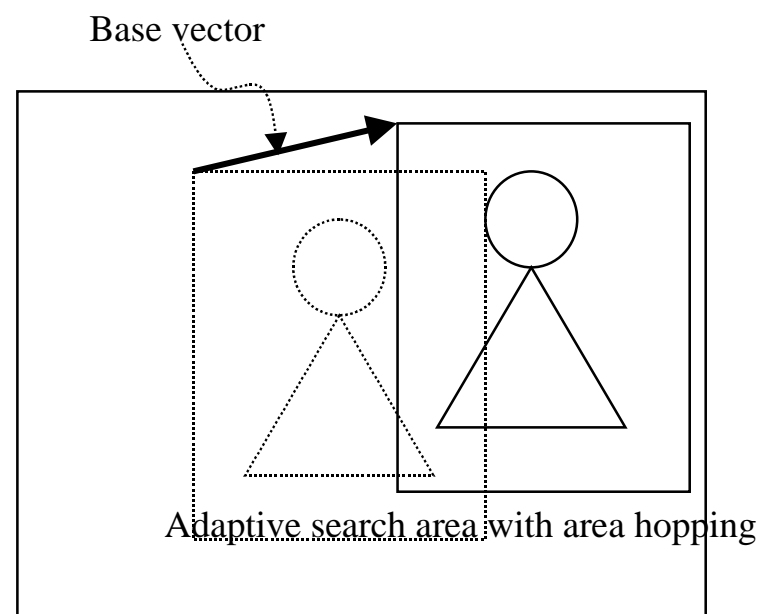
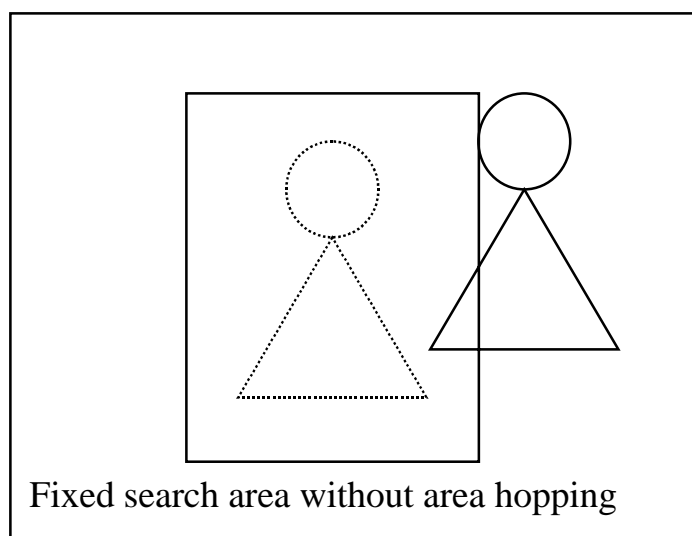
Main architecture

Hierarchical telescopic search



Main architecture

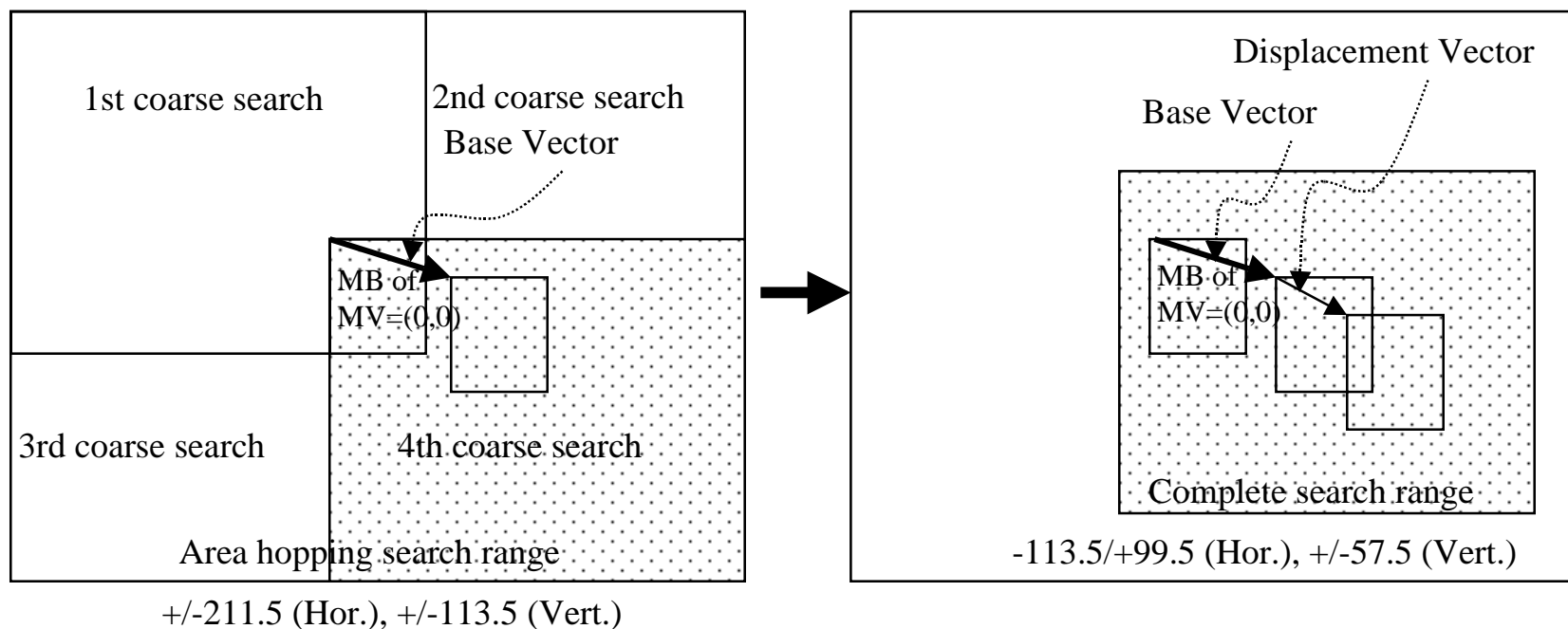
Area Hopping Search



- (1) Motion vectors in the same picture have spatial dependency.
- (2) A base vector is determined by analyzing part of the motion vectors on the current coded picture.

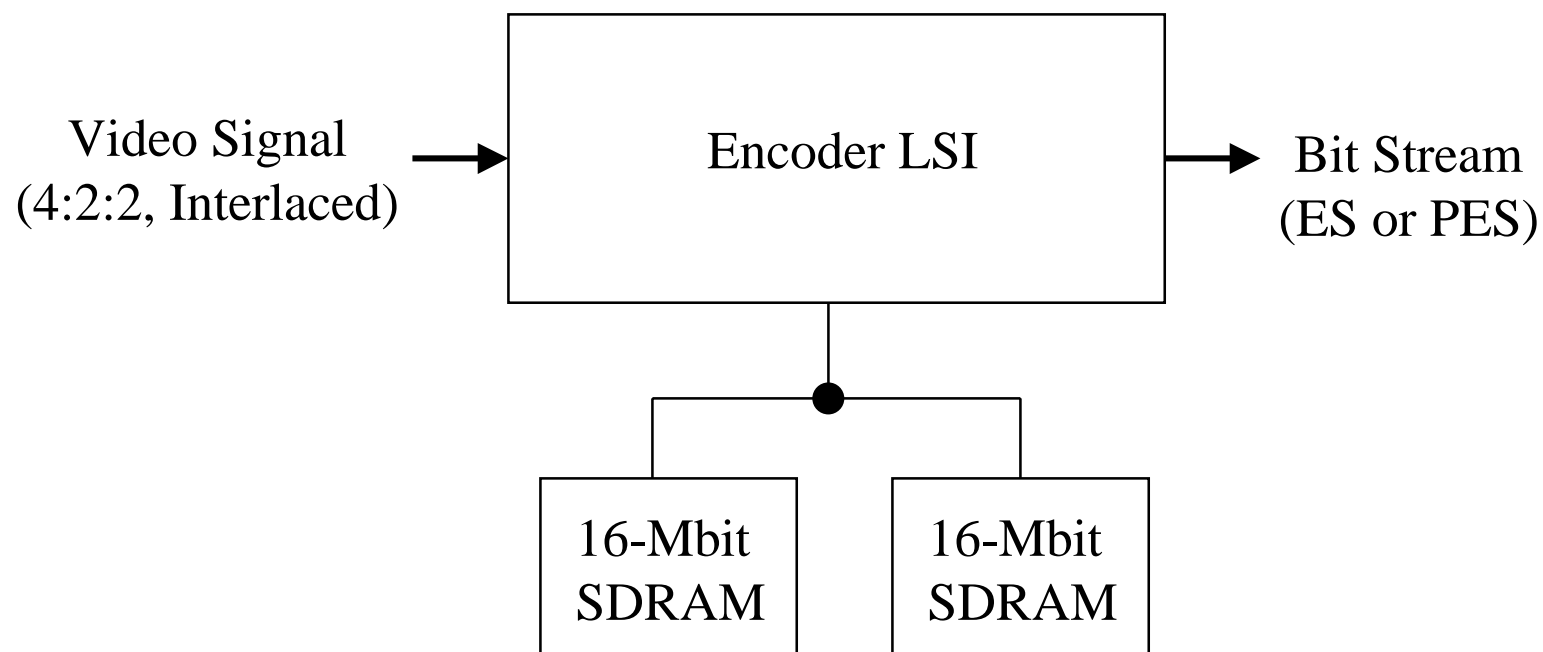
Main architecture

Area Hopping Search



System configurations

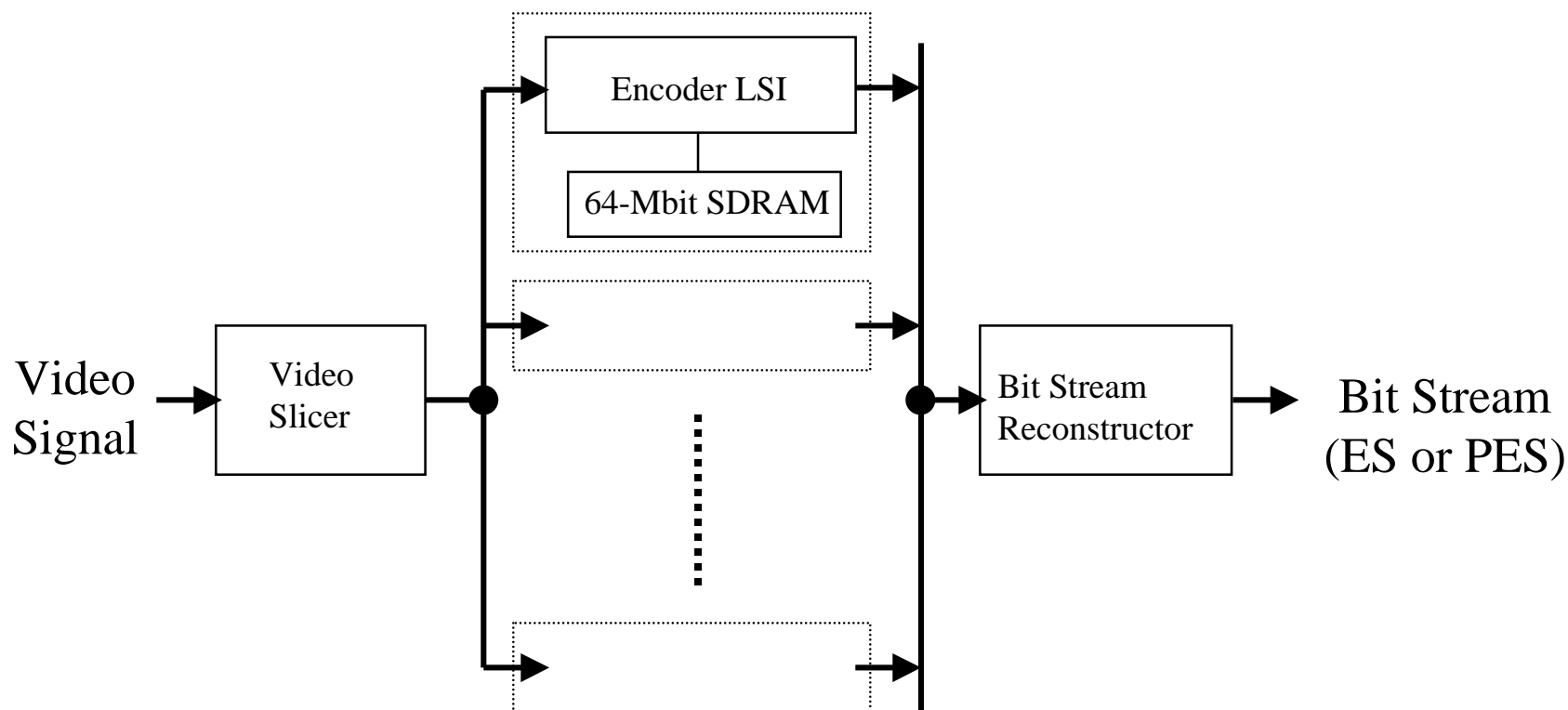
MP@ML encoder



A single-chip MP@ML encoder with only two 16-Mbit SDRAMs

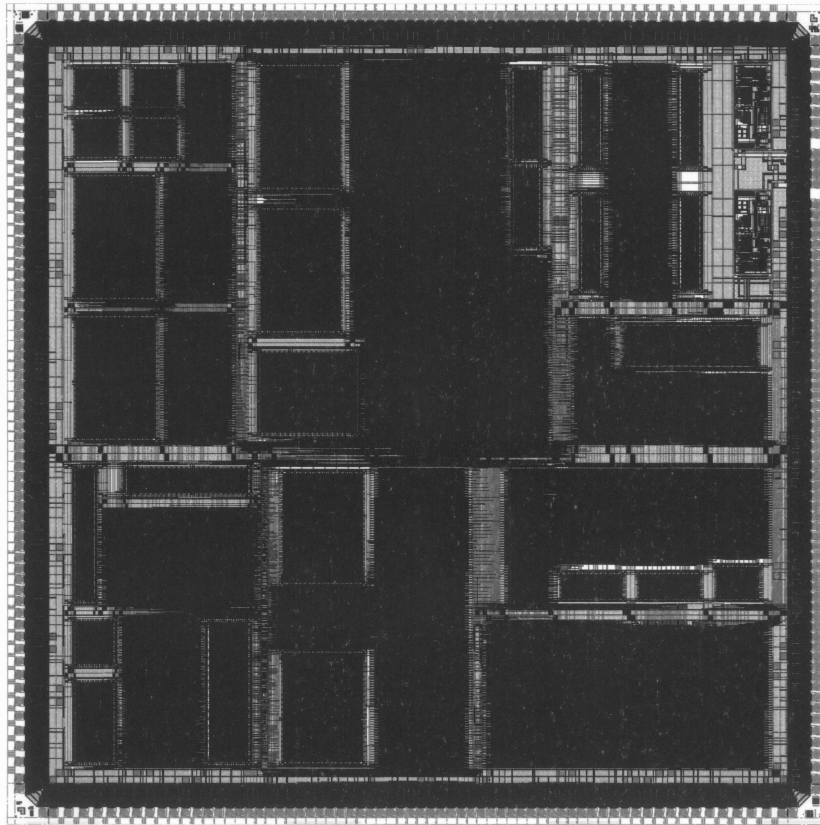
System configurations

MP@HL encoder



A single-board MP@HL encoder composed of multiple chips with a 64-Mbit SDRAM

Chip specifications



Layout pattern

- . 0.25-um 4-level metal CMOS
- . 5.0 million transistors
- . 10.0 x 10.0 mm² die size
- . 81-MHz clock
- . 2.5 V/3.3 V
- . < 2.0 W
- . 208-pin QFP
- . No hard macrocell
except for memories

Summary

- Flexible system configuration
 - Multi-chip MP@HL encoder (4:2:0 or 4:2:2)
 - Single-chip 4:2:2Profile@ML encoder
- Motion estimation using hierarchical-telescopic and area-hopping search
 - Non area-hopping $-113.5/+99.5$ (Hor.), ± 57.5 (vert.) for frame
 - Area-hopping ± 211.5 (Hor.), ± 113.5 (Vert.) for frame
 - Two-pel-precision search engine with only 32 processing elements
- No peripheral except for SDRAM(s)
 - 16-Mbit SDRAM x 2 or 64-Mbit SDRAM x 1