Genesis Microprocessor

Hot Chips X

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Presentation Outline

- Design Objectives
- Processor Features
- Micro-Architecture Overview
- Dual-Issue Superscalar Implementation
- Feature Comparison
- Summary

Design Objectives

- High Performance: 200+ MHz, 400 Dhrystone MIPS
- Efficient Memory: High Performance in Low Cost System
- Unique Features: DSP Functions & Image Processing
- Debug: System Debug Support
- Low Cost: 7mm x 7mm Die, Plastic Package
- Time To Market: 15 Months Development Time

Project Goal: Highest Performance in Its Class

Genesis Feature List

- ISA: MIPS-I through MIPS-IV, with
  Extensions to Support DSP & Vector Processing
- Pipeline: Symmetric Dual-Issue Superscalar
  - 2 Unified Integer-FP Units
  - Multiply-Accumulate Unit
  - 8 x 8-bit Packed-Data Vector Unit
  - Load-Store Unit
  - Branch Unit
- I-Cache: 32K-bytes, 2-way Set-Associative, Line Locking, LRU, Word Parity
- D-Cache: 32K-bytes, 2-way Set-Associative, Line Locking, LRU, Byte Parity,
  Write Back / Write Through
- MMU: 48 Double-entry Fully Associative TLB, with
  Separate 4-entry Micro TLB for Instruction & Data
- Sys Interface: R5000 Downward Compatible, with
  Features to Minimize Latency & Increase Throughput
- Debug: JTAG, N-Wire/N-Trace

Goals

- DSP & Image Processing Support

Extended Instructions

- MIPS-IV ISA, Plus Following Enhancements:
- 16 New Integer Multiply Accumulate Instructions
  - 32 x 32 Multiply with 64-bit Accumulate
  - 3 Cycle Latency, 1 Cycle Repeat Rate
- 32-bit and 64-bit Rotate Instructions
- 31 New Media Instructions
  - 8 x 8 bit Vector Instructions
  - Single 8 x 24-bit Vector Accumulator
  - Two or One Cycle Latency
  - 1 Cycle Repeat Rate for Most Instructions

Goals

- DSP & Image Processing Support
- Maintain Performance with an inexpensive memory system

Memory Latency Tolerance Features

- Large Caches
  - 32K I, 32K D
  - 2-Way
  - Per Line Locking
- Non-blocking Load/Store Unit
  - Up to 4 Data Prefetches
  - Up to 4 Non-blocking Loads or Stores
- Split Transaction System Interface
  - 4-entry Transaction Buffer
  - Up to 4 Outstanding Read Request
  - Interleaved Write Operations Between Read Request and Response

Goals

- DSP & Image Processing Support
- Maintain Performance with an inexpensive memory system
- Easy and Inexpensive System Debug to Decrease System Designer's Time to Market

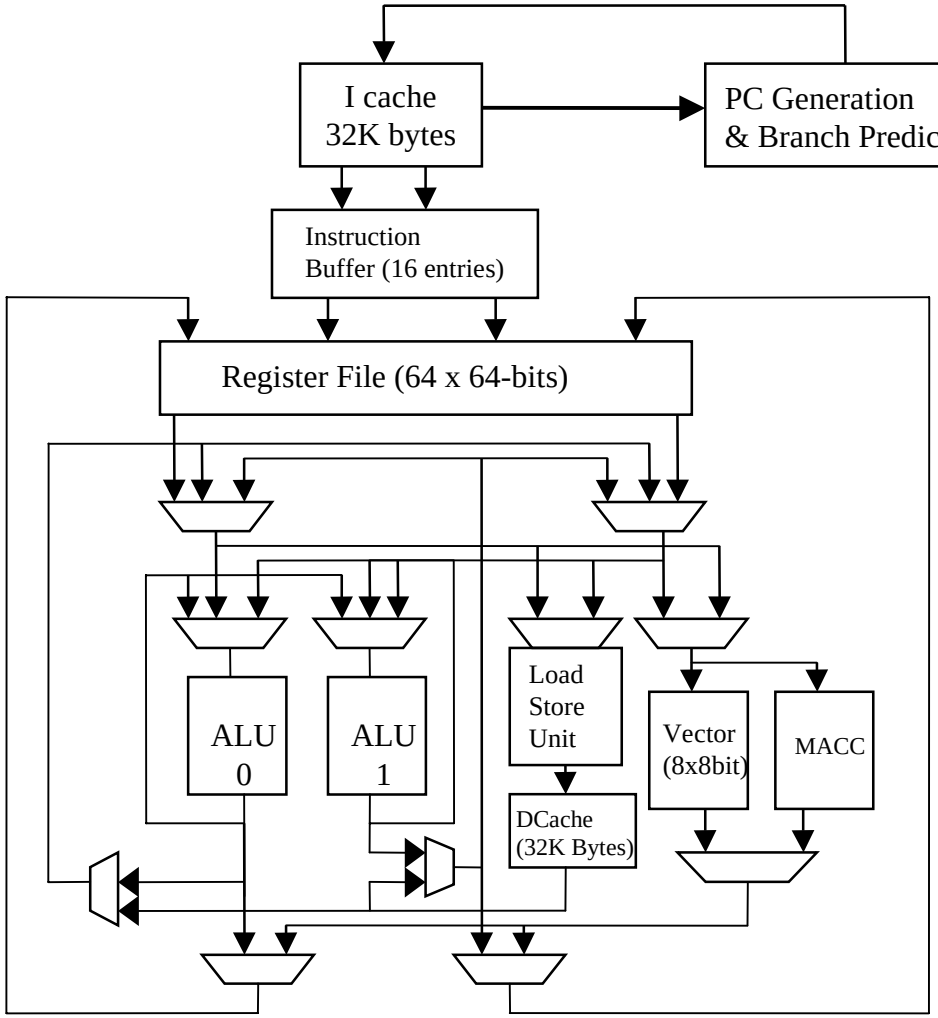
Debug Features

- Industry-standard Debug Support
- IEEE 1149.1 JTAG
- N-wire, N-trace
- Full External Access to:
  - Processor Architecture State
  - System Memory
- Multiple Breakpoints on:
  - Instruction Address
  - Data Address
  - Data Value
- Single-step Through Code
- Instruction Trace Capabilities and Performance Counters

Goals

- DSP & Image Processing Support
- Maintain Performance with an inexpensive memory system
- Easy and Inexpensive System Debug to Decrease System Designer's Time to Market
- Clean and Efficient Microarchitecture

Micro-Architecture Block Diagram



IC Stage

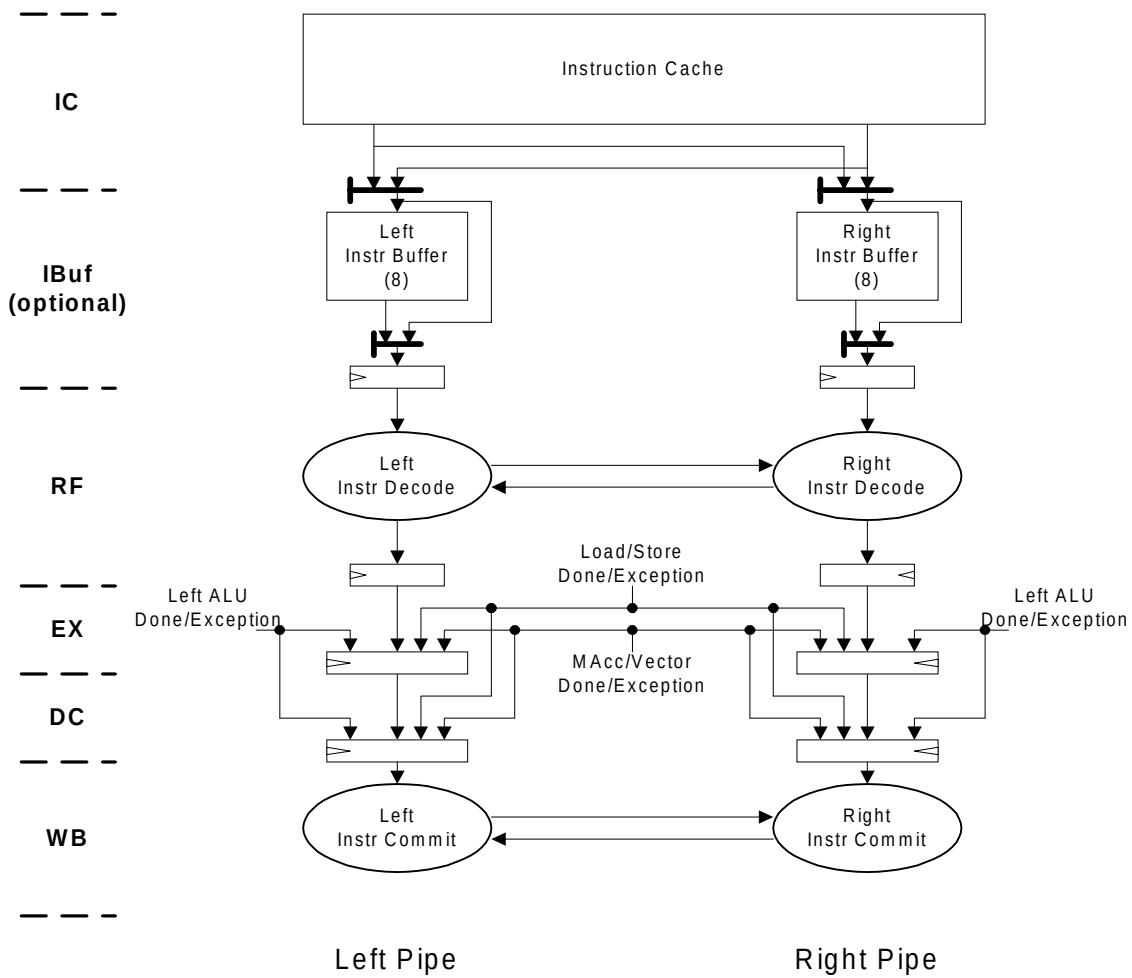
RF Stage

EX Stage

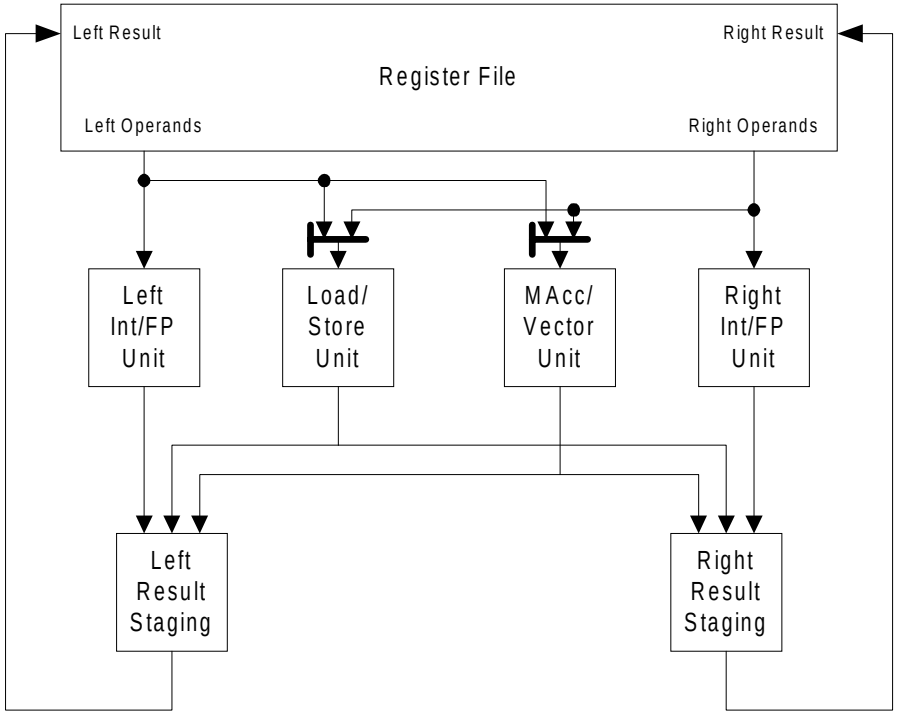
DC Stage

WB Stage

Instruction Pipeline



Data Pipeline



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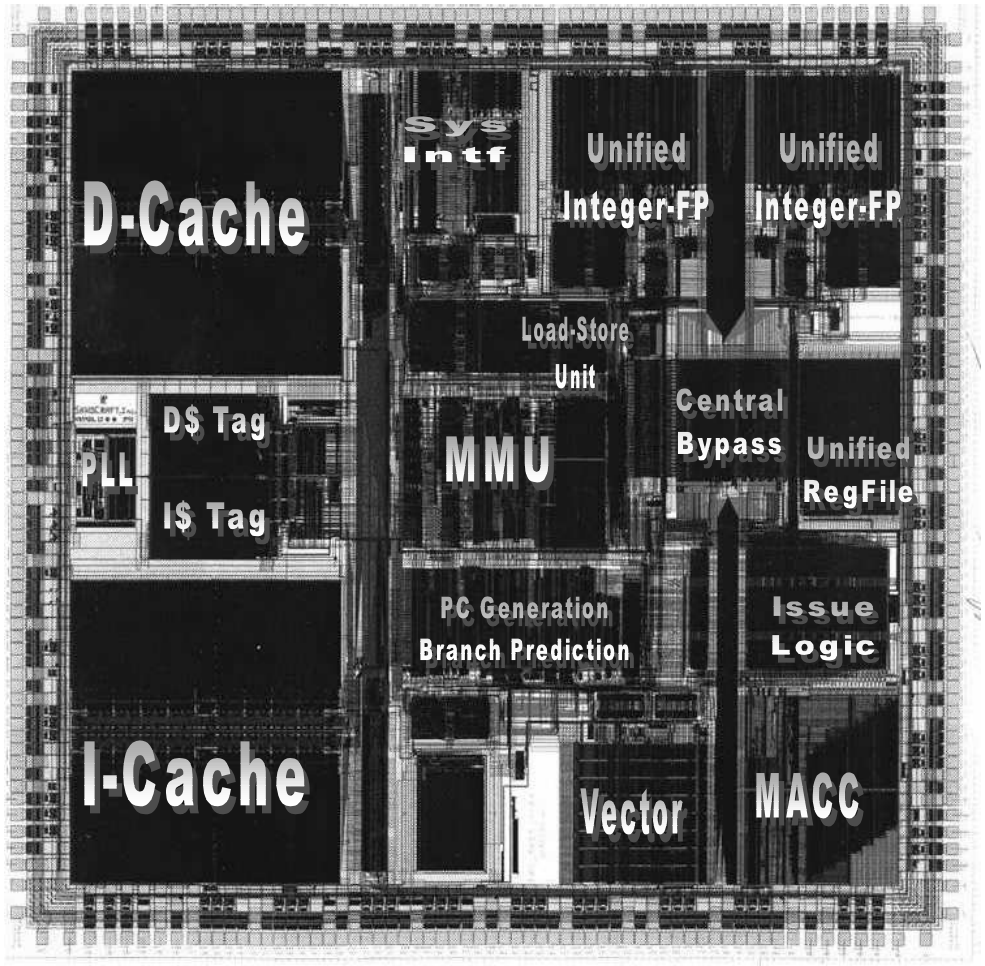

NEC VR5464™ Device Specification*

Process	0.25um, 3LM, 6-T SRAM cells
Frequency	250 MHz Pipeline, 100 MHz I/O
Performance	519 MIPS, 10 SPECint95, 4.5 SPECfp95
Die Size with scribe	47 mm^2
Voltage Supply	3.3-volt I / O, 2.5-volt Core
Power Consumption	4.4 watts
Package	272-pin plastic BGA
Price (10K)	$95

*Source: Microprocessor Report 3/9/98
TM -- trademark of NEC Electronics

Feature Comparison

	VR5464	VR5432	RM5270	RM5230	EC603e	SA-110	SH7750
Architecture	MIPS	MIPS	MIPS	MIPS	PowerPC	ARM	SuperH
Vendor	NEC	NEC	QED	QED	Motorola	Intel	Hitachi
IP Provider	SandCraft	SandCraft	QED	QED	Motorola	Digital	Hitachi
Frequency	**250 MHz**	**167 MHz**	200 MHz	175 MHz	266 MHz	233 MHz	200 Mhz
Execution Units	**6**	**6**	2	2	4	1	2
Issue/clock	**2**	**2**	1 Int, 1 FP	1 Int, 1 FP	2	1	2
FPU?	yes	yes	yes	yes	no	no	yes
Hardware MAC?	yes	yes	yes	yes	yes	yes	yes
Vector operations?	**yes**	**yes**	no	no	no	no	yes
Caches (I/D)	**32K / 32K**	**32K / 32K**	16K / 16K	16K / 16K	16K / 16K	16K / 16K	8K / 16K
Non-blocking Load/Stores	**yes**	**yes**	no	no	no	no	no
Cache locking?	yes (per line)	yes (per line)	yes (per set)	yes (per set)	no	no	no
Bus width	64 bits	64 bits	64 bits	32 bits	64 bits	32 bits	64 bits
IEEE 1149.1 JTAG support?	yes	yes	yes	yes	yes	yes	?
Debug support?	**yes**	**yes**	no	no	no	no	no
Fab process / Metal Layers	0.25um / 3LM	0.25um / 3LM	0.35um / 3LM	0.35um / 3LM	0.35um / 4LM	0.35um / 3LM	0.25um
Die Size	47 mm^2	47 mm^2	84 mm^2	84 mm^2	98 mm^2	50 mm^2	58 mm^2
Voltage (V)	2.5 / 3.3	2.5 / 3.3	3.3V	3.3	2.5 / 3.3	1.65 / 3.3	1.8 / 3.3
Power (typical)	4.4W	2.5W	4.0W	3.6W	4.8 W	1.1W	1.5W
Dhrystone MIPS	519	347	260	227	376	268	360
MIPS/MHz	2.1	2.1	1.3	1.3	1.4	1.2	1.8
SPECint95	10 (est.)	n/a	5.5	4	6.7	n/a	n/a
SPECfp95	4.5 (est.)	n/a	6.1	4.2	n/a	n/a	n/a
Price (10K) - MPR 3/9/98	**$95**	**$45**	$75	$35	$81	$49	$40

Conclusion

Project Goals Emphasized:

- Design Efficiency and High Execution Throughput
  - ⇒ De-coupled Instruction Fetch and Execution Datapaths
  - ⇒ Symmetric Dual Pipelines
  - ⇒ DSP & Image Processing Extensions
- Low Cost without Sacrificing Performance
  - ⇒ Efficient Memory
  - ⇒ Clean Superscalar implementation
  - ⇒ Inexpensive Processor
  - ⇒ Debug Support for Faster System Design
- Making a Clean Design to Achieve the Shortest Development Time
  - ⇒ From Specification to Tapeout in 15-1/2 Months

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