TriTech Microelectronics

Pyramid3D™

Pyramid3D™
Real-time Graphics Processor

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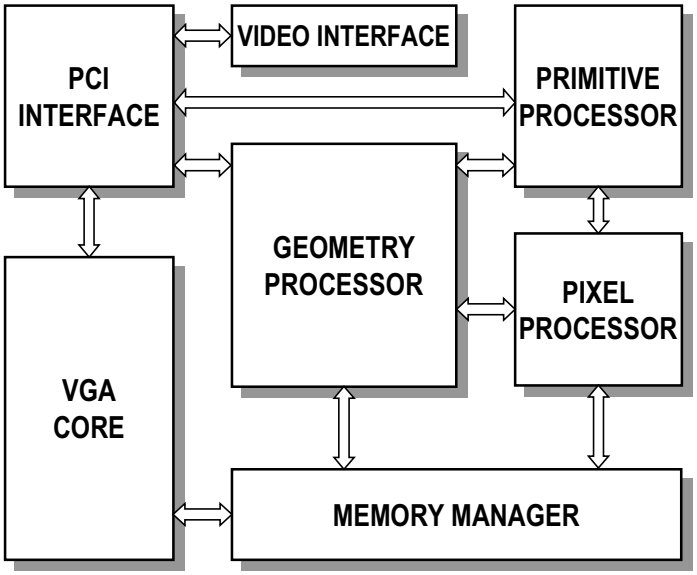
Pyramid3D™

Overview

- System architecture
- Geometry Processor
- Primitive Processor
- Pixel Processor
- Other features
- Performance

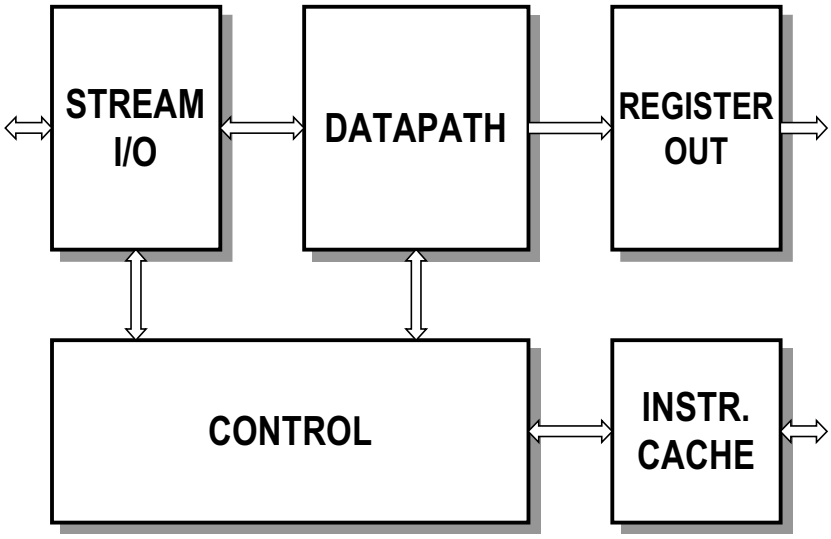
Pyramid3D System Architecture



Geometry Processor

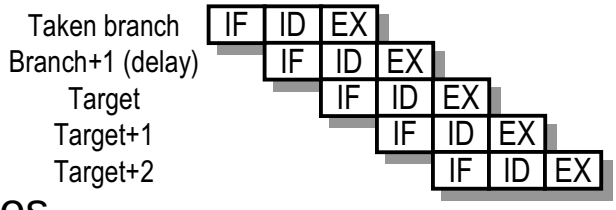
- 3-issue VLIW architecture
- 32-bit fixed point vector datapath
  - Block floating point support
- Hardware division unit
- Integrated data memory
  - 3 ×128 words 2-port SRAM
- Instruction cache
  - 4-way set associative
  - 4 × 128 word blocks

GP — Architecture

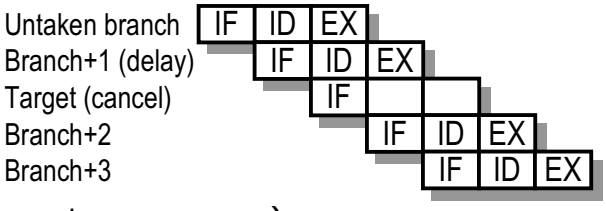


GP — Pipeline Model

- Fetch – Decode – Execute
  - Delayed branches



- Speculative branches



- No interrupts
  - 3 wait sources (cache, stream, user)
  - Use polling to synchronize

GP — Instruction Set

- Compacted VLIW instructions
  - Compaction based on code analysis
- 32-bit fixed instruction size
- 20 combinations of basic instructions

Basic Instruction Classes	
ALU	Control
Move	Stream
Branch	3D Init
Logic	Other

GP — Instruction Set [cont.]

- Indexed memory access
  - 6 index registers
  - 4 bit offset
  - 16 word zero page direct access
- Absolute branch addresses
  - 14 -bit address space
  - Configurable mapping in RAM on graphics card

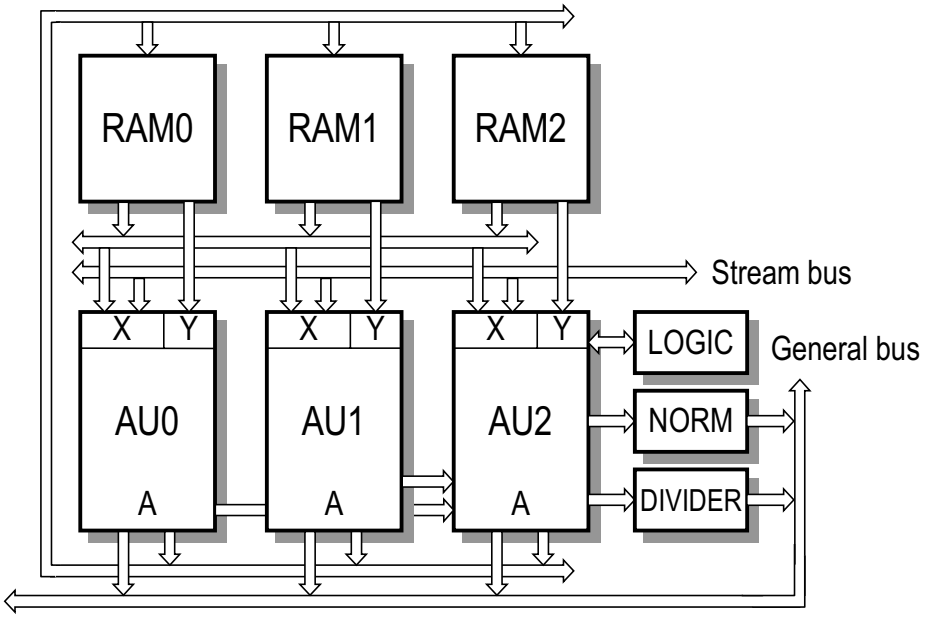
GP — Instruction Set [cont.]

3D transform of point (**x1⇒y1**) by P(**p0,p1,p2,p3**)

```
YRDBASE=Base(x1)                          Load base of x1 and y1
N=-24                                     Fixed point format
```

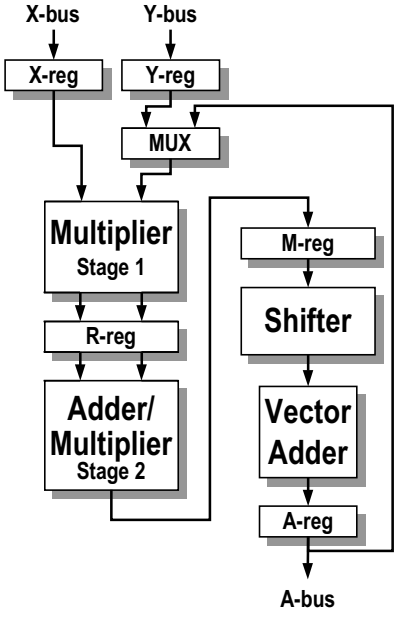
```
1  X=RAM(p1), Y=RAM(x1)
2  X=RAM(p2),            R=hi(X*Y)
3  X=RAM(p3),            R=hi(X*Y), M=R
4             Y=RAM(p0), R=hi(X*Y), M=R, A=shift(M0+M1+M2)
5  X0=A2,                           M=R, A=shift(M0+M1+M2)
6  X1=A2,                                A=shift(M0+M1+M2)
7  X2=A2
8                                        A=X+Y
9             RAM(y1)=A
```


GP — Datapath Architecture



GP — Arithmetic Unit

- 32 bit fixed point datapath
- $24 \times 24 \Rightarrow 56$ bit multiplier
  - Modified booth encoded Wallace tree
- 56 bit adder
  - Used for multiplier final adder
  - 2-level carry skip architecture
- $56 \Rightarrow 32$ bit shifter
  - Format select for multiplier
- 32 bit 3-element vector adder
  - AU2 only
- Variable 1 to 3 cycle latency
  - User visible pipeline registers
  - Pass-thrus for simple operations



GP — Other Datapath Features

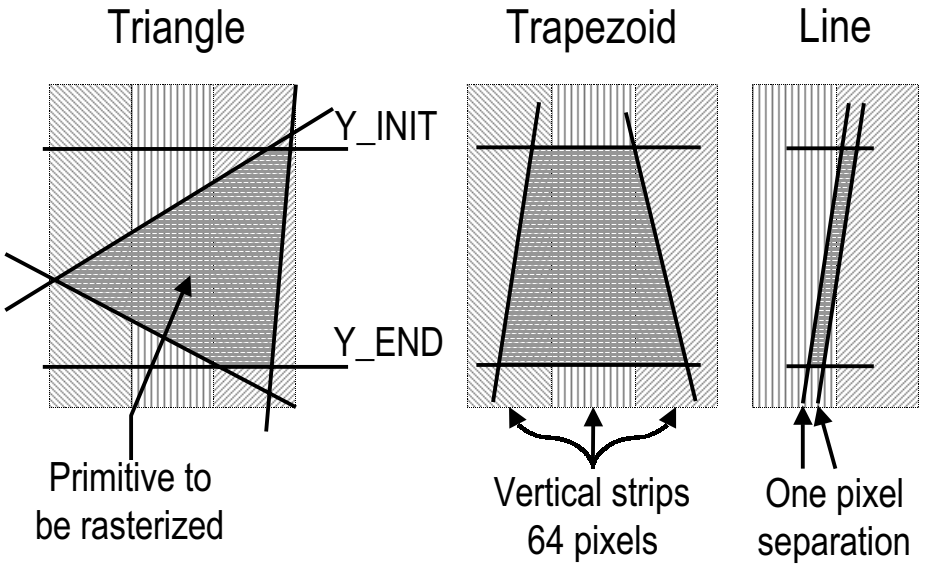
- Hardware division
  - Radix-4 iterative algorithm
  - 24 and 32 bit formats
  - Quotient and remainder available
- Normalization unit
  - Used for block floating point support
- Logic unit
  - Normal logic operations
  - Bit-field operations

Primitive Processor

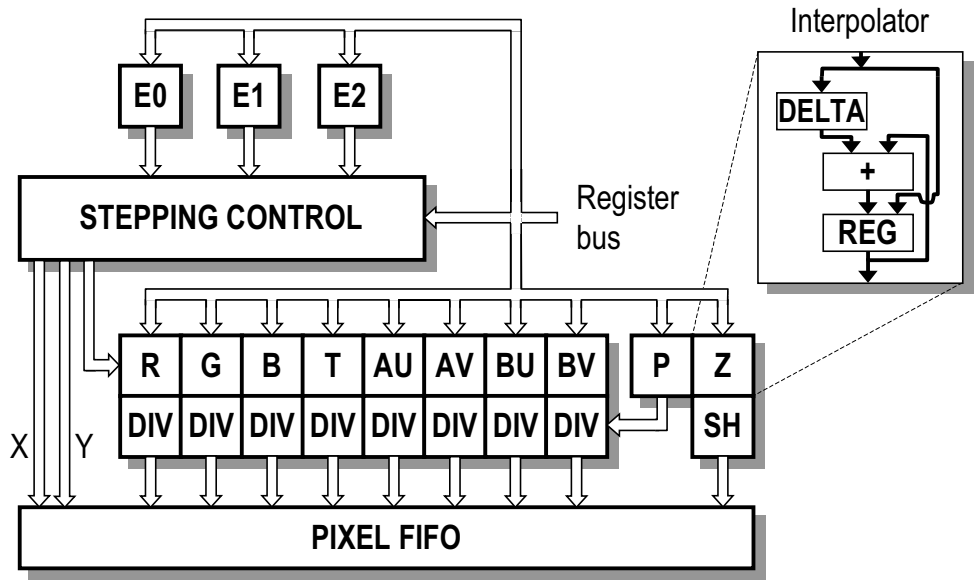
- Converts graphics primitives into pixels
- 15 interpolators
- 8 dividers
  - Perspective correct rendering

Interpolator	Correction	Stored to FIFO
Red, Green, Blue	perspective	yes, 8 bits
Transparency	perspective	yes, 8 bits
A Texture U, V	perspective	yes, 12 bits
B Texture U, V	perspective	yes, 12 bits
Z Depth	linear	yes, 24 bits
Perspective P	linear	no
X, Y Coordinates	linear	yes, 22+4 bits total
3 Edge Functions	linear	no

Supported Graphics Primitives



Primitive Processor Architecture



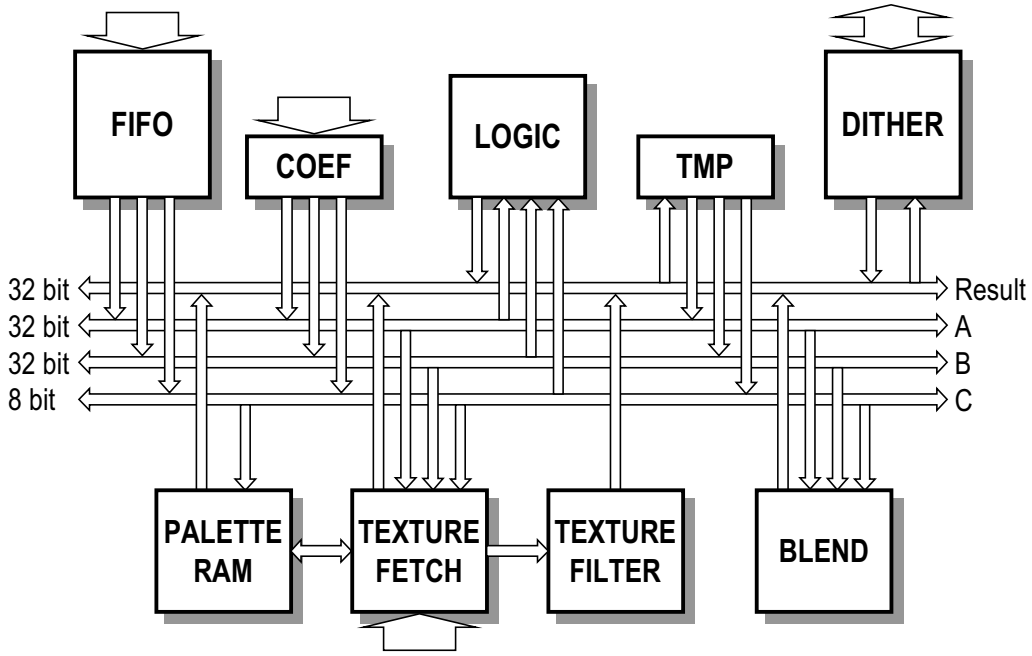
Primitive Processor Features

- Hardwired unit
  - Fixed operations on user data
- Two FIFO's for load balancing
  - Each FIFO 64 130-bit words
- Primitives defined by 3 edge functions
- Operates on vertical strips
  - Better performance due to locality of RAM references

Pixel Processor

- Dual parallel units
- Programmable vector processor
  - Up to 32 instruction shading program
  - Conditional execution ⇒ variable latency
- 4 central buses
  - A, B, and Result 32 bits
  - C 8 bits
- Operations
  - Z-buffer read+compare, write
  - Frame buffer read, write
  - Texture fetch, filter
  - Blend, logic, bump mapping

Pixel Processor Architecture



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Pixel Processor Features

- Operates on 32 pixel groups with two units
  - 32 and 16 bit pixel formats
- Variable processing time for each pixel
  - Extra speed from early pixel elimination
- Dithering for better 16-bit quality
  - Uses 4-by-4 ordered dithering
- Environment mapping support
  - Dual textures in single rendering pass
- Bump mapping support
  - Uses two textures to calculate bump effects

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Pyramid3D™

SVGA Core and Video Interface

- Integrated with PCI interface
- Full implementation of VGA standard
- Integrated PixBLT engine
- High performance
  - Up to 1600 × 1200 @ 70Hz Displays
  - 80MB/s linear framebuffer access
- Integrated clock synthesizers
- Integrated 200MHz DAC

Memory Manager

- Utilizes single memory space for all data
- Supports 2–32 MB memory with
  - SDRAM
  - SGRAM
  - DRAM (EDO, FPM)
- PCI bypass directly to memory on card

Performance

- 1.3 million 16bpp shaded 25 pixel triangles/s
- 1 million 16bpp shaded, Z-buffered triangles/s
- Maximum pixel fill rate 50 million pixels/s
- GP full triangle init 550k triangles/s
  - Initializes all the parameters
- Up to 10 million triangles/s with multiple chips
  - Need extra hardware to combine results

Physical Characteristics

- 304 pin 31mm MBGA package
- Initial design (sampling 3Q97)
  - 100 MHz clock frequency
  - 0.6 µm 3 layer metal process
  - 13 × 13 mm^2 area (est.)
- Production version (1Q98)
  - 160 MHz clock frequency
  - 0.35 µm 4 layer metal process
  - 8.6 × 8.6 mm^2 area (est.)

Summary

- Single-chip 3D graphics solution
  - Geometry Processor
  - Primitive Processor
  - Pixel Processor
  - SVGA
- Multiprocessor architecture
- >1M triangles/s performance
- High quality rendering