The VelociTI™ Architecture of the TMS320C6xxx

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Loc Truong

DSP Applications Manager

Agenda

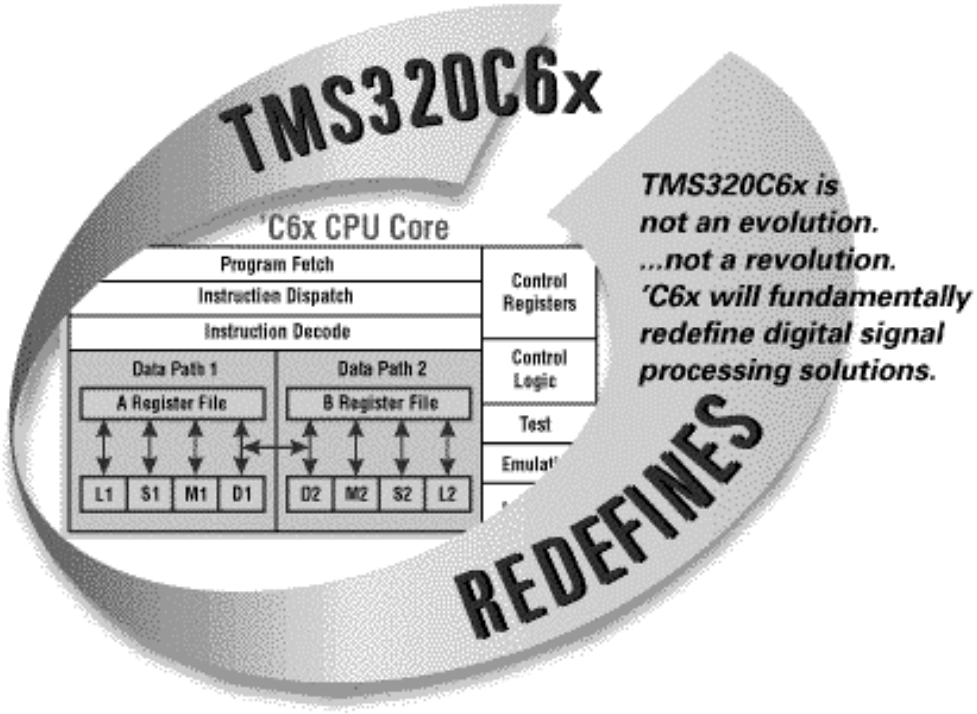
- Motivation for Quantum Leap in DSP Performance
- The VelociTI™ Advanced VLIW Architecture
- VelociTI ™ Pushes New Levels of DSP Performance
- Advanced Development Tools
- State-of-the-Art Process Technology

Motivation For Quantum Leap in Programmable DSP Performance

- Emerging demands for **mainstream applications** of *massively parallel, uniform DSP processing* in wireless or wireline communications
- Economic and engineering necessity to **reduce** system size and power consumption
- Rapid improvements in DSP algorithms, quickly evolving standards and shorter time-to-market

⇨ **VelociTI™** Advanced VLIW architecture opens up unlimited possibilities for *high-performance multi-channel, multi-function applications* by delivering 10x performance over existing Digital Signal Processors

The VelociTI™ Advanced VLIW Architecture



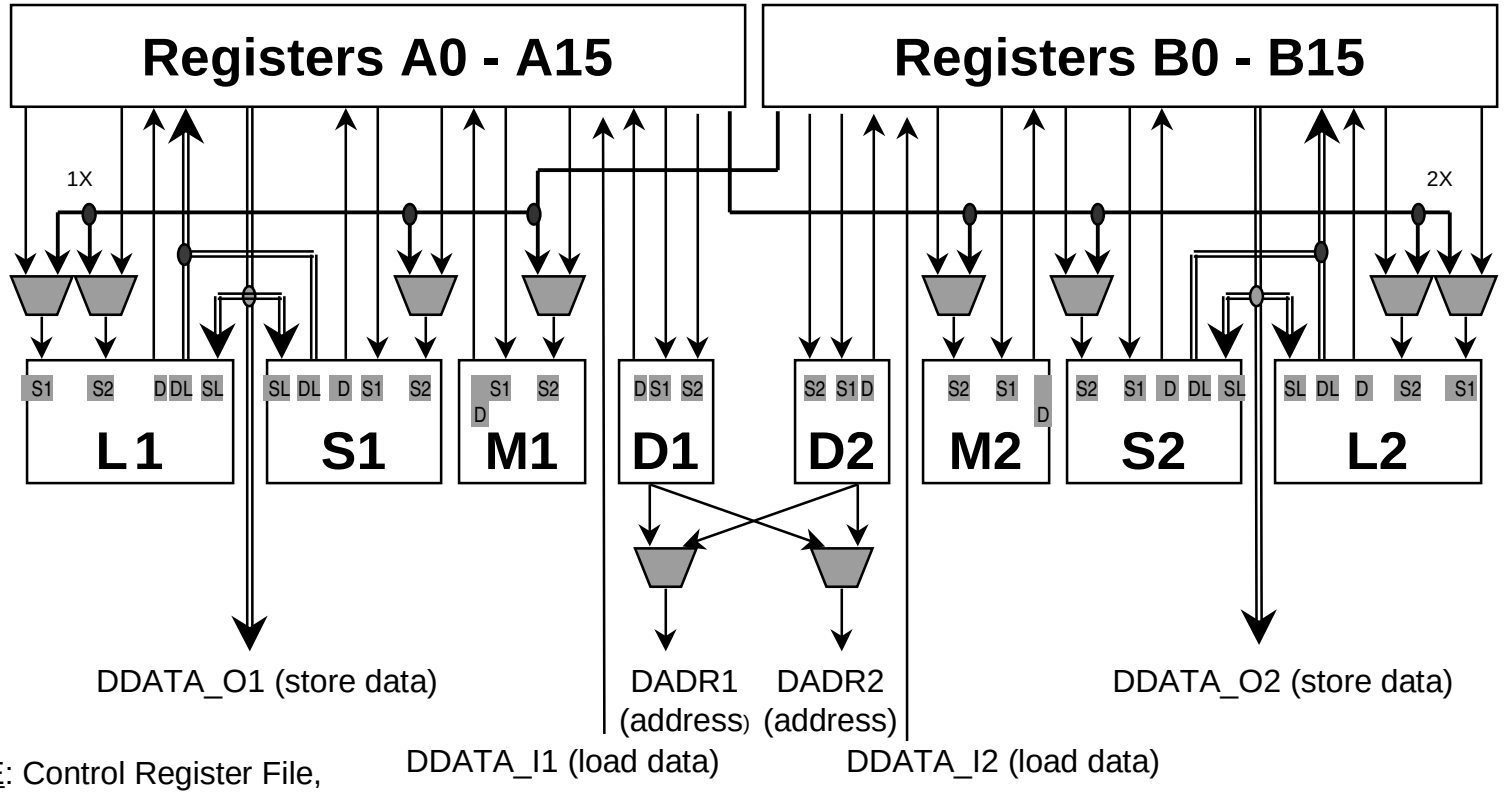
VelociTI™ Advanced VLIW Architecture

Why VLIW?

- VLIW lends well to DSP algorithms and offers possibilities for very high performance
- VelociTI™ capitalizes on VLIW strengths while addressing its shortcomings with:
  - high silicon densities to improve speed paths through functional units
  - architectural innovations: flexible addressing modes, intelligent memory and peripheral support, flexible instruction packing and critical-path pipelining schemes
  - compiler-friendly: orthogonal, deterministic, 100% conditional RISC-like instruction set
  - advanced compiler and optimization technologies

VelociTI™ Advanced VLIW Architecture

Core Block Diagram

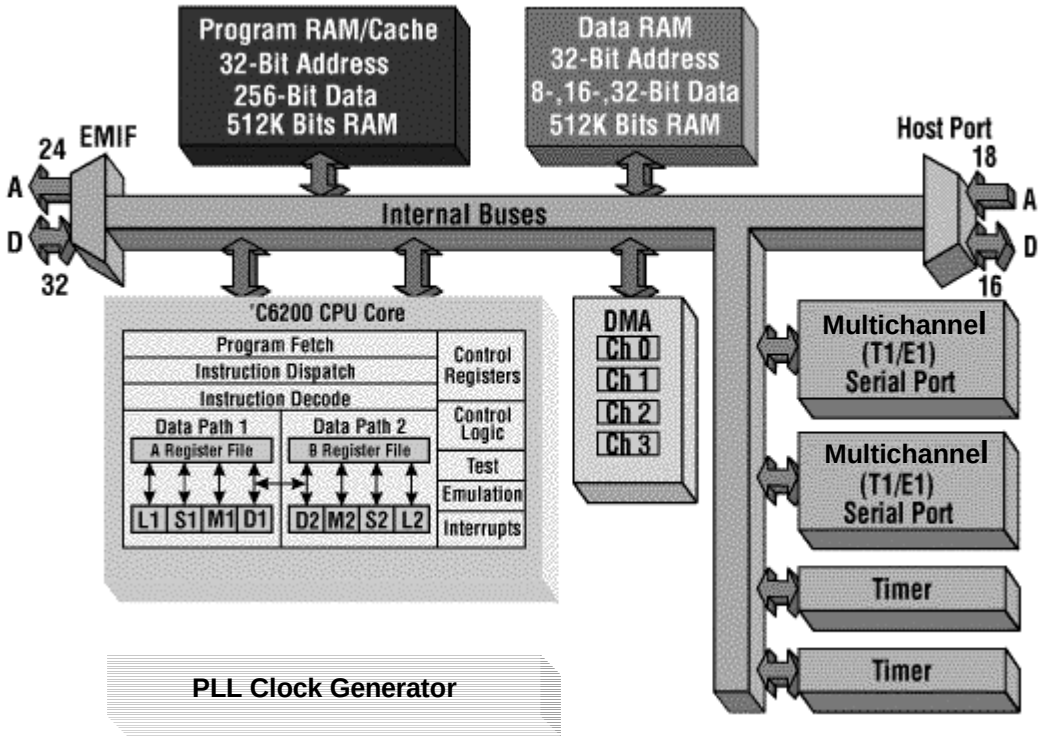


NOTE: Control Register File, Pipeline, Interrupt Processing, Power Management and Emulation & Test Logic Blocks Are Not Shown.

Cross Paths
40-bit Write Paths (8 MSBs)
40-bit Read Paths/Store Paths

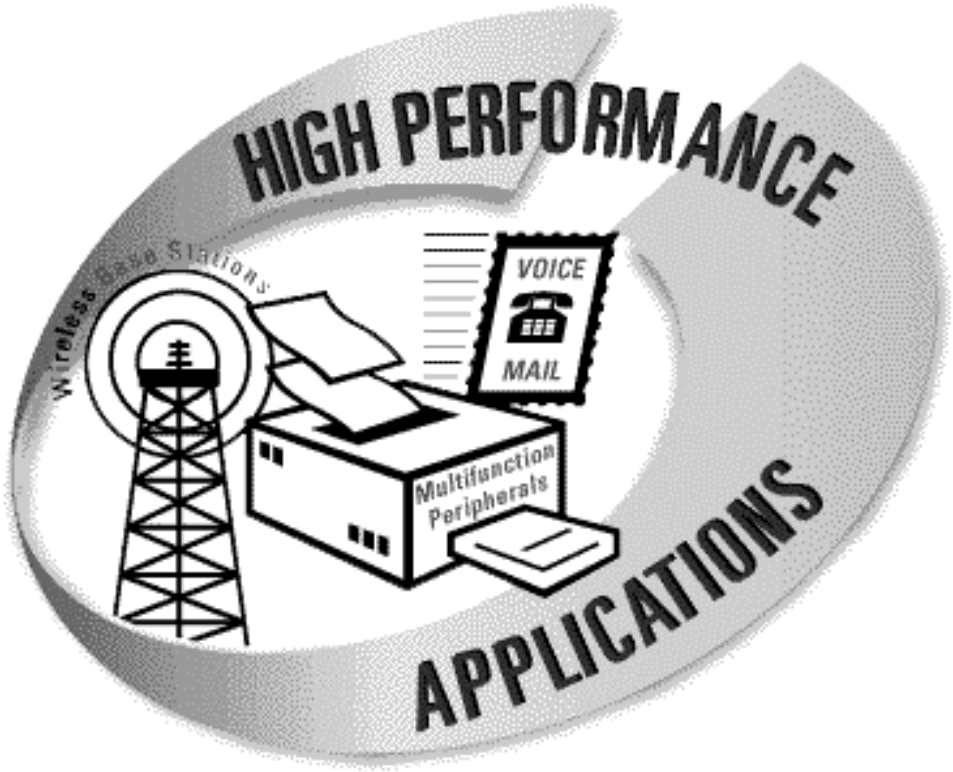
VelociTI™ Advanced VLIW Architecture

First Offering: TMS320c6201



- 1,600 MIPS @200-MHz
- 5 ns internal cycle time
- Up to eight 32-bit instructions per cycle
- 3.3V I/O, 2.5V Internal
- 0.25 micron, 5-layer metal
- One Megabit On-Chip RAM
- SRAM, SB-SRAM, SDRAM Interface
- Four-Channel DMA
- Two MultiChannel T1/E1 Serial Ports
- 16-bit DMA Host Port
- 352-pin BGA

VelociTI™ Pushes New Levels of DSP Performance



VelociTI™ - New Levels of DSP Performance

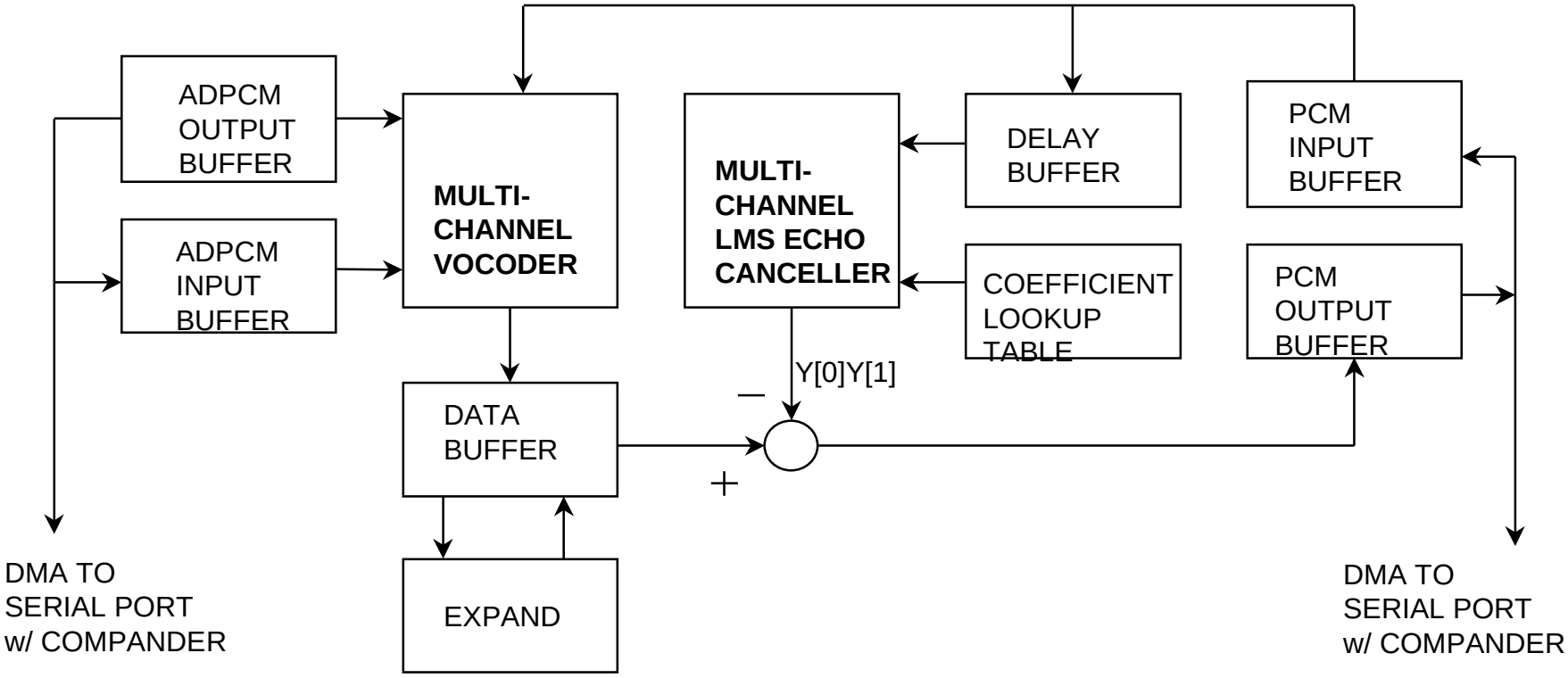
Algorithm	*'C6x @ 200MHz*	*Typical DSP @ 60 MHz*	*'C6x vs. Typical Ratio*
FFT (256-point)	14.0 us	199 us	14:1
DCT (8x8)	1.14 us	15.3 us	13.4:1
Viterbi – IS54 (89 terms)	29.5 us	315 us	10.7:1
LMS Filter (24 tap)	0.21 us	1.9 us	9:1
IIR Filter (8-biquads)	0.15 us	1.3 us	8.9:1
FIR Filter (24-tap, 64 data points)	3.9 us	31 us	8:1

New generation of tools use

- *advanced scheduling strategies* to achieve up to eight instruction in parallel every cycle
- *software pipelining techniques* to generate code that can execute multiple iterations of loops in parallel.

VelociTI™ - New Levels of DSP Performance

‘C6201 Multi-channel Application - Data Flow



VelociTI™ - New Levels of DSP Performance

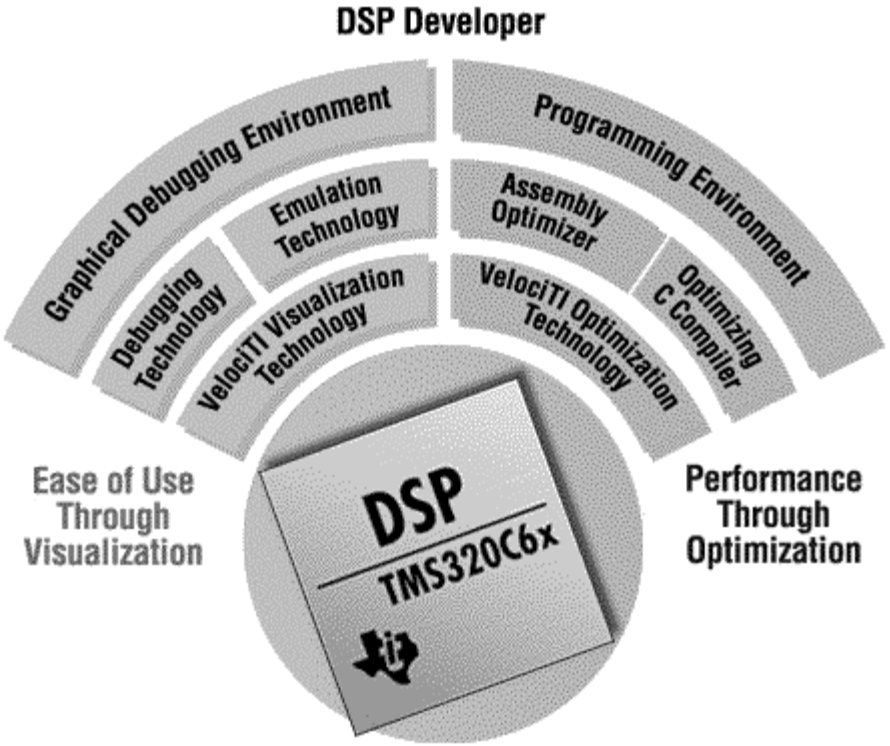
‘C6201 Multi-channel Application - Performance

•VLIW Signal Processing performance brings up to 40 channels of vocoders (ADPCM and Line Echo Cancellation) or 80 channels of ADPCM on a single-chip programmable DSP!

32K-bit ADPCM Implementation Statistics:

Program Memory: 8328 bytes (G.721 vocoder and LEC)
Data Memory: 39 KB total
(256-tap+256-coeff) * 32 channels * 2 bytes/word = 32KB for LEC
Cycles:
Real time processing between samples provides 25K cycles/125 us.
Cycles for vocoder: 9.5K cycles per sample of 32 channels
Cycles for LEC: 10.5K cycles per sample of 32 channels
Total: 20Kcps ⇨ <80% of 200MHz ‘C6201

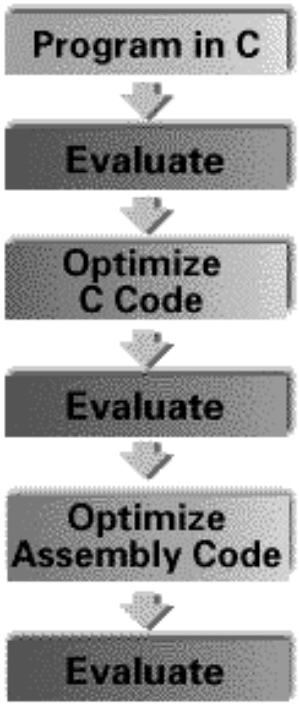
Advanced Development Tools



TI has shifted the DSP development paradigm from a hardware to software focus by supporting the programmable, high-performance 'C6x DSP with ***ultra-efficient, new-generation optimization tools****.*

Advanced Development Tools

Code Generation Flow

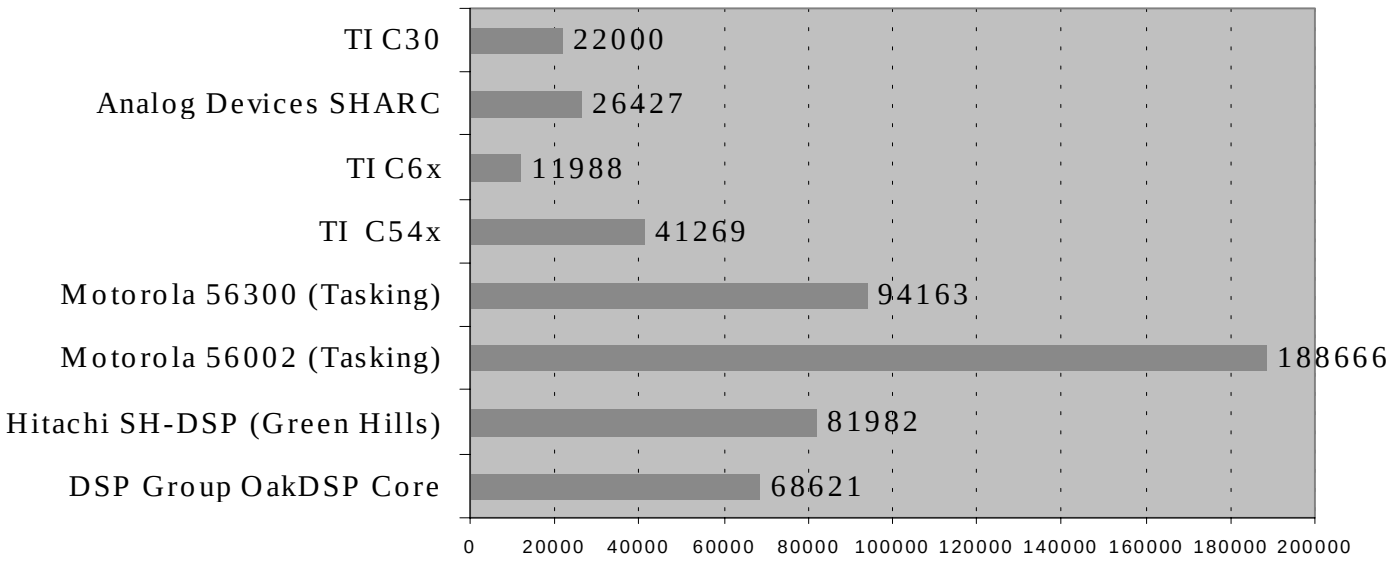


- Automated code generation handles scheduling complexities of traditional VLIW
- Tool suite support optimizing through an iterative programming process:
  - Use C Compiler to optimize and S/W pipeline
  - Use Assembly Optimizer to automatically schedule and optimize serial assembly code
  - Debug code through intuitive Windows-based source code (C and Assembly) debugger
- Optionally hand optimize only most critical functions

Advanced Development Tools

‘C6201 Compiler Efficiency (ver 1.0)

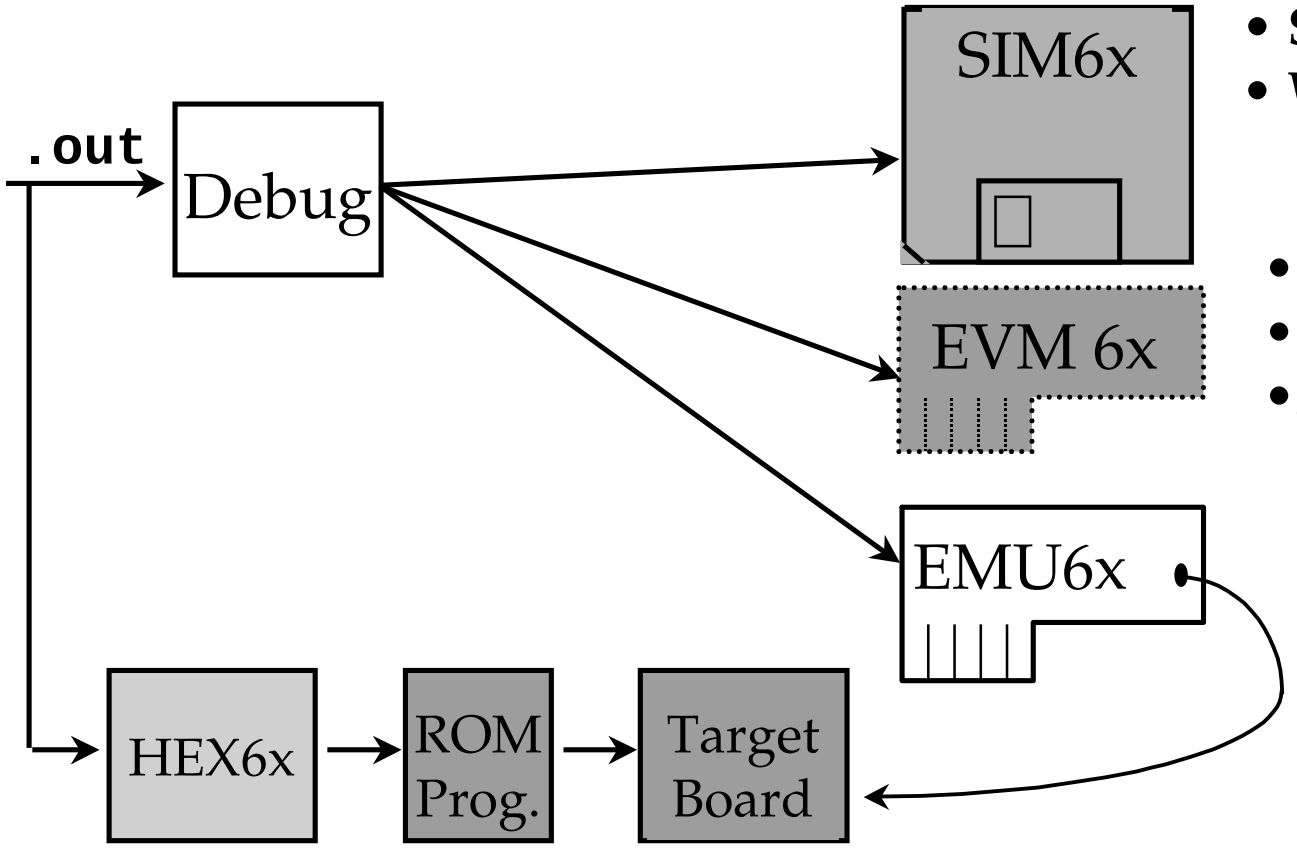
Cycle Counts for Unmodified C Benchmark Results



Cumulative Cycles of 8 Typical DSP Benchmarks (Data Courtesy EDN)

Advanced Development Tools

Debug Tools Flow



- **Software Only**
- **Win 95/NT**

- **Contains DSP**
- **PCI Card**
- **Avail 1Q98**

- **ISA card**
- **No DSP**
- **PC/Target JTAG cable**

State-of-the-Art Process Technology

- C6201 will be manufactured with TI*meline*™ 0.18 micron process 1H98
- Higher speed version (250+ MHz) and derivatives to be expected in near future
- Higher levels of integration and peripheral mix using ASIC-flow are forthcoming

Summary

‘C6x VelociTI™ Advanced VLIW enables:

- Delivering 10x performance of any DSP on the market today.
- Shifting development paradigm from a hardware focus to a software focus.
- Establishing VelociTI Advanced VLIW as the architecture of choice for high-performance, low-cost DSP solutions.
- Reducing development time by half with new-generation tools designed for greatest ease of use and maximum optimization.
- Reducing system cost by half for multi-channel/multi-function applications.
- Opening the future to endless possibilities in real-time voice and data communications.