# 1/4-Inch CMOS Active Pixel Sensor with Smart On-Chip Functions and Full Digital Interface

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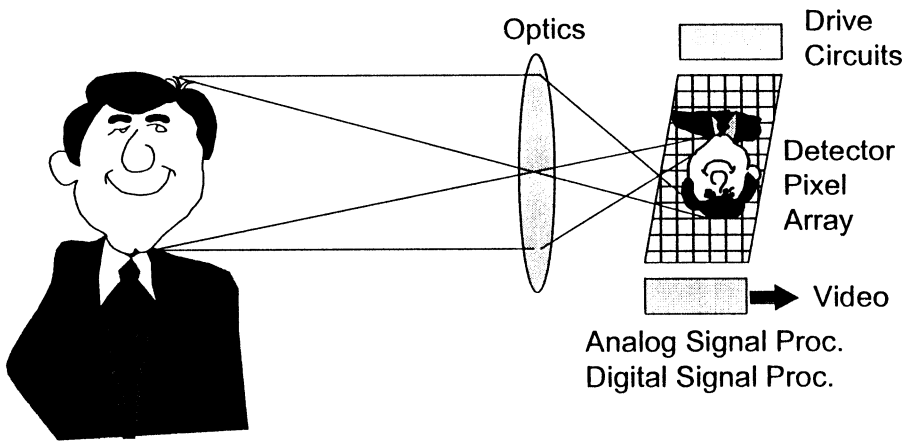
# Part I.

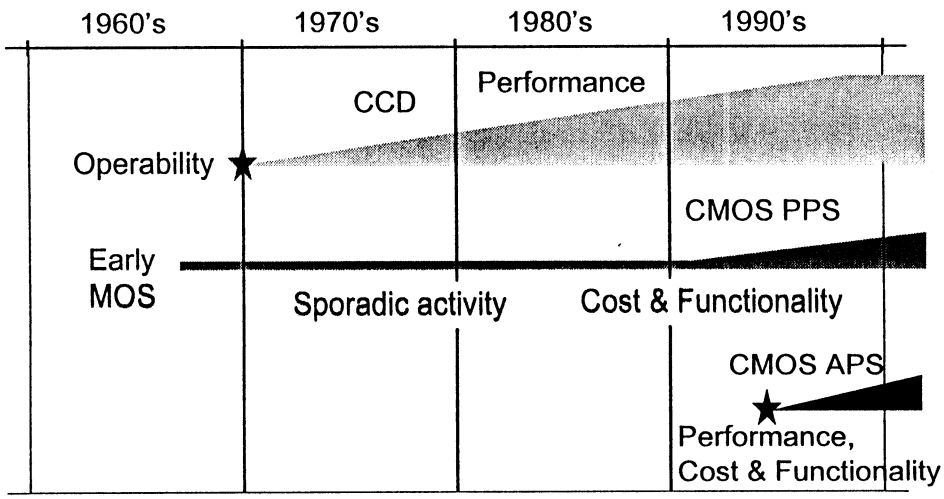
## Brief Introduction to CMOS Image Sensors

## IMAGING SYSTEMS






## TIMELINE

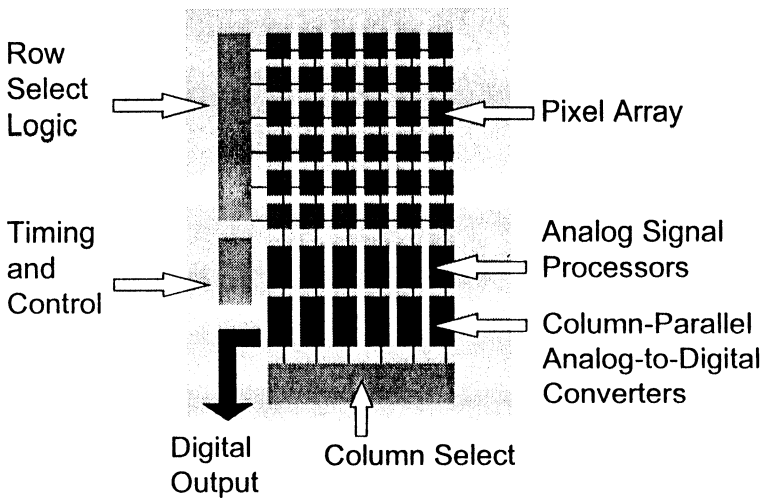


## CCD LIMITATIONS

- Requires high charge transfer efficiency
  - Special fabrication process
  - Large voltage swings, different voltage levels
- Difficult to integrate on-chip timing, control, drive and signal chain electronics
- Serial access to image data
- System power in 1-10 Watt range



## CMOS IMAGE SENSOR ARCHITECTURE

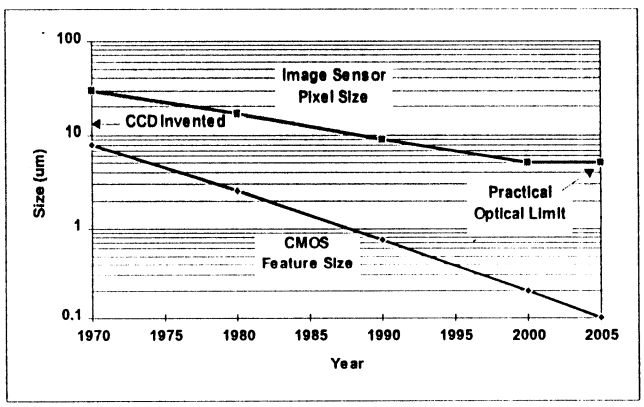


## TIMING IS EVERYTHING

- CMOS state of the art is ripe for image sensors
  - Design rules permit competitive pixel sizes
  - Defects and contamination well controlled
  - Threshold voltages stable and fairly uniform
- Customers demand low power, miniaturized systems-on-a-chip
- Circuit techniques developed for high performance
  - Active pixel provides gain in pixel
  - Column parallel architecture permits low analog bandwidths to reduce noise and artifacts.
  - Use of double-correlated sampling and double-delta sampling on-chip removes temporal & fixed pattern noise



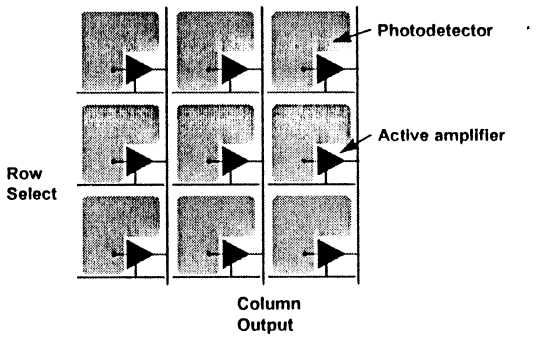
## EVOLUTION OF FEATURE SIZE




- Enough space to put amplifier into each pixel.

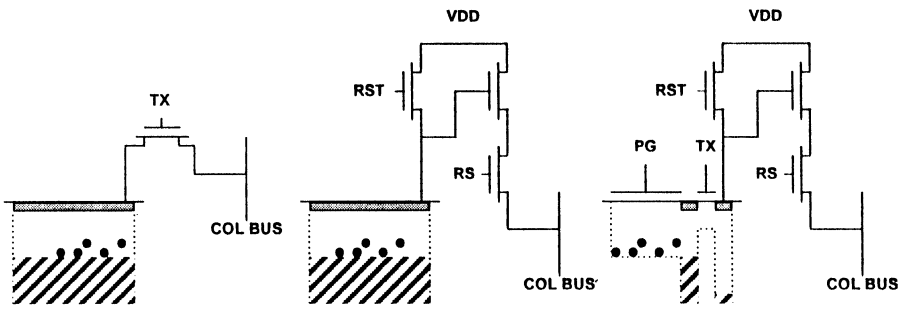
# ACTIVE PIXEL

- Each pixel has its own output amplifier
- Pixels are X-Y addressed
- Key is low noise readout circuit
- Best of CCD detection/readout and CMOS integration



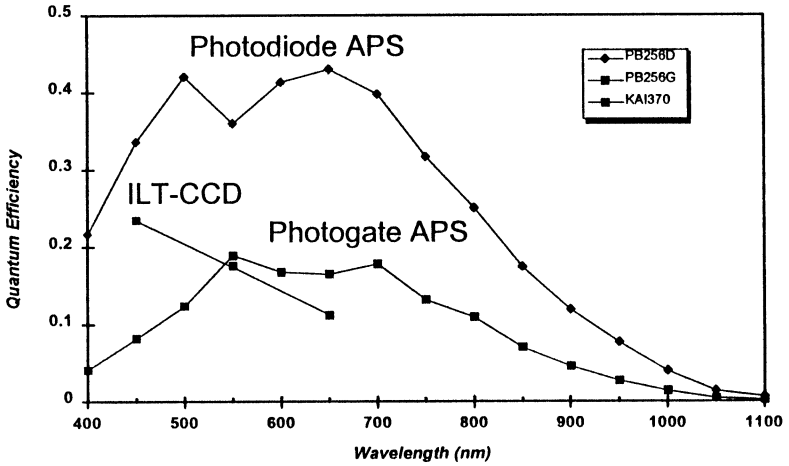



# COMMON CMOS PIXELS



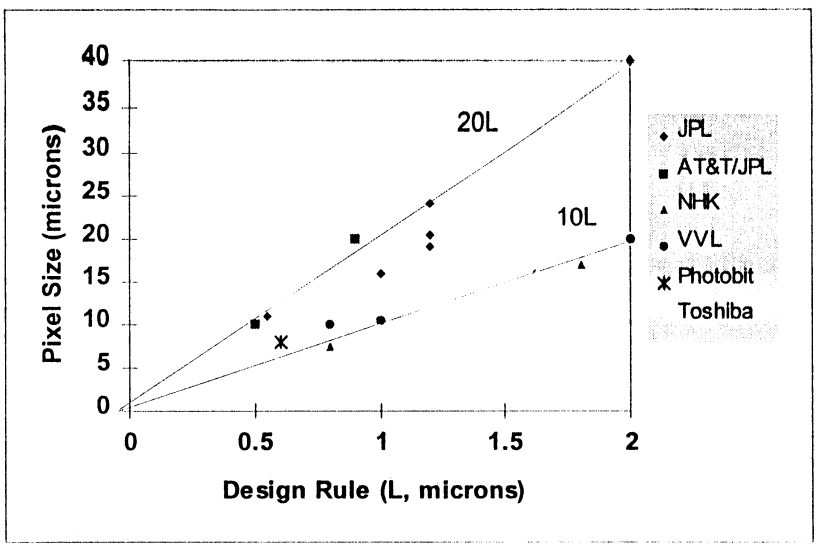

| Passive Pixel | Photodiode CMOS APS | Photogate CMOS APS |
|---|---|---|
| • 1 transistor pixel | • 3 transistor pixel | • 5 transistor pixel |
| • 10 L scaling | • 15 L scaling | • 20 L scaling |
| • Great QE | • Great QE | • Good QE |
| • Poor noise (250 e-) | • OK noise (50-100 e-) | • Great noise (15 e-) |
| • Poor scaling for large arrays | • Good for large arrays | • Good for large arrays |
| • Poor for fast readout | • Good for fast readout | • Good for fast readout |

# APS QUANTUM EFFICIENCY






# SCALING TREND



## ON-CHIP ADC

- Permits full digital interface
- Permits on-chip DSP for camera control, color interpolation, etc.
- Suppresses noise pick up from EMI, crosstalk
- Simplifies interface
- Permits faster readout
- Can reduce overall chip power



## ON-CHIP ADC CHOICES

- One (or two or three) ADCs per chip
  - High data rate requirement (5-60 Mconv/s)
  - Local high power dissipation
- One ADC per pixel
  - Large pixels and low fill factor
- One ADC per column (column-parallel)
  - Tall, skinny ADCs

- Single-slope
  - slow
- Successive approximation
  - 8-10 b max
- Algorithmic
  - needs op-amp
- Oversampled
  - Filter takes lots of area
- Flash
  - Lots of power

# PB256E

- 256x256 Element PD-APS
- 256 Column-parallel ADCs
- 8b Resolution
- On-chip FPN suppression
- 30 frames per second
- Under 50 mW total power
- Note lack of blooming or other artifacts

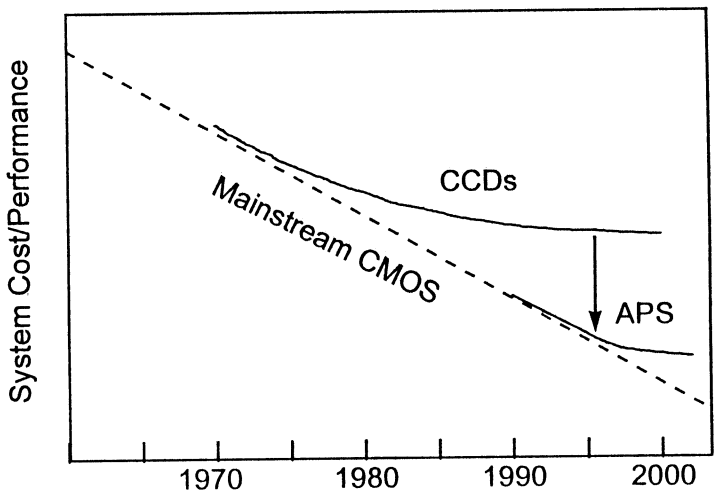
*Panicacci 1996*



# ADVANTAGES OF CMOS APS

- Maintains high performance of CCD sensors
  - high sensitivity, low noise, wide dynamic range
  - no smear, no blooming, no lag
- 100 x less system power than comparable CCD system
  - 10-50 milliWatts instead of 1-5 Watts
  - single 5V (3.3V) supply, full digital interface
- 10 x less camera volume than comparable CCD system
  - on-chip integration of timing, control, ADC functions
- 2 x less cost
  - fewer components, simple module assembly
- Unique functional advantages
  - Window of interest readout for electronic pan, tilt, zoom.
  - Ultra wide intrascene dynamic range
  - On-chip DSP and sensor control functions (e.g. AGC)

## DISCUSSION






# Part II.

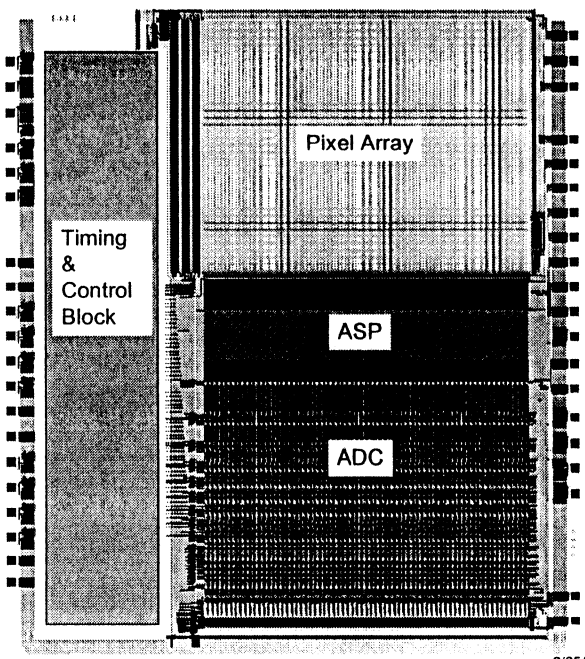
# 1/4-Inch CMOS APS with On-Chip Smart Functions and Full Digital Interface (PB159)

# STATUS

- Sensor is in fabrication (7/7/97).



# CHIP LAYOUT

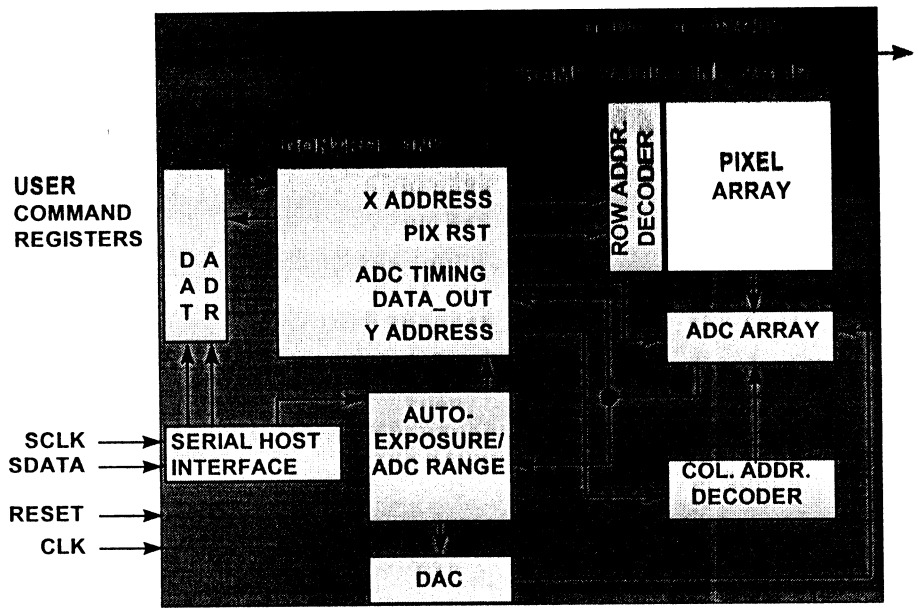


# CHIP SPECIFICATIONS

| | |
|---|---|
| Total Effective Pixels | : 196,608 (512 x 384) |
| Pixel Size | : 7.9 μm x 7.9 μm photo-diode |
| Shutter | : electronic rolling snap |
| CDS | : on chip |
| ADC | : on chip 8 bit column parallel |
| Output | : 8 bit color digital video |
| Data rate | : 14.3 Mbytes/s |
| Auto Exposure | : on chip with manual user override |
| Package | : 40 pins |
| Timing and Control | : on chip controller with 14.3 MHz master clock |
| Power | : 40 - 50 mW |
| Programmable features | : window size and location |
| | exposure |
| | ADC reference |
| | frame rate |
| | ADC test mode |
| | readable chip internal registers for test |
| | auto exposure parameters (update rate, thresholds) |
| | on command ADC calibration |



# SENSOR BLOCK DIAGRAM



## FEATURES

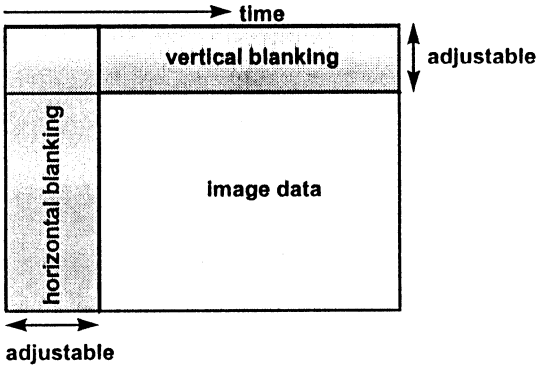
- Default power up state does not require user to program the device in order to get continuos video (default setting produces 512 x 384 window at a 30 Hz frame rate with auto exposure enabled).
- Industry standard serial interface to load user commands (Sensor has 2 hardware selectable device addresses so that other devices can share the serial bus including another APS sensor).
- Auto exposure settings includes a disable for manual exposure control. Hold current exposure command also available for auto-exposure.



## FEATURES (cont.)

- Adjustable frame rate (3-40 Hz)
- Sensor chip enable register allows user to pause imager (no integration).
- Low power standby pin available to turn off DC power consumption (10 mW residual AC power from14.3 MHz clock component)
- Simple user interface has a master clock, 2 signals for serial interface, 8 data outputs, 4-5 bias pins (1.2V,2.5V,1V), VDD(5V), and GND(0V). External biases generated with simple resistor divider between VDD and GND.

# OUTPUT DATA FORMAT




- 8 bit digital image data with embedded sync's (pseudo CCIR-656)
- data control codes requires FF, 00 image data to be mapped to FE, 01
- frame valid, line valid sync output pins also available



# SUMMARY

- CMOS APS technology permits high performance imaging with standard CMOS.
- A new 1/4-inch CMOS APS with smart on-chip functions and full digital interface has been introduced.