Technical challenges associated with the development of Intel 440LX AGPset

Richard Malinowski
Director, Chipset Engineering
Platform Components Division
Intel

Agenda

- The Goal
- System Architecture Overview
- 440LX AGPset Design Goals
- 440LX AGPset Microarchitecture
- 440LX AGPset Complexity & Design Challenges
- 440LX AGPset Performance
- Summary

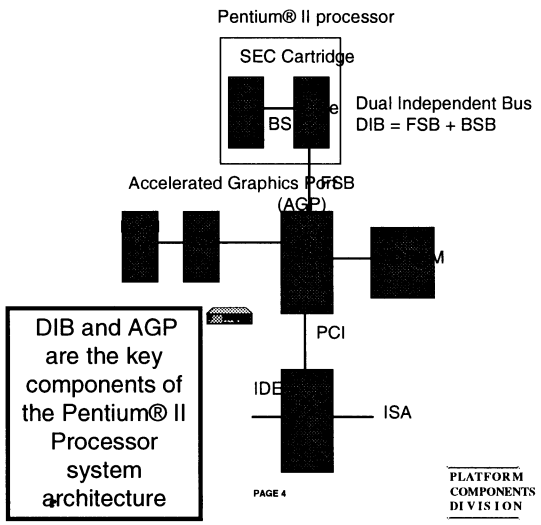
The Goal

Deliver High Performance 3D Graphics to the Mainstream PC

The system must manage the explosion in data flows that result

System Architecture Overview

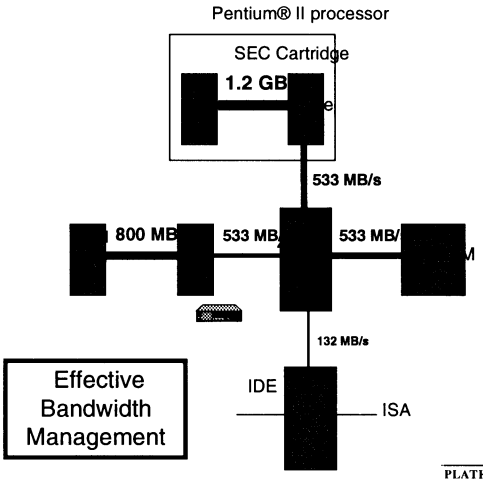
Pentium® II Processor System with AGP



DIB and AGP are the key components of the Pentium® II Processor system architecture

440LX AGPset Design Goals

Performance: The Problem



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440LX AGPset Design Goals

Performance: The Problem, 3D Example

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440LX AGPset Design Goals

Performance: The Solution

- 3-port Concurrency
  - CPU-L2 and the rest of the system
  - CPU-AGP and AGP-memory
  - CPU-AGP and PCI-memory
- Flexible Arbitration
- Deep Buffering and Pipelining

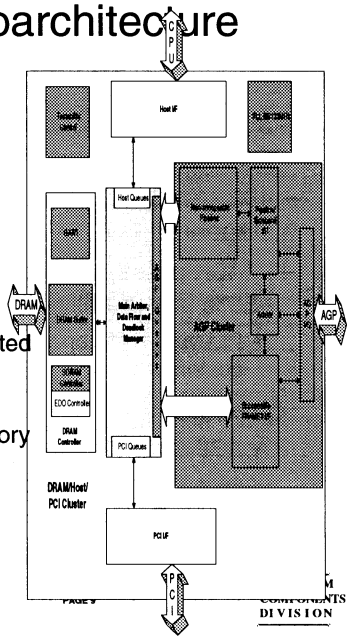
440LX AGPset Design Goals

Cost and Schedule

- Cost
  - 0.6u BiCMOS technology
  - 492 MiniBGA packaging
- Schedule
  - 1 year from AGP spec to production shipments

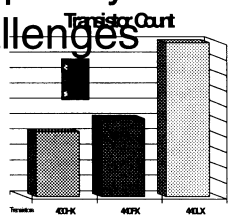
440LX AGPset Microarchitecture

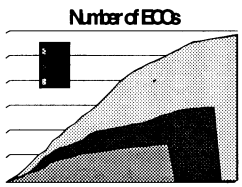
- 3-port concurrency
- 2 AGP data streams:
  - snoopable
  - non-snoopable
- Distributed arbitration
- Deep, distributed queuing & buffering
- SDRAM Memory Controller
- GART
- Testability
- Circuits, PLL (133/66)

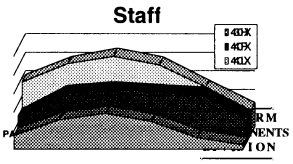


440LX Complexity and Design Challenges

- 2x complexity of the previous PC chipset generations
  - 3 port concurrency boundary cases
  - Complex arbitration
  - Deep pipelining and buffering architecture
  - AGP circuit design
  - SSO and noise
  - 492 BGA packaging
- Performance modelling





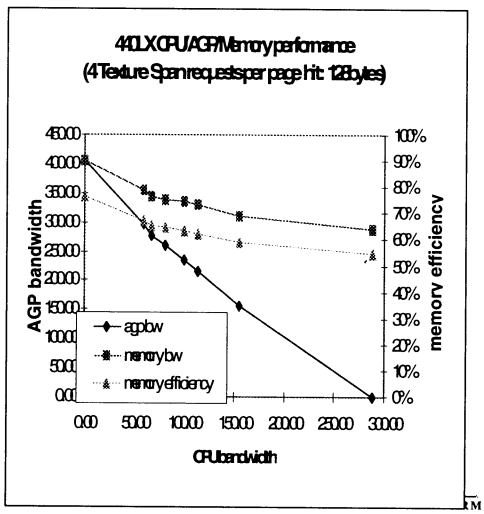


440LX AGPset Design Goals

- Cost Results
  - 350 mil die size, 0.6u 4LM Bi-CMOS process
  - 492 MiniBGA, 60/120 mil pad pitch staggered I/O
  - ~140K gates, embedded array, ~50% layout utilization
    - PLL and RAM array embedded blocks, custom I/O
- Schedule
  - AGP Spec 1.0 - August'96
  - 440LX A-0 T/O - December'96
  - 440LX Production Shipments - July'97
  - 440LX Product Launch - August'97

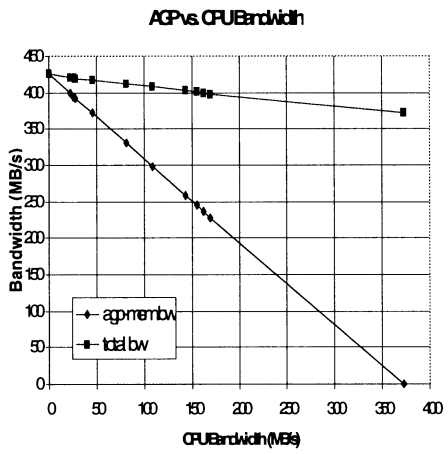
440LX AGPset Performance

Simulated bandwidth



440LX AGPset Performance

Measured bandwidth



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Summary

- DIB and AGP are the key components of the Pentium® II Processor system architecture
- Intel 440LX AGPset is the most complex PC core logic developed to date
- Efficient memory bandwidth management via 3-port concurrency enables high performance 3D in the mainstream PC

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