High Performance Caches: The Quiet Revolution

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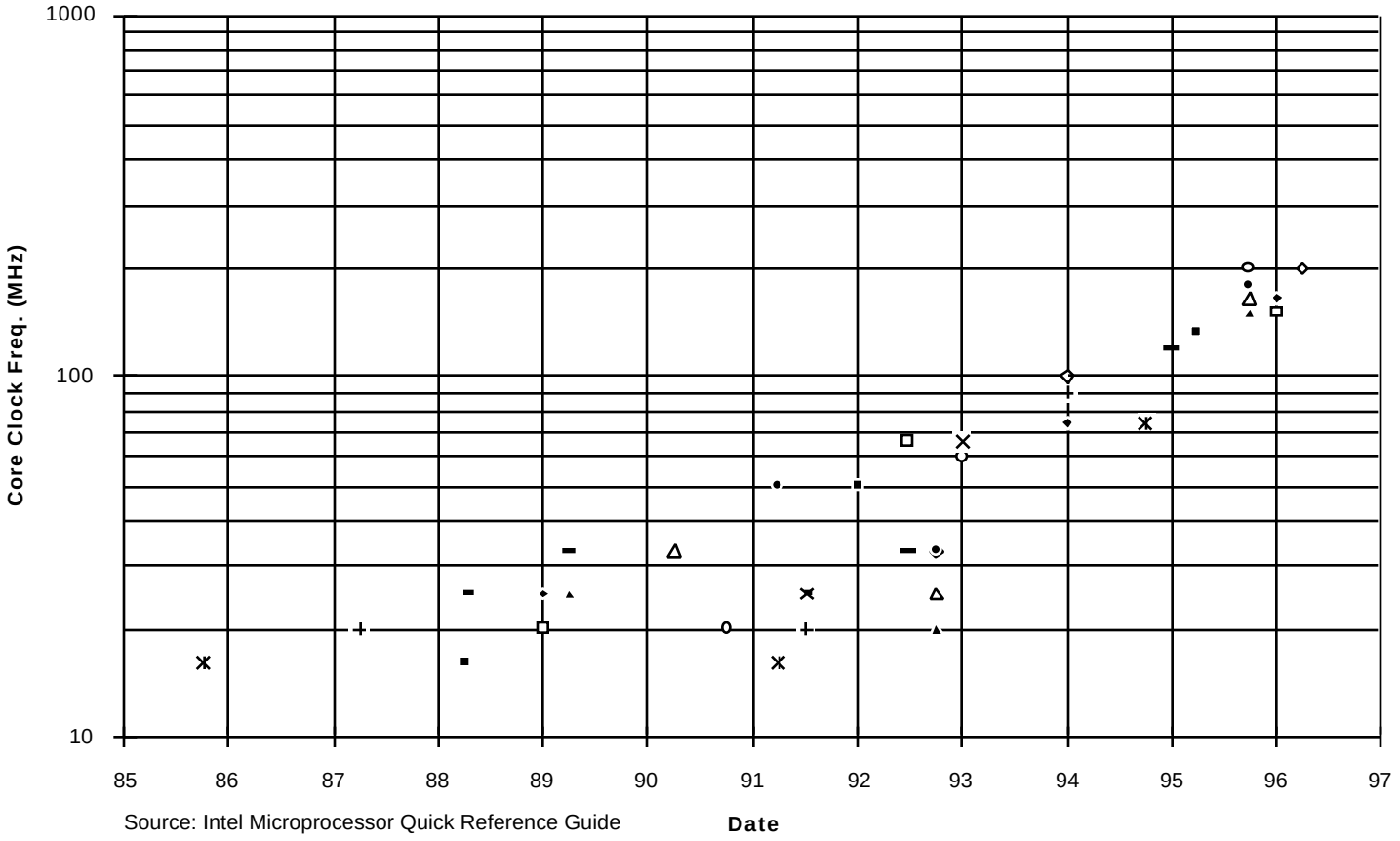
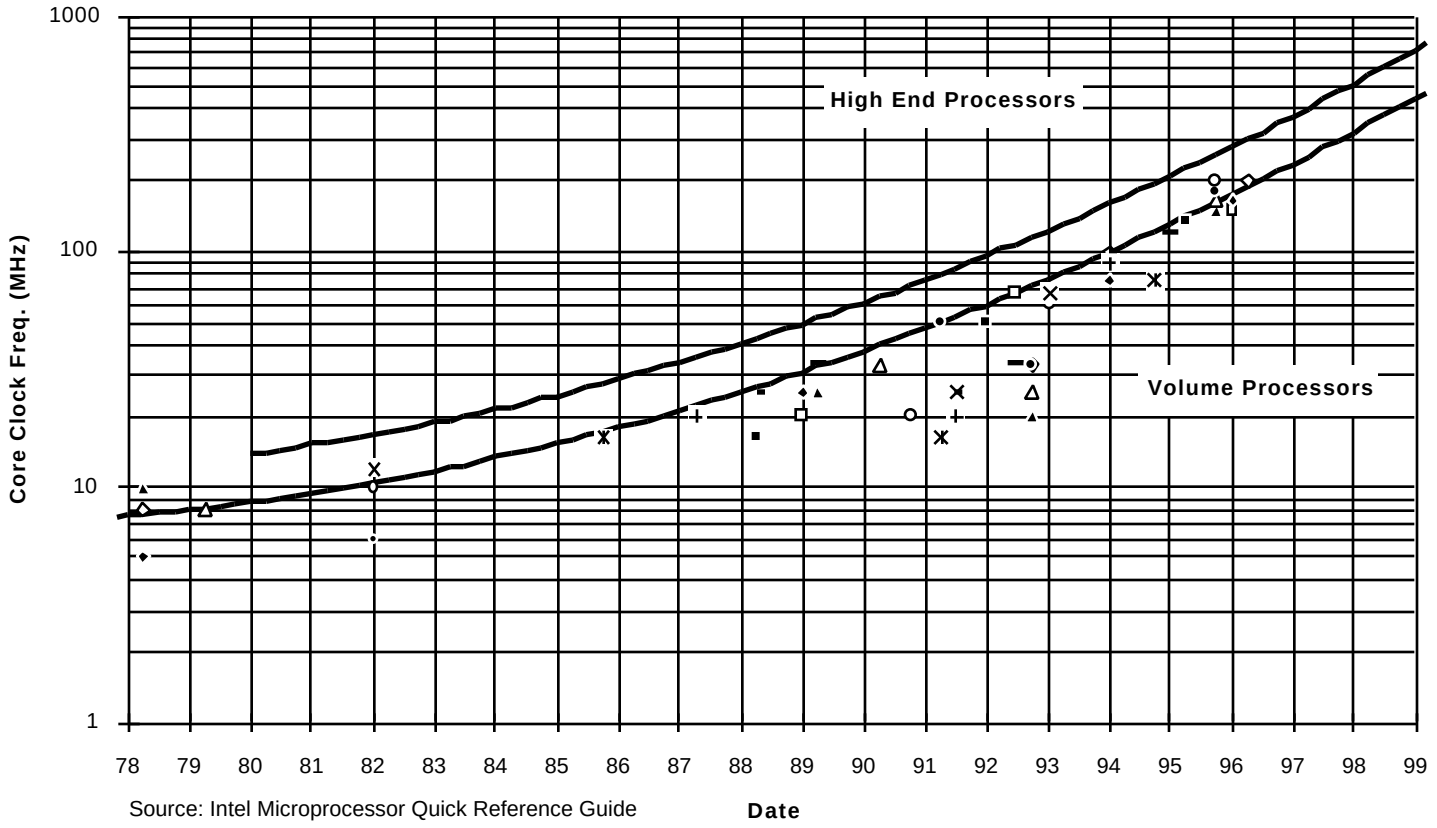
MOTOROLA

Intel Processor Core Clock Frequencies



Source: Intel Microprocessor Quick Reference Guide

Processor Core Speed Trends
The Long View



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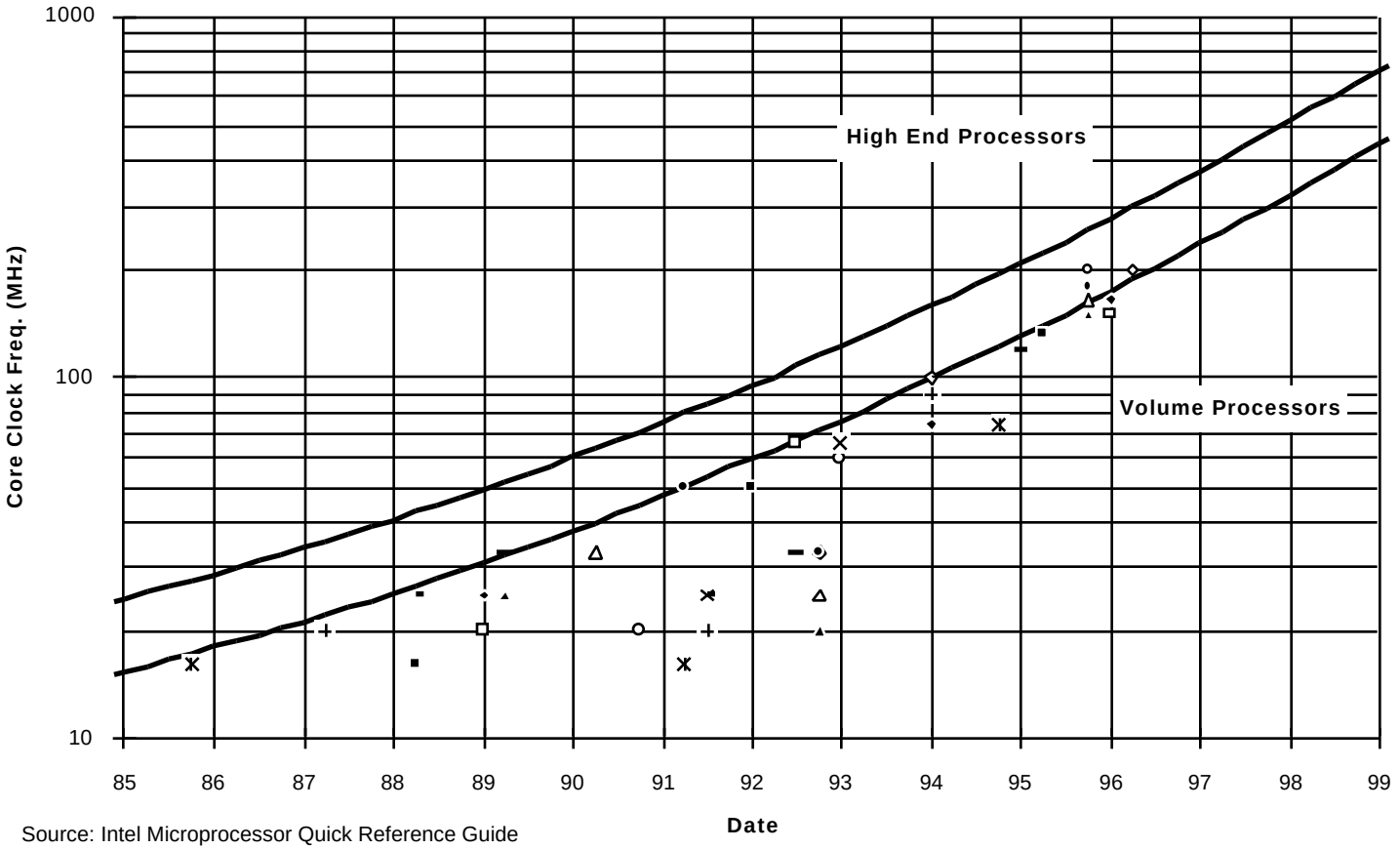
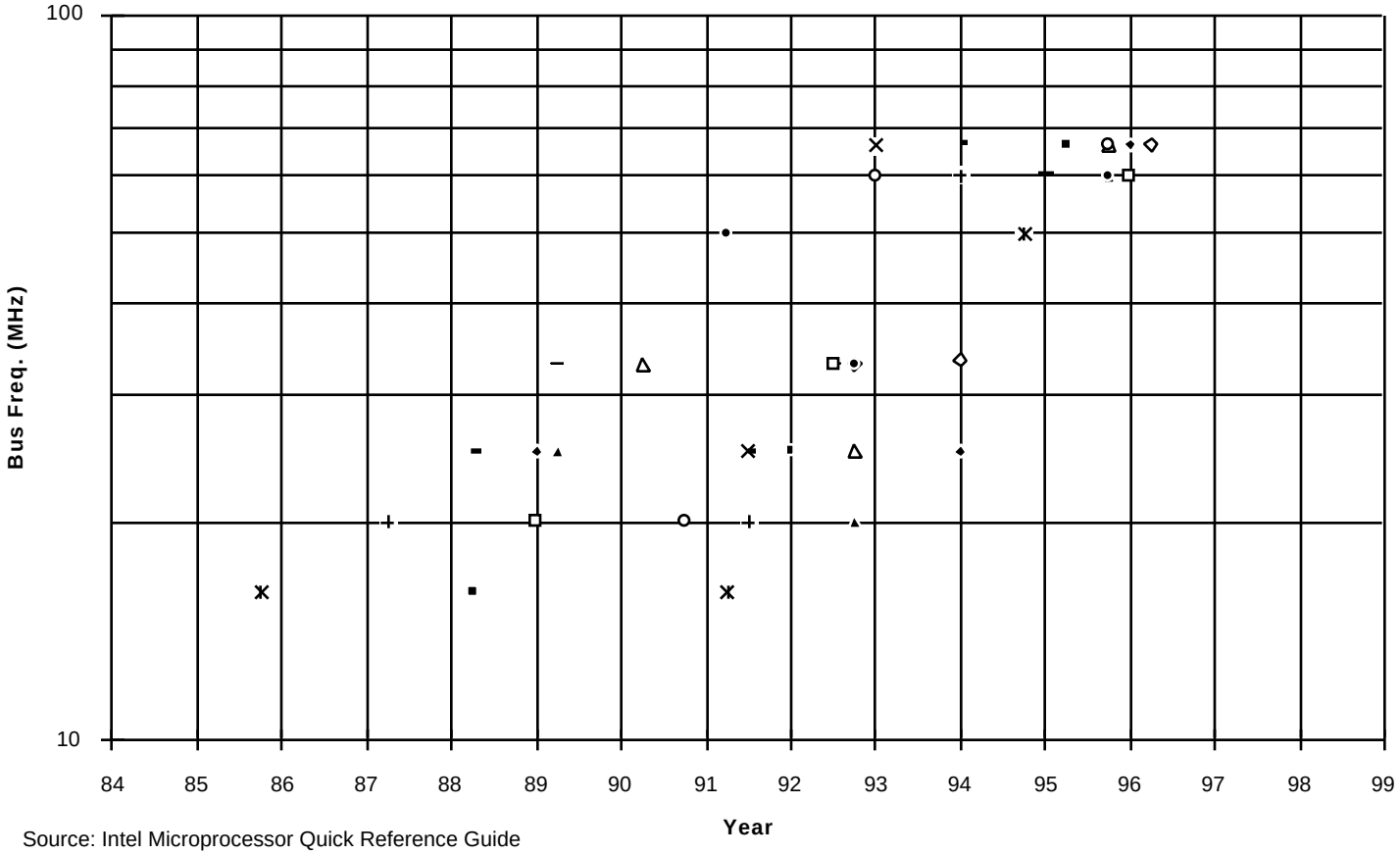
Processor Core Speed Trends



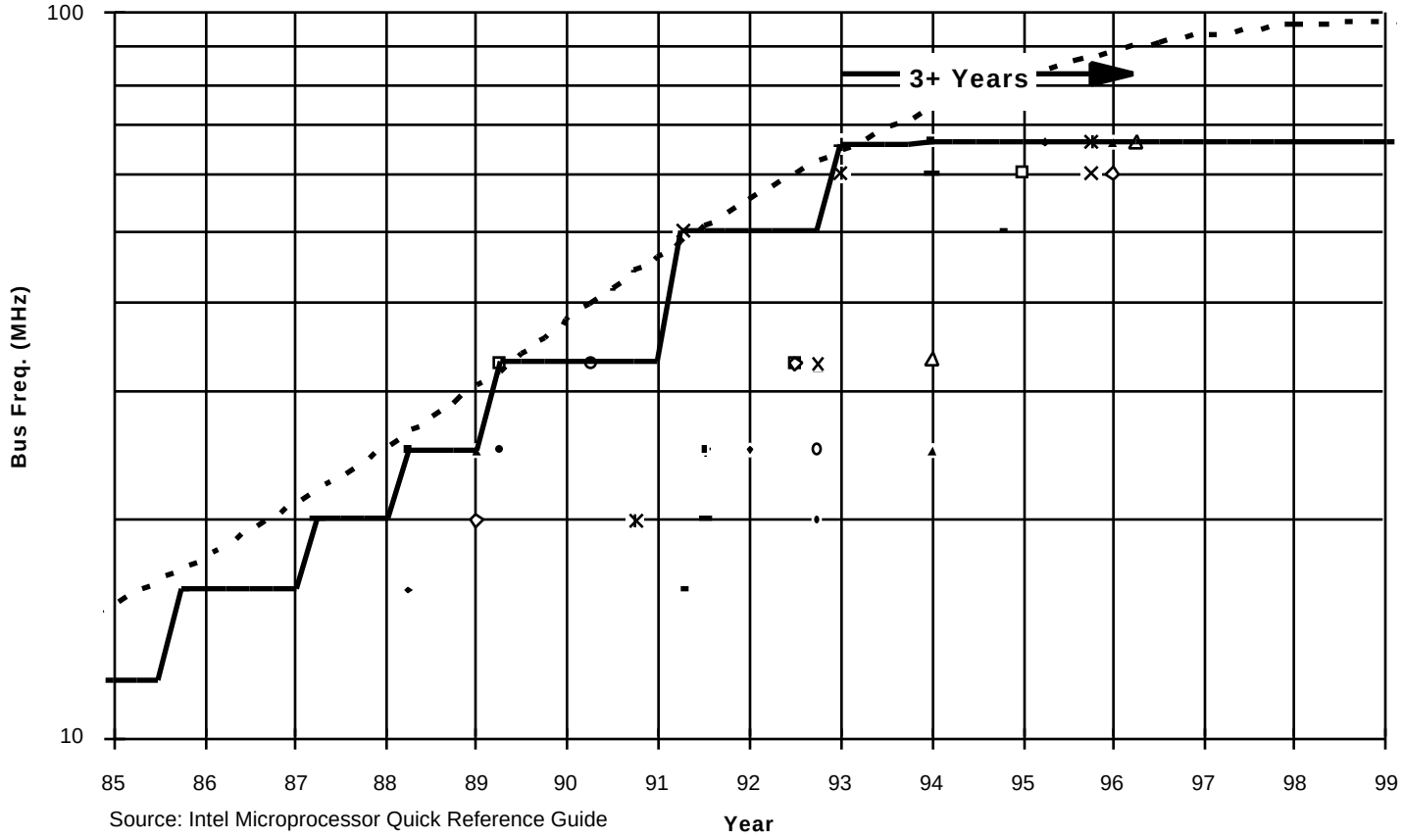
Source: Intel Microprocessor Quick Reference Guide

Intel System Bus Speeds



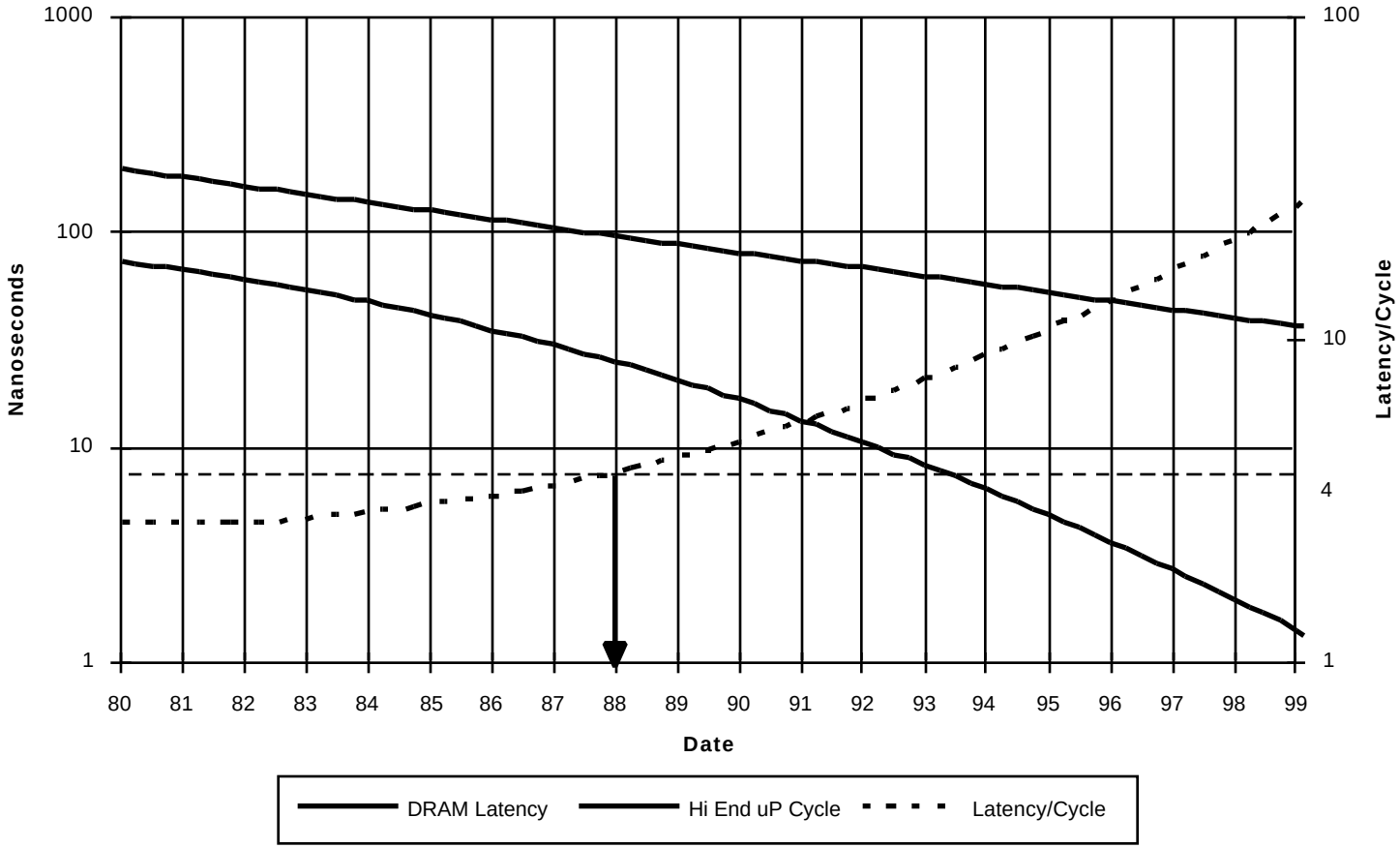
Source: Intel Microprocessor Quick Reference Guide

Volume Processor Max. Bus Speed Trend

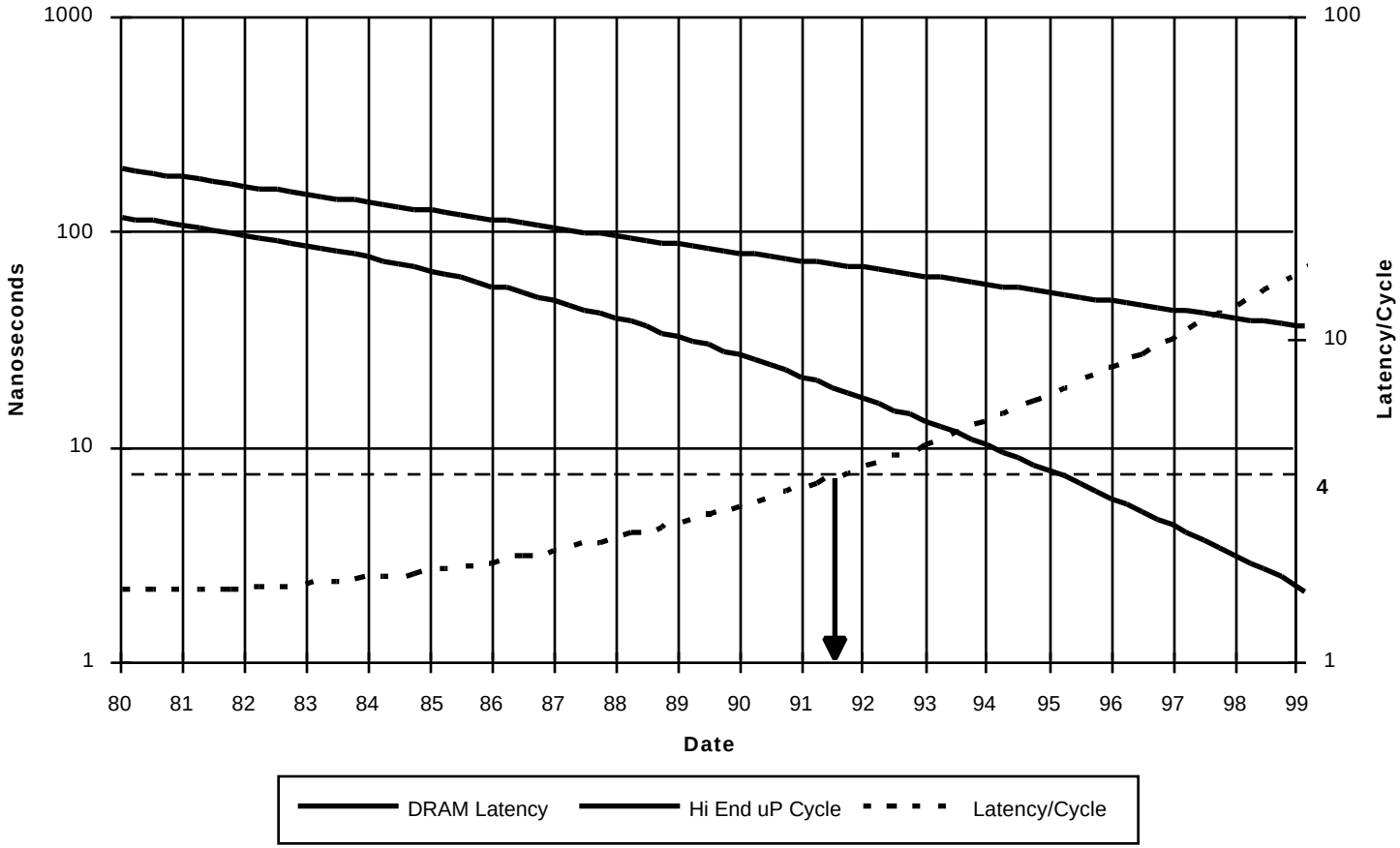


Source: Intel Microprocessor Quick Reference Guide

High End Processor Cycle Time vs. DRAM Latency

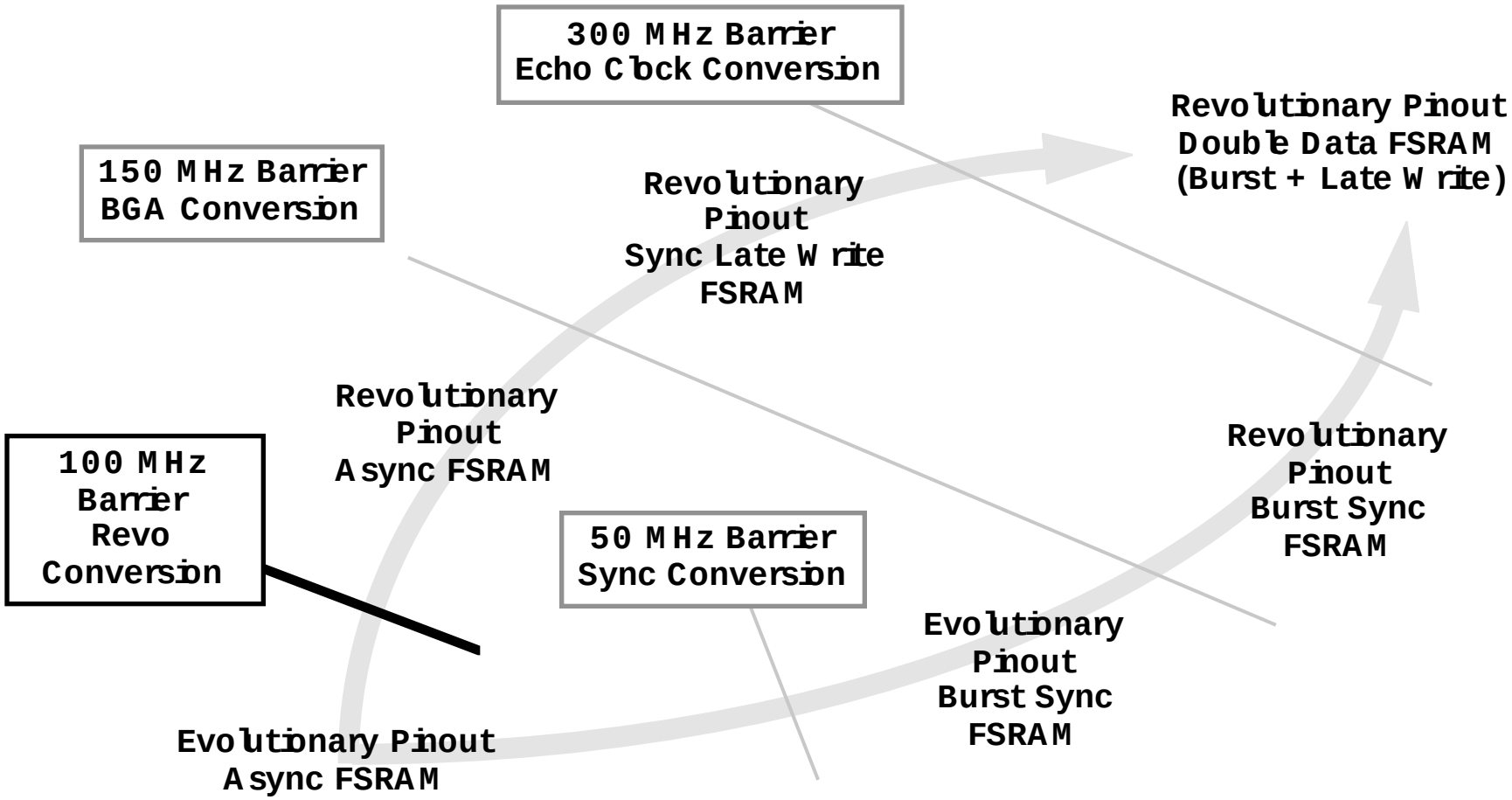


Volume Processor Cycle Time vs. DRAM Latency

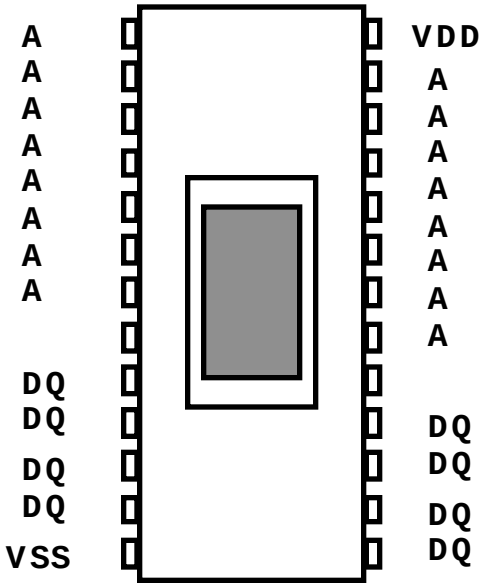


Processor Bus Frequency	Processor Cycle Time	RAM Access Time Requirement
MHz	ns	ns
16	60	30
20	50	25
25	40	20
33	30	15
40	25	12.5
50	20	10
58	17	8.5
66	15	7.5
83	12	6
100	10	5
125	8	4
142	7	3.5
166	6	3
200	5	2.5
250	4	2
333	3	1.5
285	3.5	1.75
333	3	1.5
400	2.5	1.25
500	2	1
666	1.5	0.75

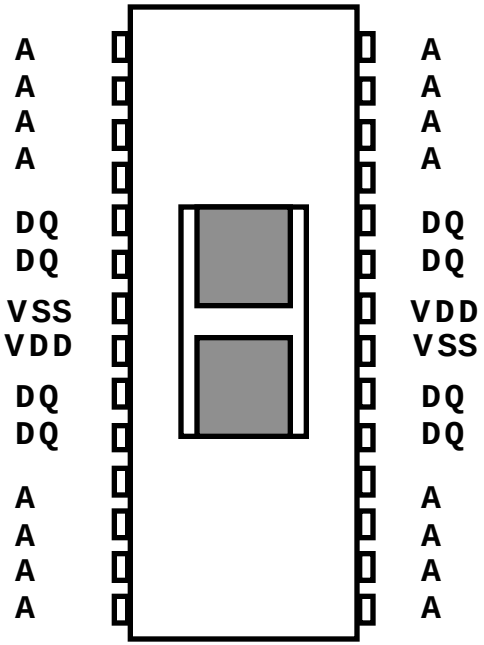
Cache SRAM Breakthroughs



Evolutionary Pinout and Architecture FSRAM

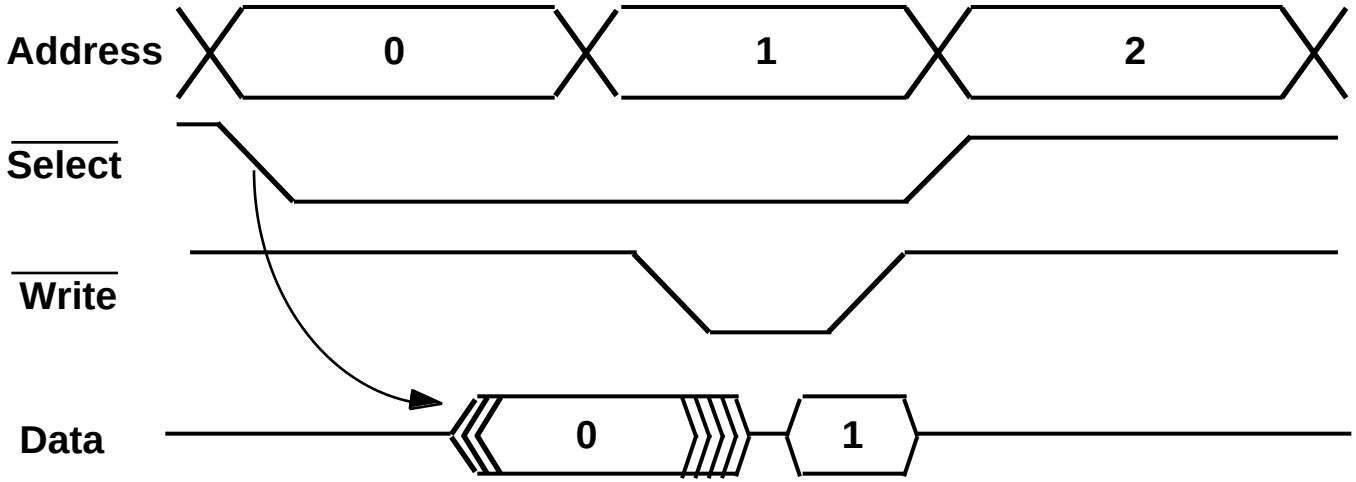


Revolutionary Pinout and Architecture FSRAM

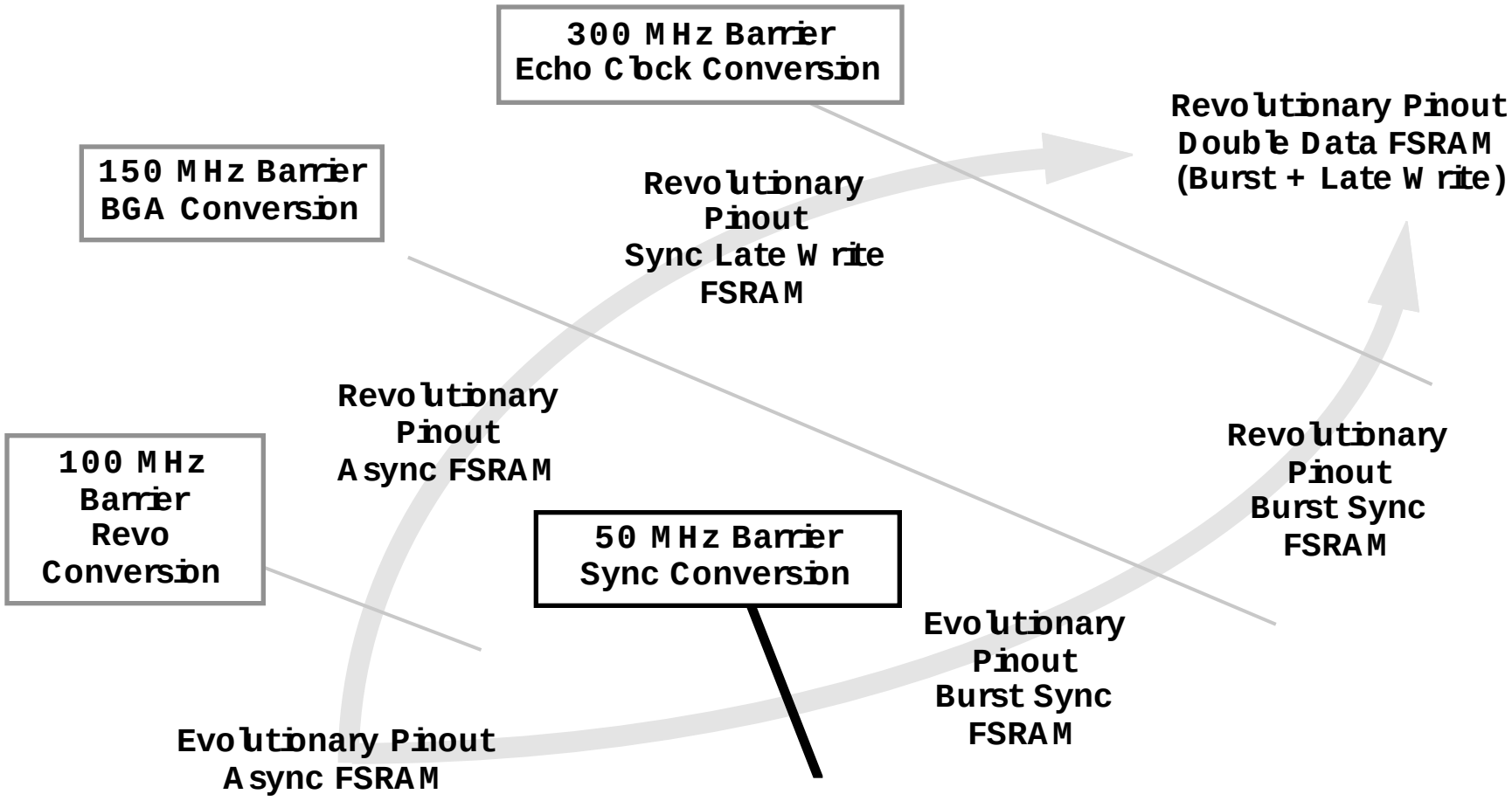


Note: Drawings not to scale

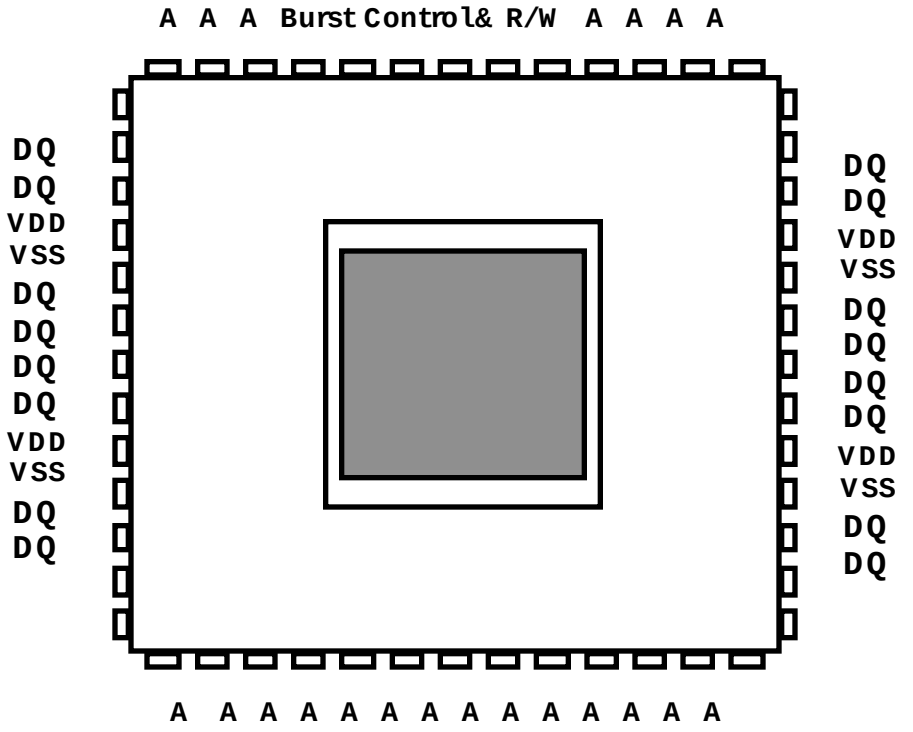
Asynchronous Read-Write Sequence



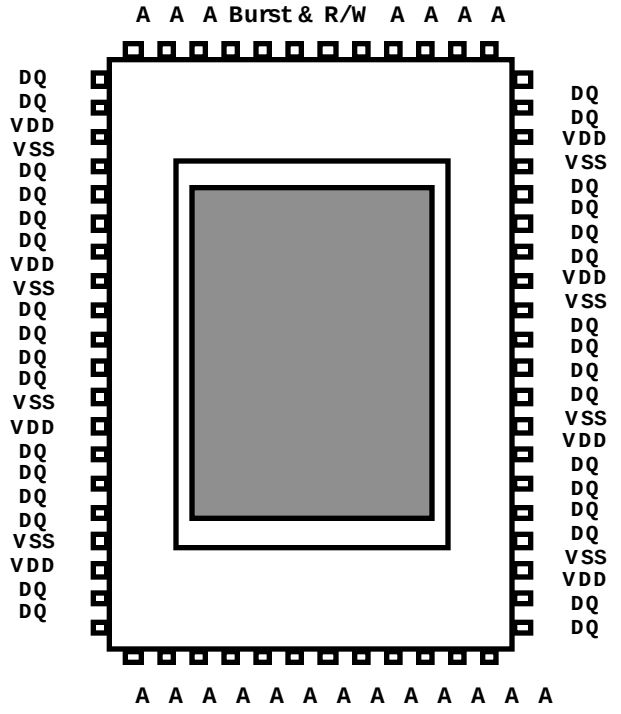
Cache SRAM Breakthroughs



Evolutionary
Pinout and Architecture
Pipelined Burst SRAM



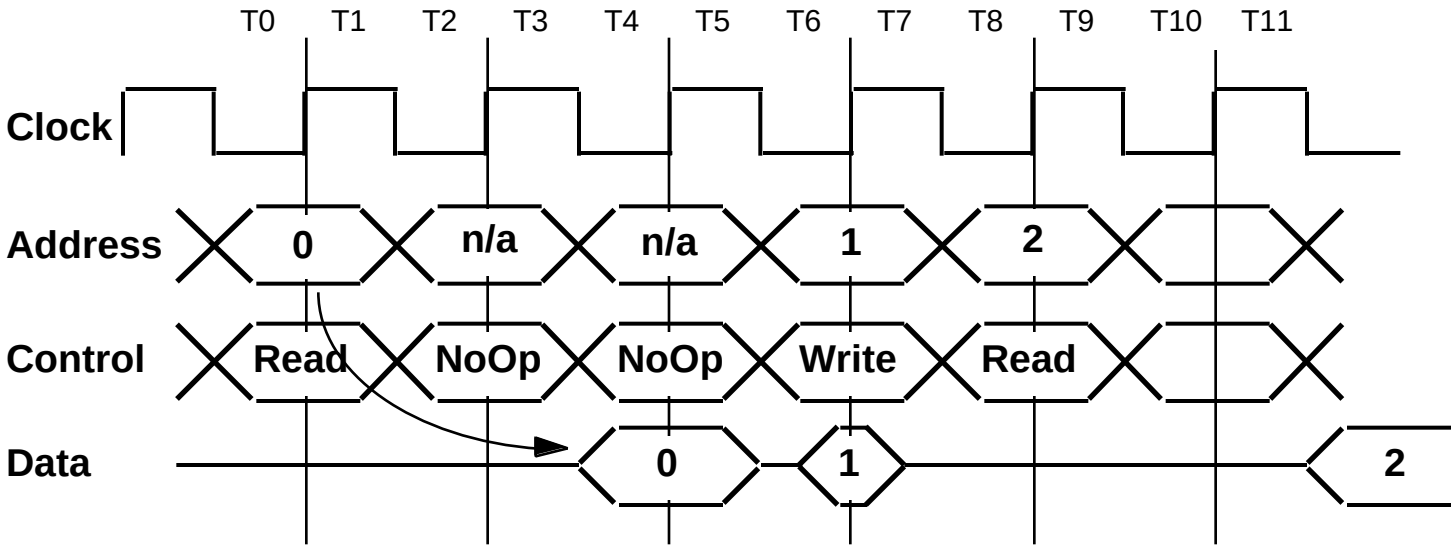
x16 PLCC



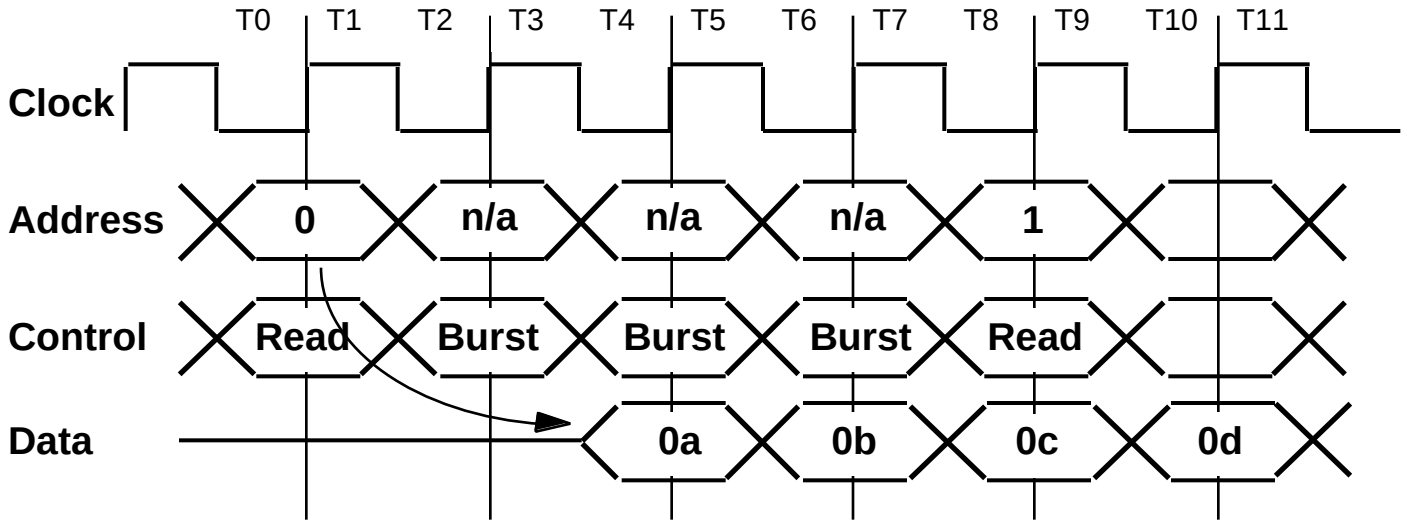
x32 TQFP

Note: Drawings not to scale

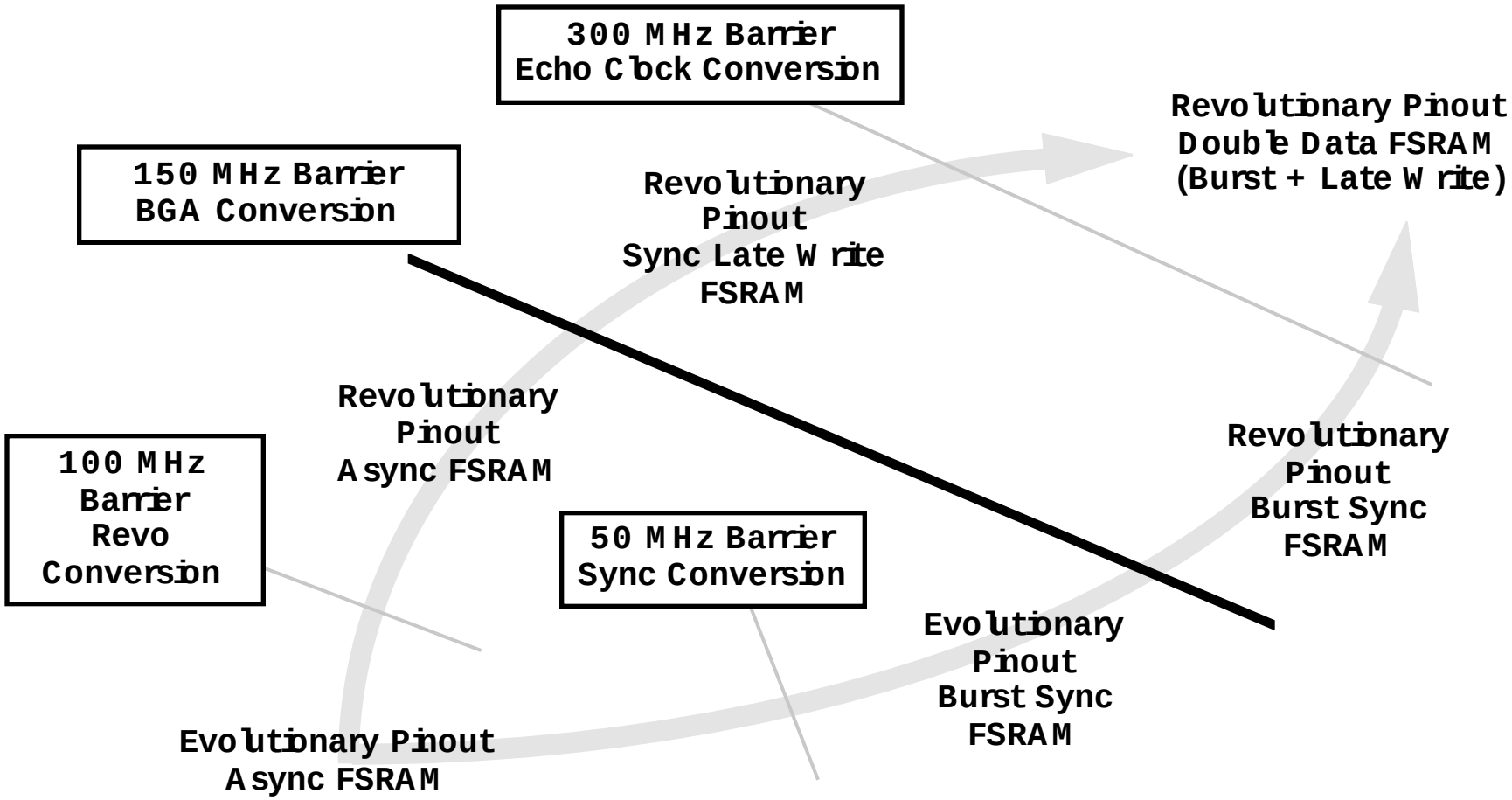
Pipelined Burst Synchronous Read-Write-Read Sequence



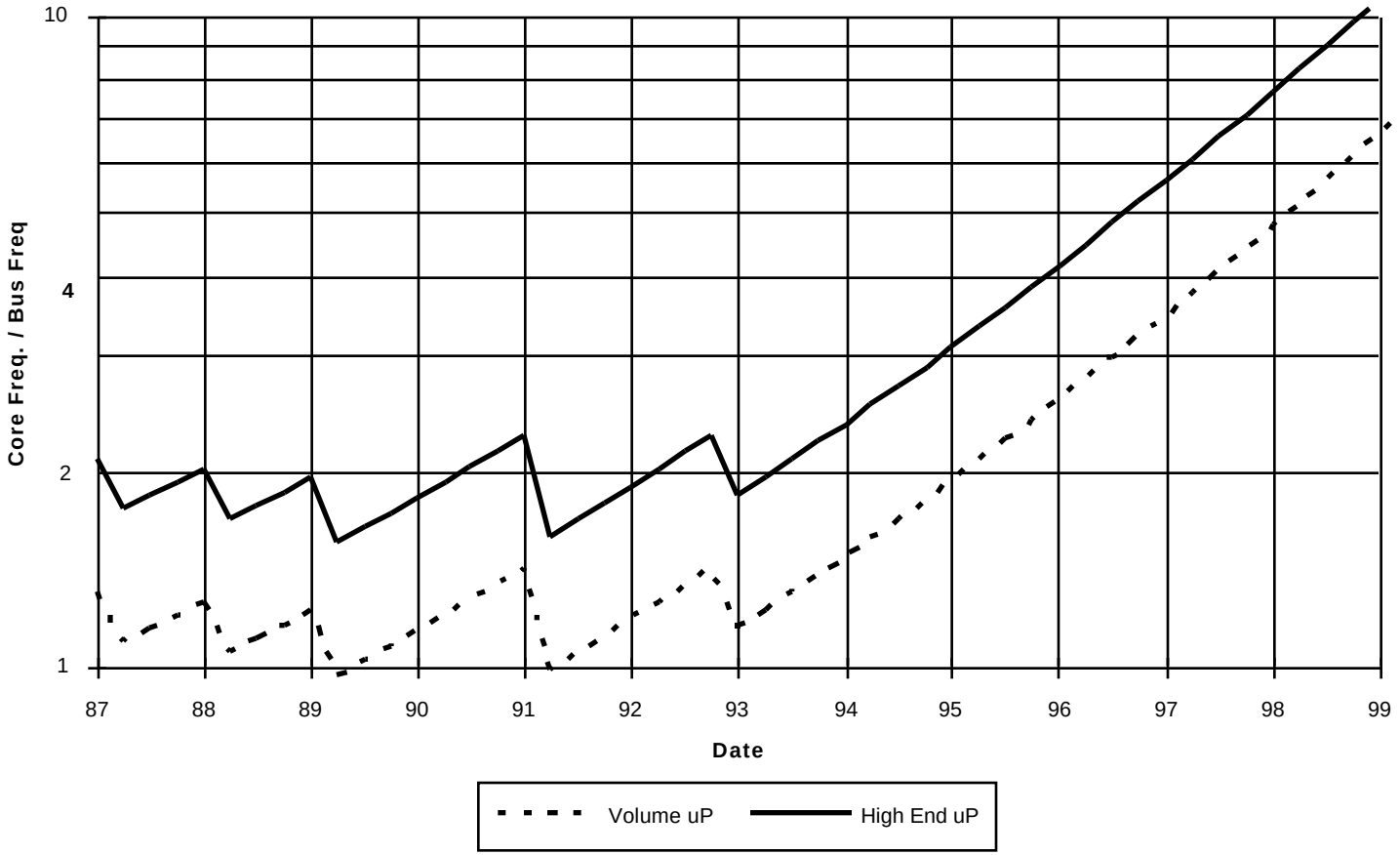
Pipelined Synchronous BurstRAM Burst Read Sequence



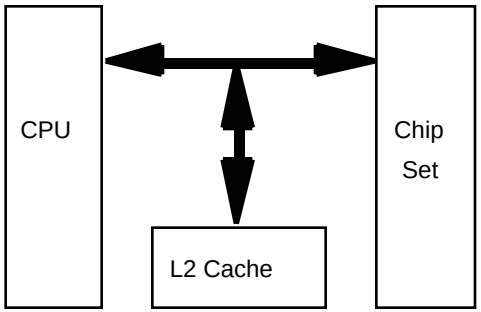
Cache SRAM Breakthroughs



Processor Core Frequency vs. Volume Bus Frequency

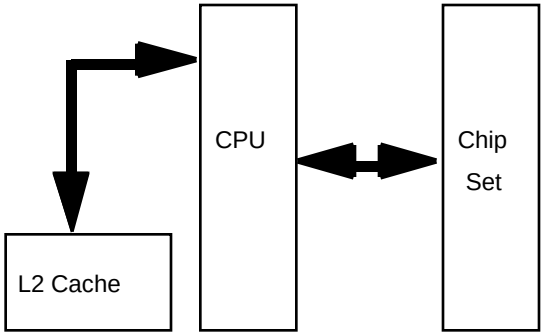


Back Side L2 Port Architecture Frees FSRAMs to Run at Core Frequency



Traditional Standard Lookaside L2

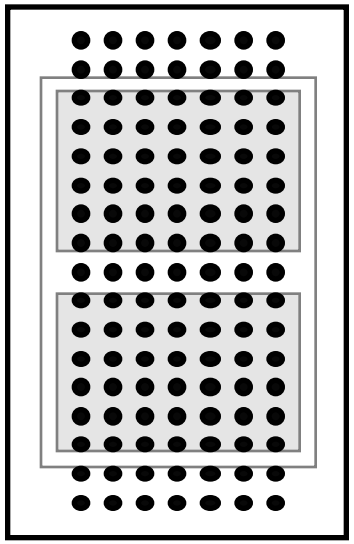
- The **Traditional** CPU/ L2 Cache Architecture
- Processor Bus Speed constrained by load to
  - 100 MHz - 133MHz in Workstation Market
  - 50 MHz - 66MHz in the PC Market
- L2 Cache sits on the slow processor bus



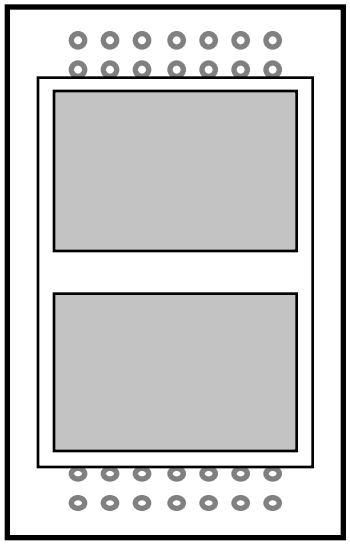
Emerging Back-Side L2 Architecture

- The **Emerging** CPU/ L2 Cache Architecture
- Processor Bus Speed constrained by load to
  - 100 MHz - 133MHz in Workstation Market
  - 50 MHz - 66MHz in the PC Market
- Cache Bus Speed
  - 133 MHz - 250 MHz in Workstation Market
  - 90 MHz - 133 MHz in the PC Market

Revolutionary
Pinout and Architecture
Late Write SRAM
in
Plastic BGA Package



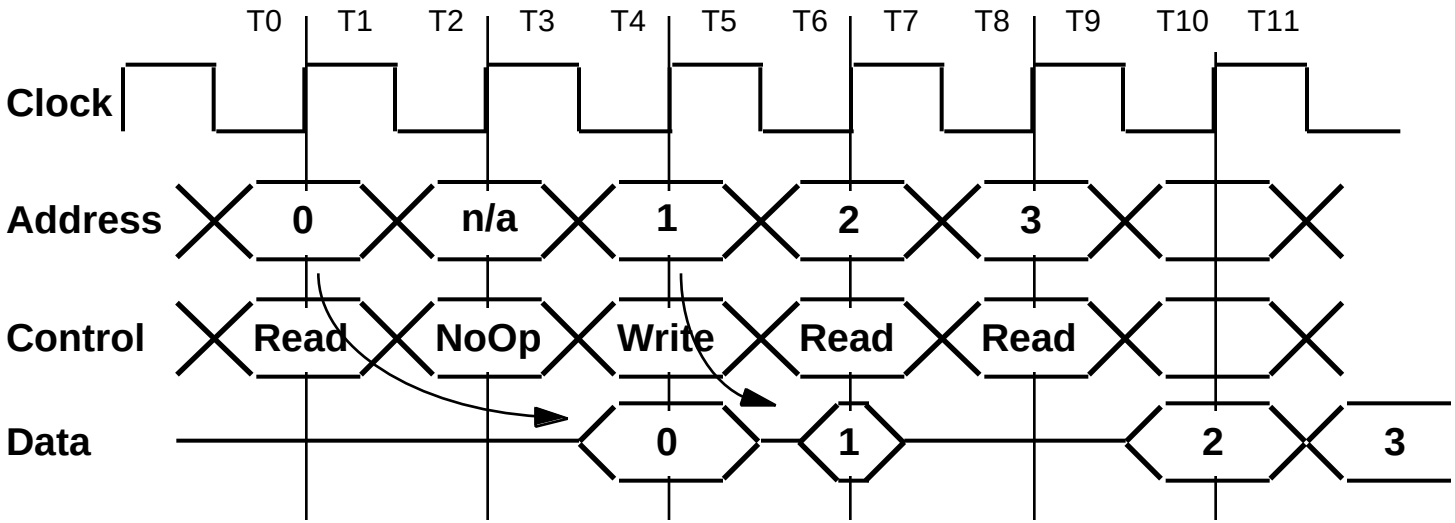
Bottom View



Top View

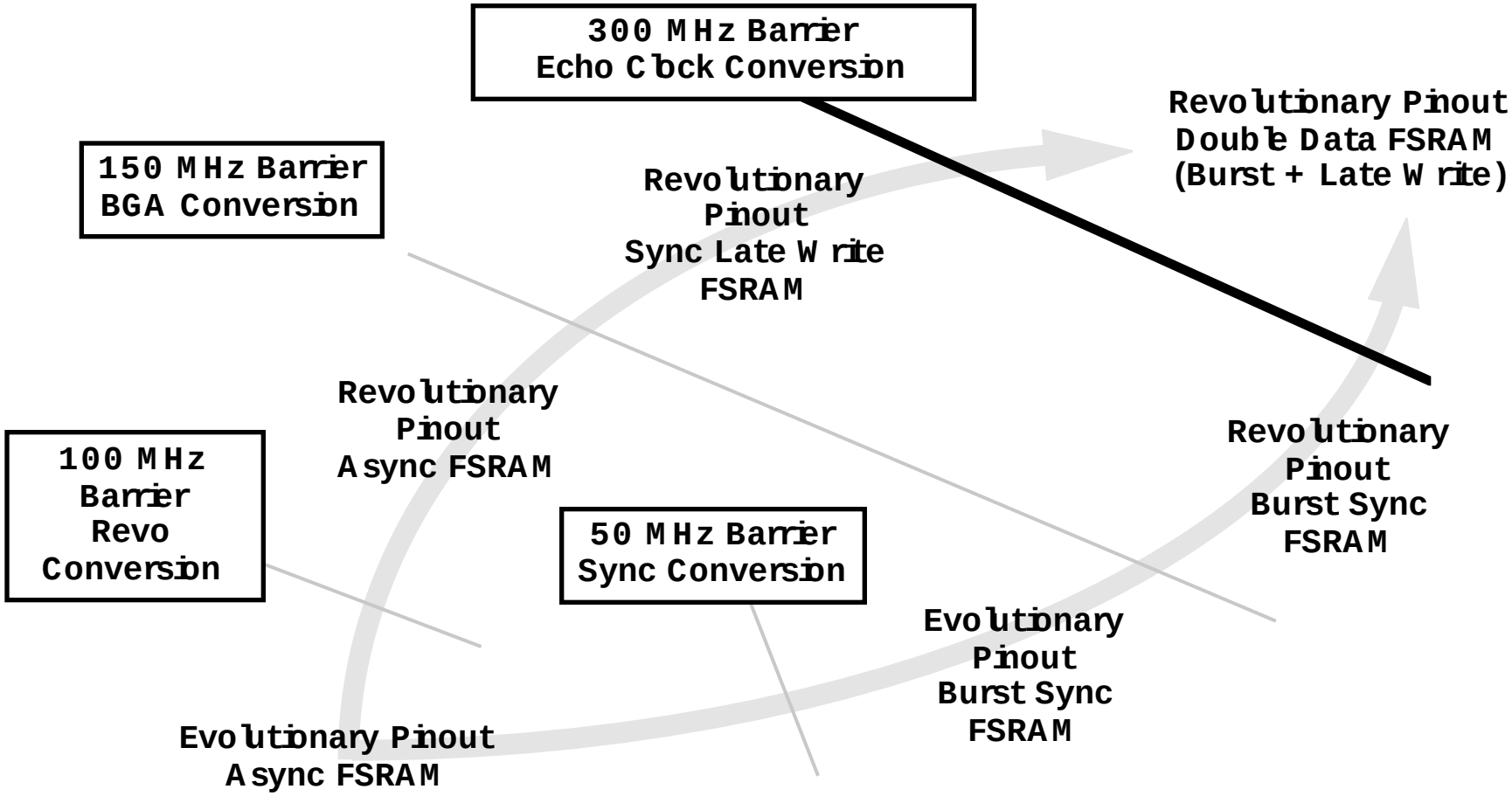
Note: Drawings not to scale

R/R Late Write Synchronous Read-Write-Read Sequence



Processor Bus Frequency	Processor Cycle Time	RAM Access Time Requirment	SRAM Type By Speed Range				
MHz	ns	ns					
16	60	30	Async				
20	50	25	•				
25	40	20	•				
33	30	15	•				
40	25	12.5	•	Revo Async	BurstRAM		
50	20	10		•	•		
58	17	8.5		•	•		
66	15	7.5		•	•		
83	12	6		•	•		
100	10	5			•		
125	8	4			•		
142	7	3.5			•	LW RAM	
166	6	3				•	
200	5	2.5				•	
250	4	2				•	
333	3	1.5					DDR RAM
285	3.5	1.75					•
333	3	1.5					•
400	2.5	1.25					•
500	2	1					•
666	1.5	0.75					

Cache SRAM Breakthroughs



Double Data Rate FSRAM Family

- 1Mb thru 16Mb
- x16,18,32,36
- Burst Sync
- 1.27mm Pitch
- 14mm x22mm Body
- PBGA Package
- HSTL I/O

Double Data Rate Synchronous FSRAM **Item 773**

1M thru 16M, x16/18/32/36

in 9x17 bump BGA, 50mil Pitch

	1	2	3	4	5	6	7	8	9
A	VSS	VDDQ	SA	SA	ZQ	SA	SA	VDDQ	VSS
B	DQ*	DQ	SA	VSS	B1	VSS	SA	DQ*	DQ
C	VSS	VDDQ	SA,NC	SA	G\	SA	SA,NC	VDDQ	VSS
D	DQ	DQ*	SA,NC	VSS	VDD	VSS	SA,NC	DQ	DQ*
E	VSS	VDDQ	VSS	VDD	VREF	VDD	VSS	VDDQ	VSS
F	DQ*	CQ	DQ*	VDD	VDD	VDD	DQ	CQ*	DQ
G	VSS	VDDQ	VSS	VSS	CK	VSS	VSS	VDDQ	VSS
H	DQ	DQ*%	DQ	VDD	CK\	VDD	DQ*	DQ%	DQ*
J	VSS	VDDQ	VSS	VDD	VDD	VDD	VSS	VDDQ	VSS
K	DQ*	DQ%	DQ*	VSS	B2	VSS	DQ	DQ*%	DQ
L	VSS	VDDQ	VSS	LBO	B3	MODE	VSS	VDDQ	VSS
M	DQ	CQ*	DQ	VDD	VDD	VDD	DQ*	CQ\	DQ*
N	VSS	VDDQ	VSS	VDD	VREF	VDD	VSS	VDDQ	VSS
P	DQ*	DQ	SA*	VSS	VDD	VSS	SA	DQ*	DQ
R	VSS	VDDQ	VDD	SA	SA1	SA	VDD	VDDQ	VSS
T	DQ	DQ*	SA	VSS	SA0	VSS	SA	DQ	DQ*
U	VSS	VDDQ	TDI	TMS	TCK	TRST	TDO	VDDQ	VSS

Top View Rev. 3.2 - 5/30/96

KEY

DQ* = NC for x16/18 version

CQ* and CQ* = NC on x16/18 version

SA* = NC for x32/36 version

DQ% and DQ*% = NC for x16/x32 version

Density Upgrades

x32/36	x16/18	3C	7C	7D	3D	BGA Package
1M	1M	NC	NC	NC	NC	14mmx22mm (MO-163)
2M	2M	**SA**	NC	NC	NC	14mmx22mm (MO-163)
4M	4M	**SA**	**SA**	NC	NC	14mmx22mm (MO-163)
8M	8M	**SA**	**SA**	**SA**	NC	TBD
16M	16M	**SA**	**SA**	**SA**	**SA**	TBD

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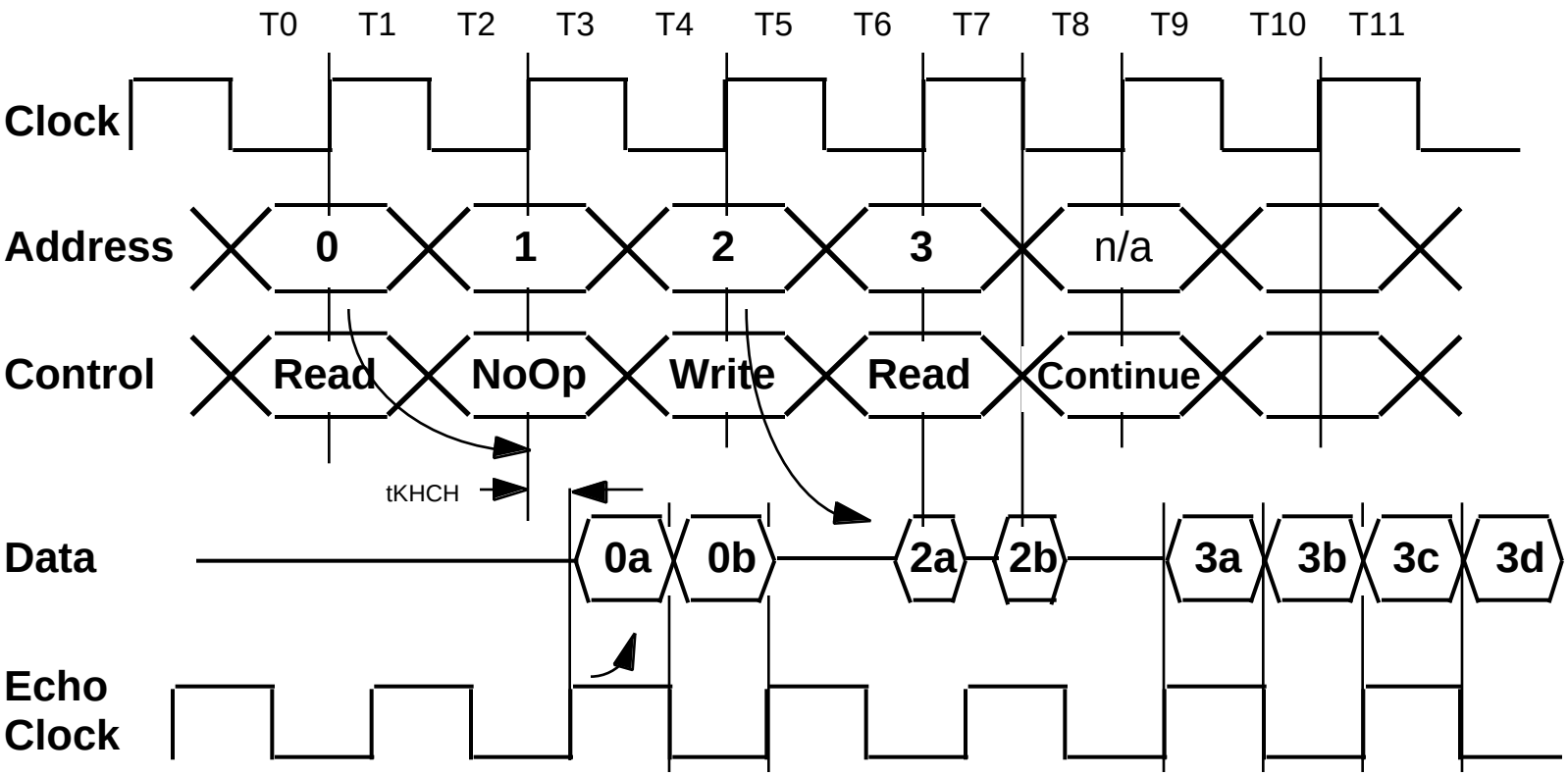
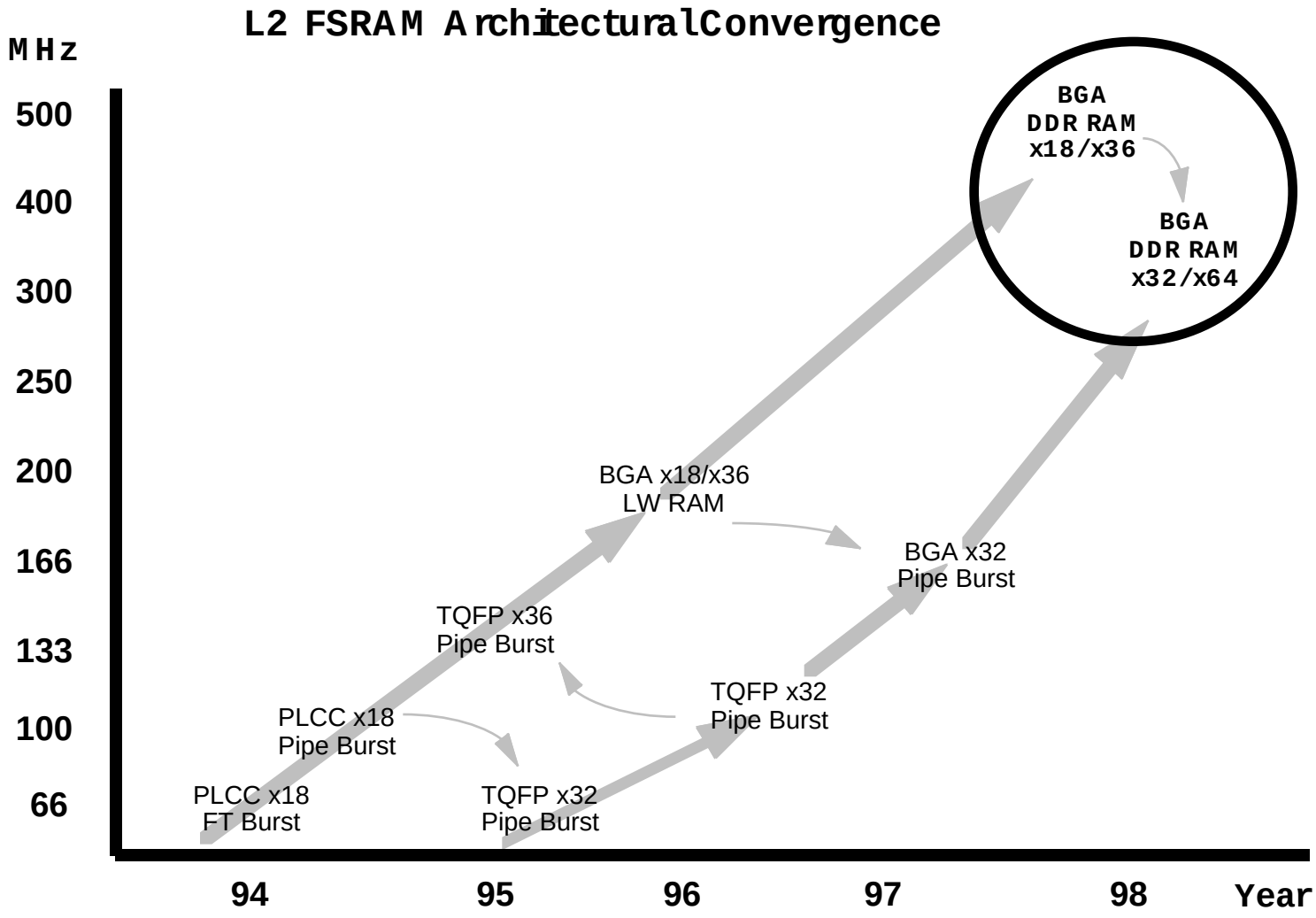
Double Data Burst Synchronous Read-Write-Read Sequence




L2 FSRAM Architectural Convergence
MHz
500
400
300
250
200
166
133
100
66
94
95
96
97
98
Year
BGA
DDR RAM
x18/x36
BGA
DDR RAM
x32/x64
BGA x18/x36
LW RAM
BGA x32
Pipe Burst
TQFP x36
Pipe Burst
TQFP x32
Pipe Burst
PLCC x18
Pipe Burst
PLCC x18
FT Burst
TQFP x32
Pipe Burst

The Quiet Revolution