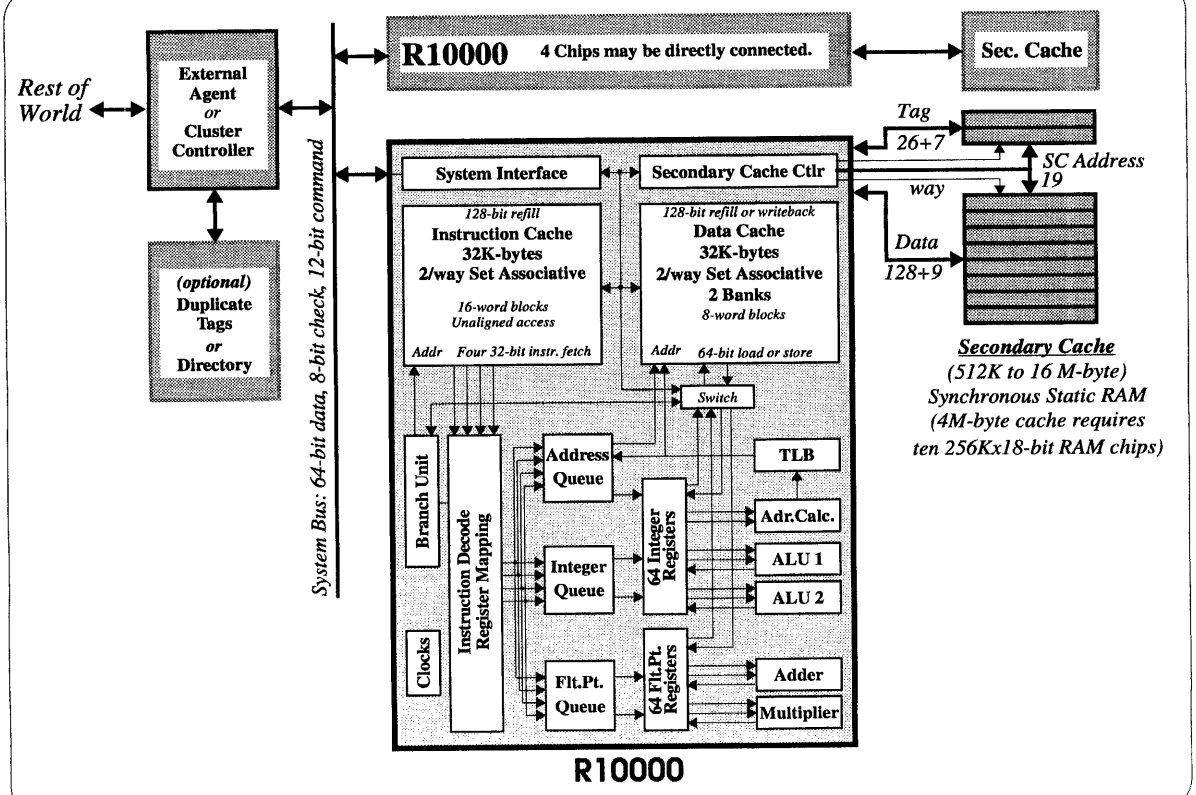
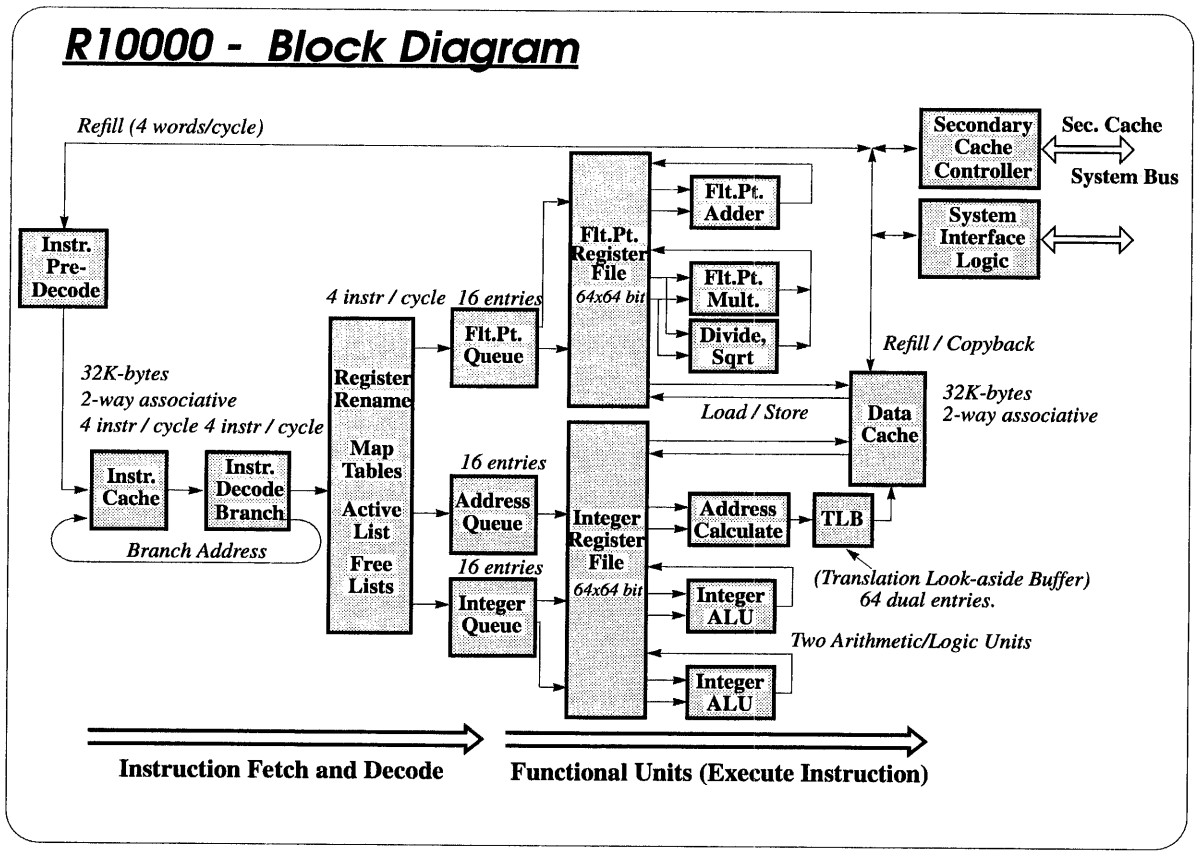
R10000 Superscalar Microprocessor

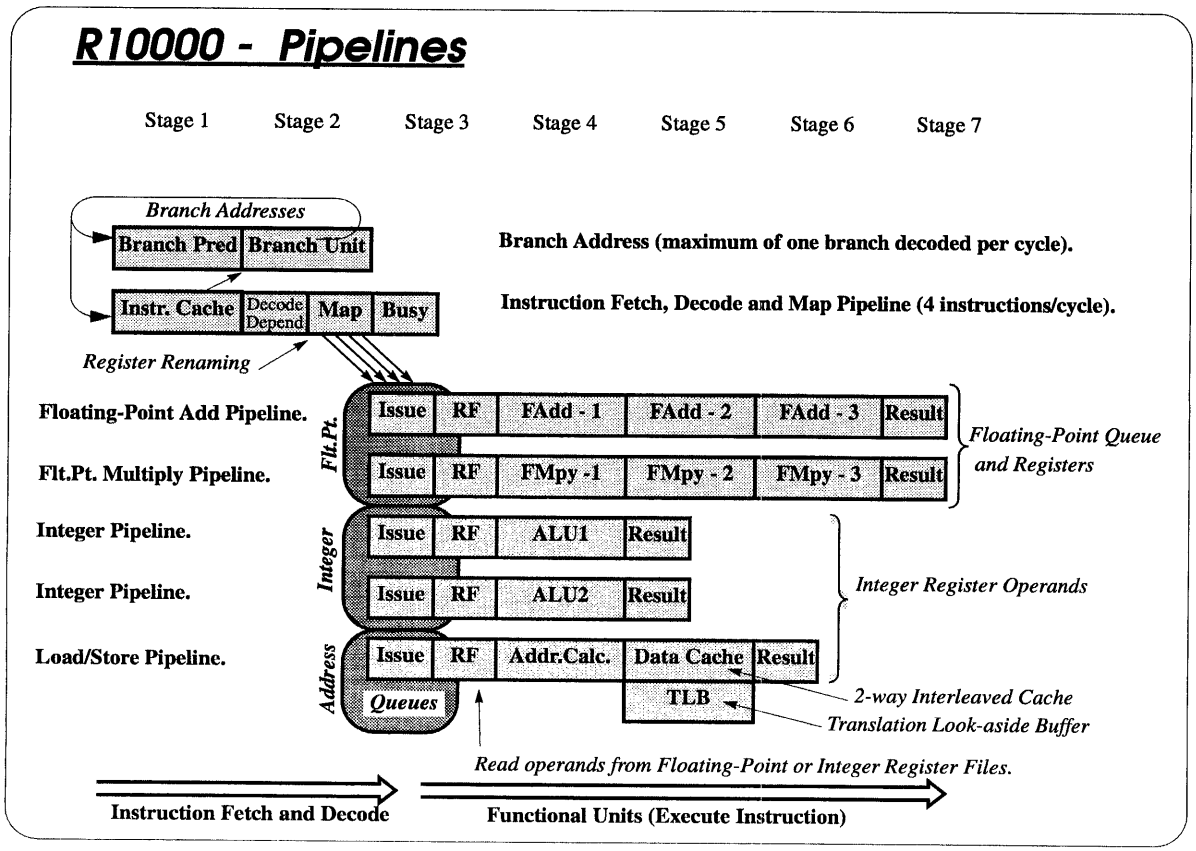
Ali Ahi, Yung-chin Chen, Robert Conrad, Randal Martin, Ratan Ramchandani, Mahdi Seddighnezhad, Greg Shippen, Hong-men Su, Hector Sucar, Nader Vasseghi, William Voegtli Jr., Kenneth Yeager, Yeffi

Presentation Outline

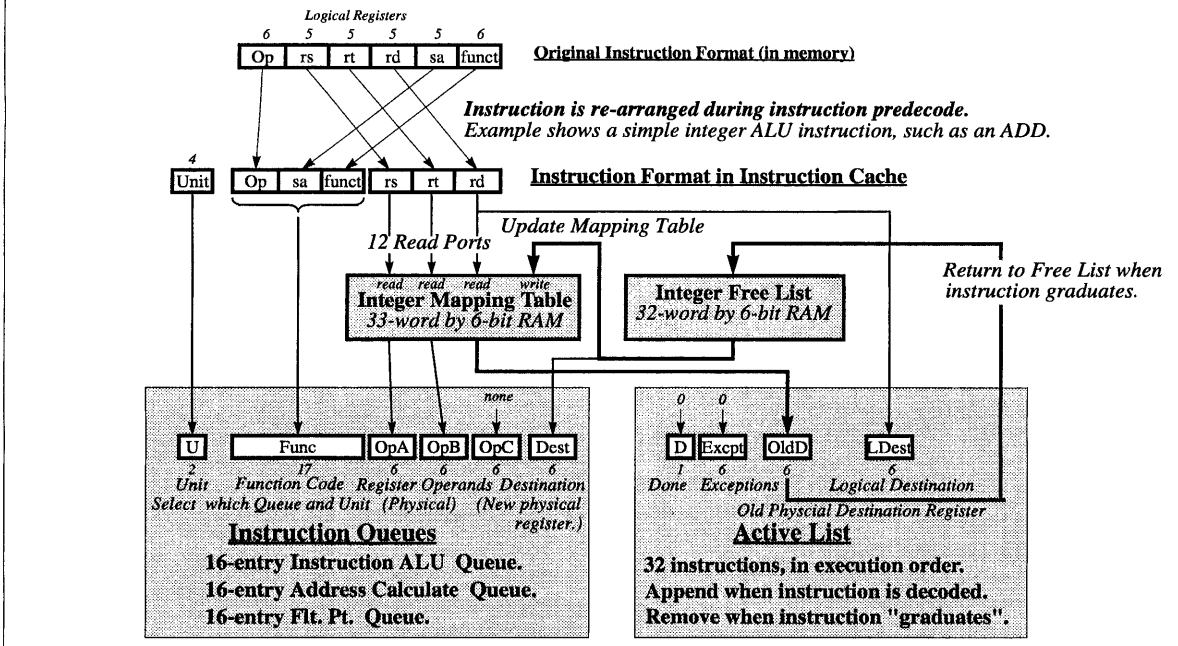
- Architecture of CPU and FPU
- Memory Hierarchy
- System Configuration
- Verification and Design Methods




R10000 - Block Diagram
Refill (4 words/cycle)
Secondary Cache Controller
Sec. Cache
System Bus
System Interface Logic
Instr. Pre-Decode
4 instr / cycle
16 entries
Flt.Pt. Queue
Flt.Pt. Register File
64x64 bit
Flt.Pt. Adder
Flt.Pt. Mult.
Divide, Sqrt
Refill / Copyback
32K-bytes
2-way associative
4 instr / cycle 4 instr / cycle
Register Rename
Map Tables
Active List
Free Lists
Load / Store
Data Cache
32K-bytes
2-way associative
Instr. Cache
Instr. Decode Branch
Branch Address
16 entries
Address Queue
16 entries
Integer Queue
Integer Register File
64x64 bit
Address Calculate
TLB
(Translation Look-aside Buffer)
64 dual entries.
Integer ALU
Two Arithmetic/Logic Units
Integer ALU
Instruction Fetch and Decode
Functional Units (Execute Instruction)


R10000 - Pipelines
Stage 1
Stage 2
Stage 3
Stage 4
Stage 5
Stage 6
Stage 7
Branch Addresses
Branch Pred
Branch Unit
Instr. Cache
Decode Depend
Map
Busy
Branch Address (maximum of one branch decoded per cycle).
Instruction Fetch, Decode and Map Pipeline (4 instructions/cycle).
Register Renaming
Floating-Point Add Pipeline.
Flt.Pt. Multiply Pipeline.
Integer Pipeline.
Integer Pipeline.
Load/Store Pipeline.
Flt.Pt.
Integer
Address
Issue
RF
FAdd - 1
FAdd - 2
FAdd - 3
Result
Issue
RF
FMpy -1
FMpy - 2
FMpy - 3
Result
Floating-Point Queue and Registers
Issue
RF
ALU1
Result
Issue
RF
ALU2
Result
Integer Register Operands
Issue
RF
Addr.Calc.
Data Cache
Result
Queues
TLB
2-way Interleaved Cache
Translation Look-aside Buffer
Read operands from Floating-Point or Integer Register Files.
Instruction Fetch and Decode
Functional Units (Execute Instruction)

Register Renaming



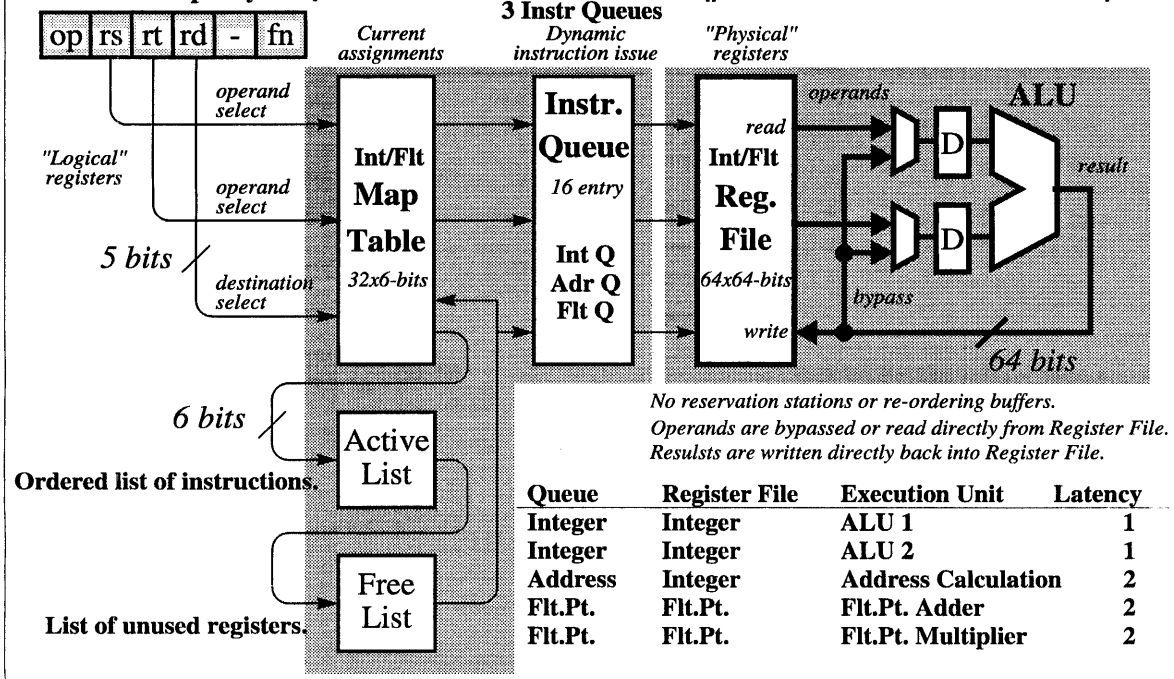
During any cycle, each physical register number is either in Mapping Table, Active List, or Free List.

Control Paths

Register Renaming 6-bit Control Logic

Five Execution Units 64-bit Data Path

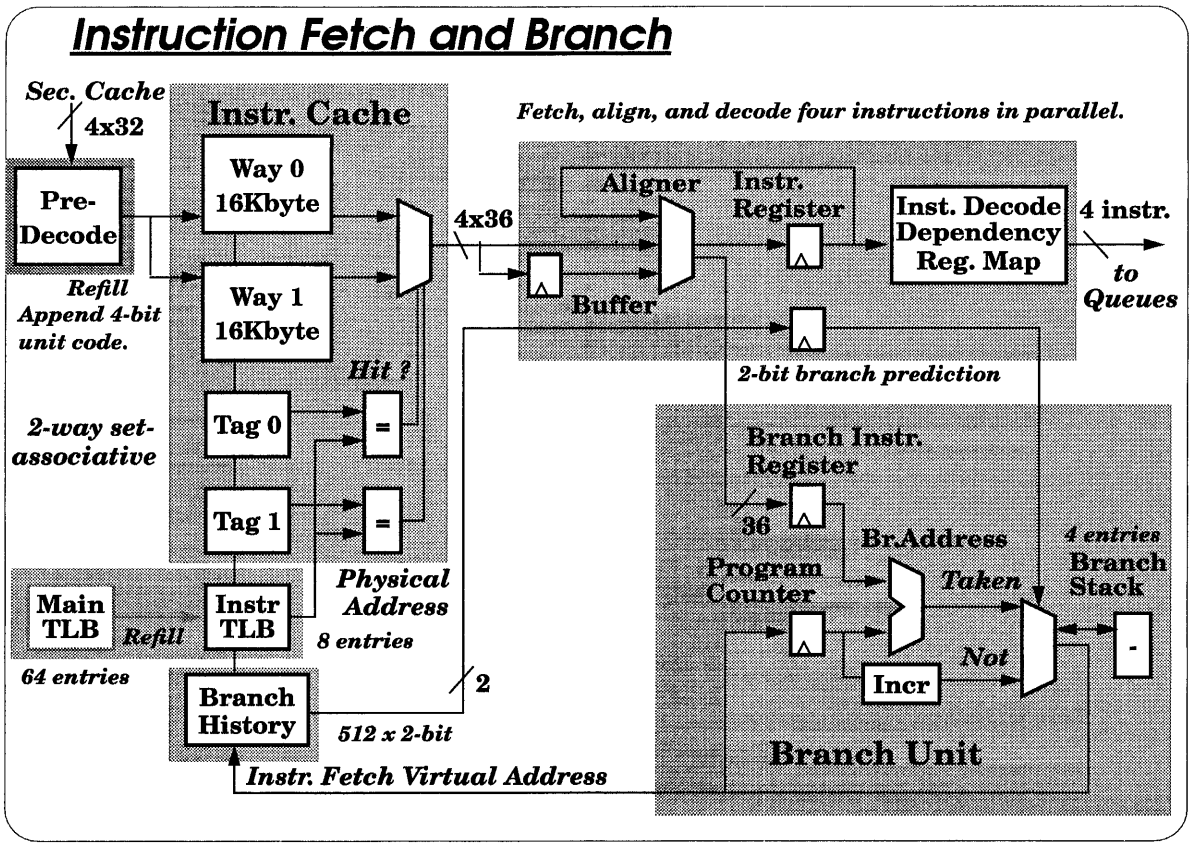
Fetch and Decode
4 Instructions per cycle



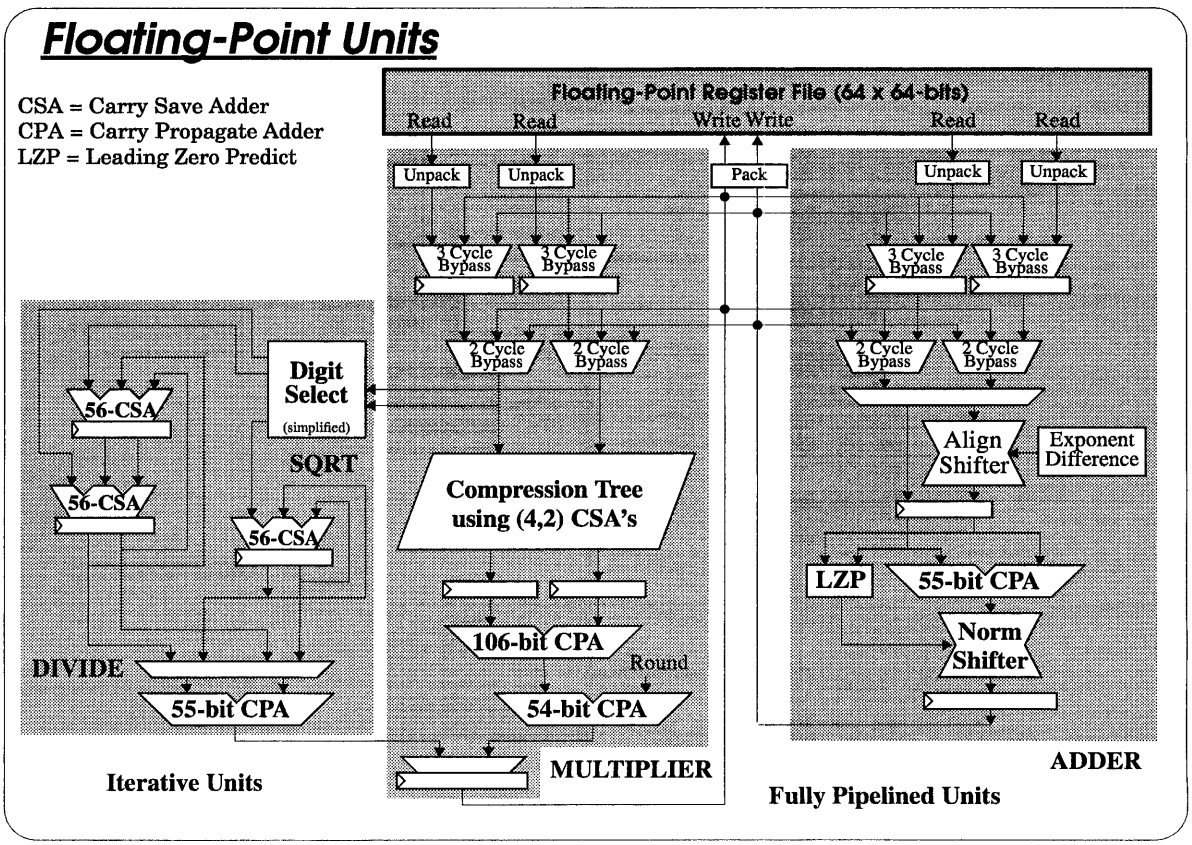
No reservation stations or re-ordering buffers.
Operands are bypassed or read directly from Register File.
Resulsts are written directly back into Register File.

Queue	Register File	Execution Unit	Latency
Integer	Integer	ALU 1	1
Integer	Integer	ALU 2	1
Address	Integer	Address Calculation	2
Flt.Pt.	Flt.Pt.	Flt.Pt. Adder	2
Flt.Pt.	Flt.Pt.	Flt.Pt. Multiplier	2

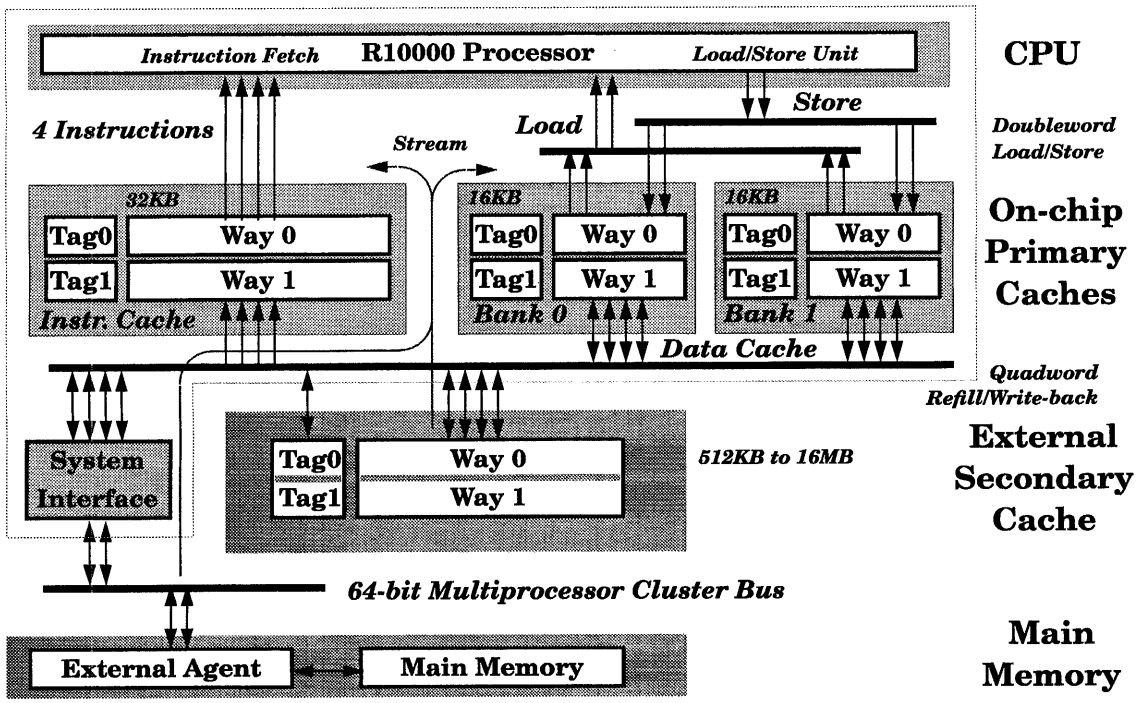
7.4-07


Instruction Fetch and Branch
Sec. Cache
4x32
Instr. Cache
Fetch, align, and decode four instructions in parallel.
Pre-Decode
Way 0 16Kbyte
Way 1 16Kbyte
Refill
Append 4-bit unit code.
4x36
Aligner
Instr. Register
Buffer
Inst. Decode Dependency Reg. Map
4 instr.
to Queues
2-bit branch prediction
Hit ?
2-way set-associative
Tag 0
Tag 1
=
=
Branch Instr. Register
36
Br.Address
4 entries
Branch Stack
Program Counter
Taken
Not
Incr
-
Main TLB
Refill
64 entries
Instr TLB
Physical Address
8 entries
Branch History
2
512 x 2-bit
Branch Unit
Instr. Fetch Virtual Address

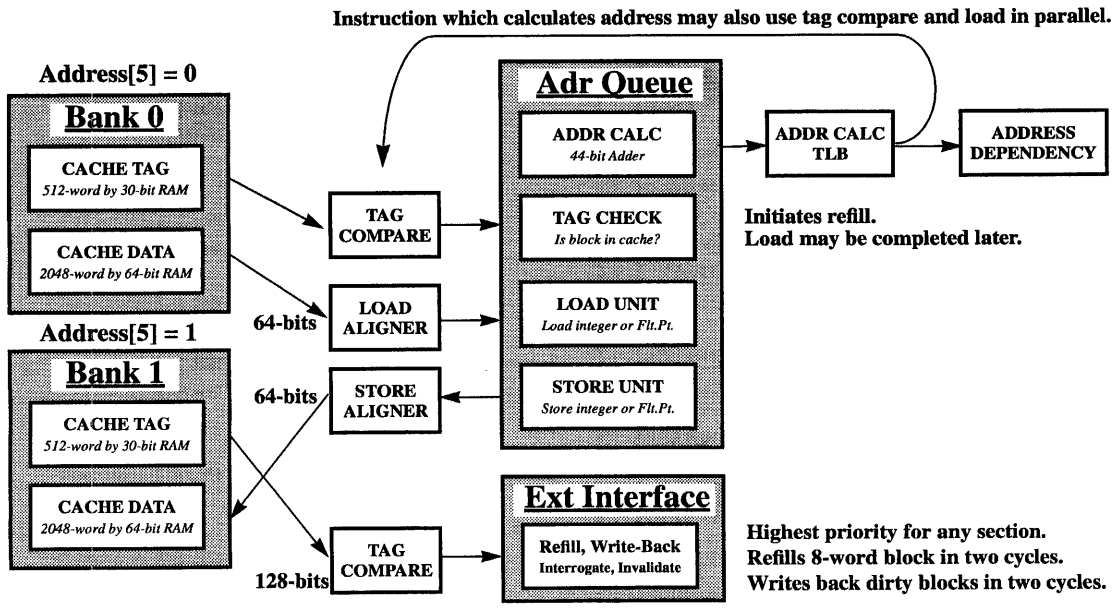
7.4-08


Floating-Point Units
CSA = Carry Save Adder
CPA = Carry Propagate Adder
LZP = Leading Zero Predict
Floating-Point Register File (64 x 64-bits)
Read
Read
Write
Write
Read
Read
Unpack
Unpack
Pack
Unpack
Unpack
3 Cycle Bypass
2 Cycle Bypass
Digit Select
(simplified)
56-CSA
SQRT
Compression Tree using (4,2) CSA's
Align Shifter
Exponent Difference
LZP
55-bit CPA
Norm Shifter
106-bit CPA
Round
54-bit CPA
DIVIDE
55-bit CPA
MULTIPLIER
ADDER
Iterative Units
Fully Pipelined Units

R10000 Memory Hierarchy



Parallelism in Data Cache

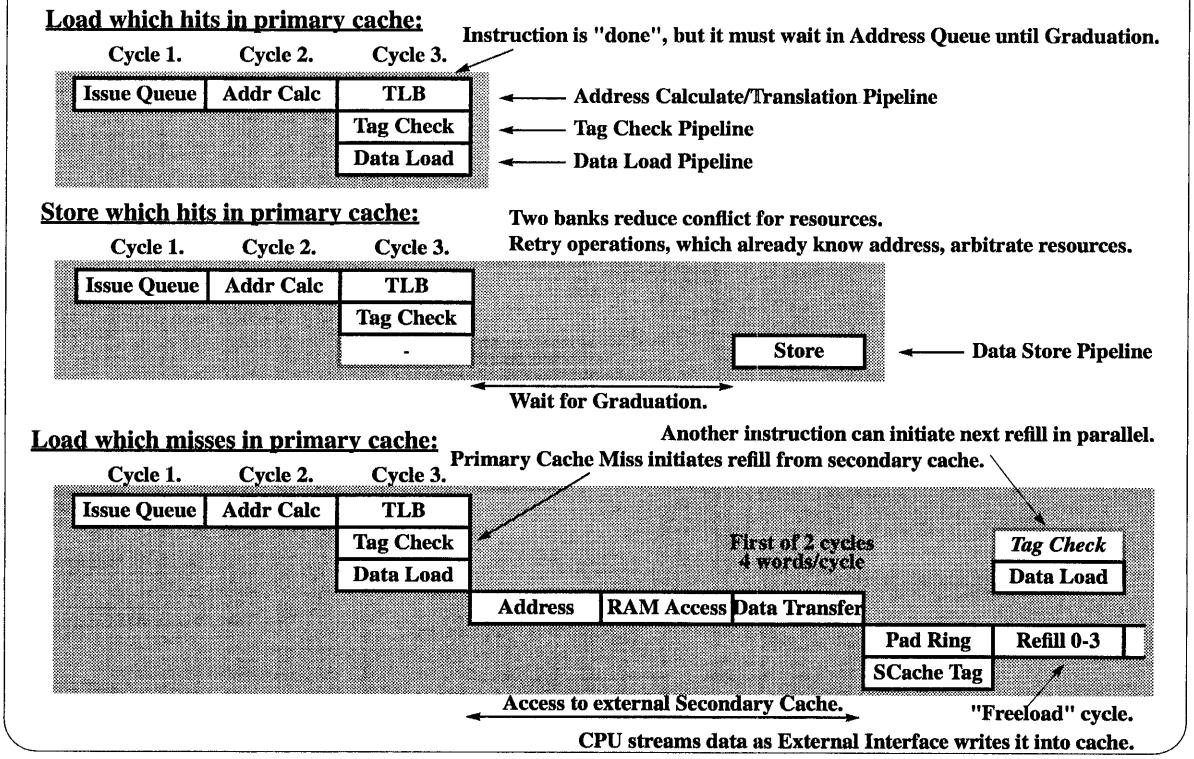


Four sections can be independently allocated.
CPU accesses are 64 bits wide, 2-way associative.
Refill and write-back are 128 bits wide. (Way is known.)

Five control units can operate in parallel, if resources do not collide.

7.4-11

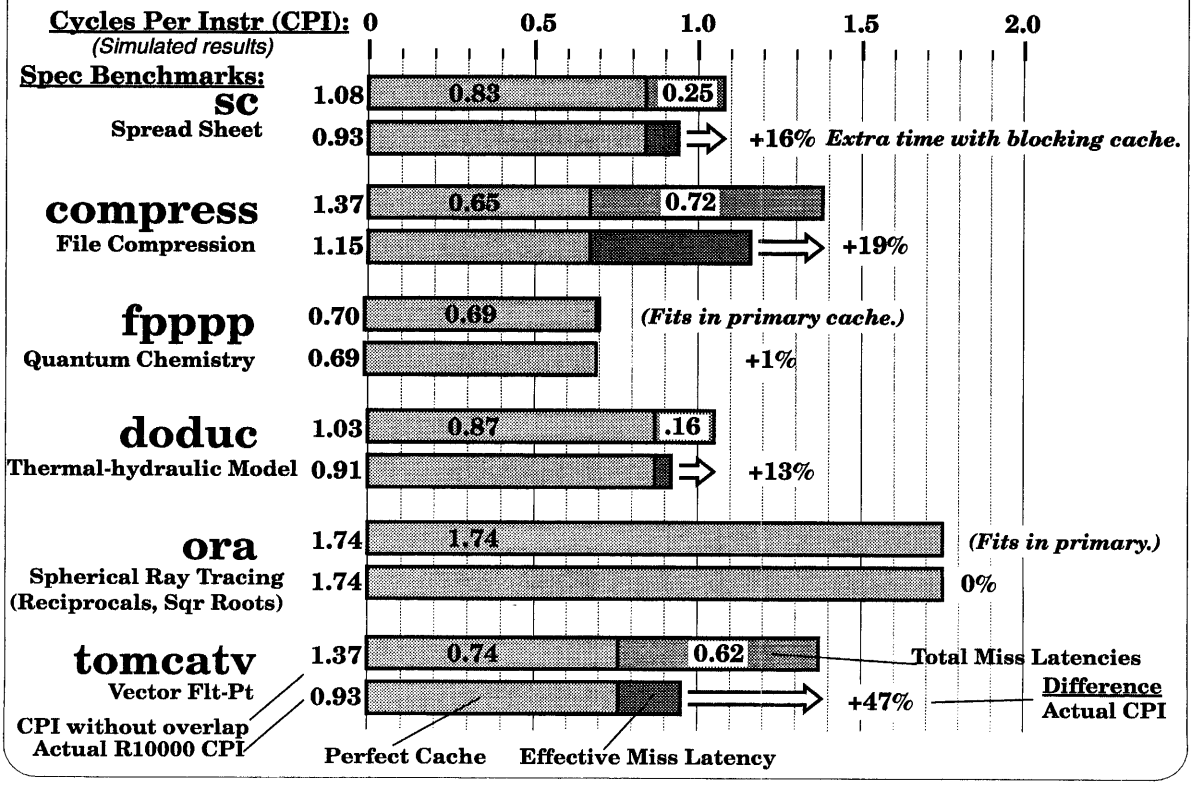
Data Cache Pipelines



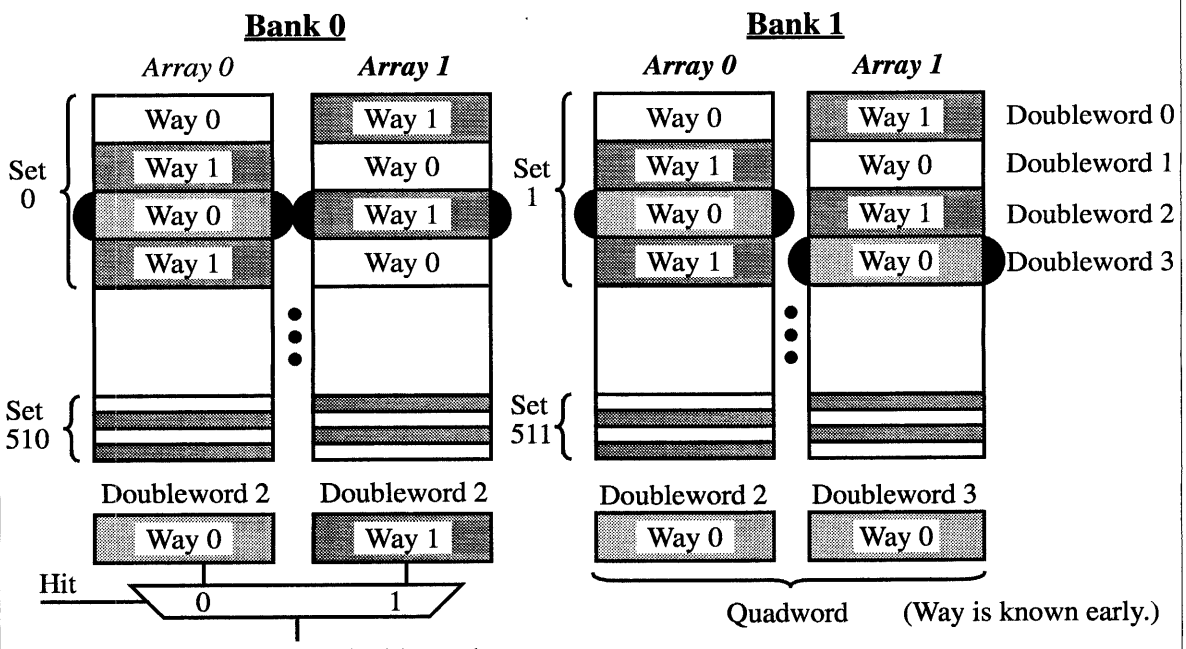
7.4-12

Non-blocking Cache

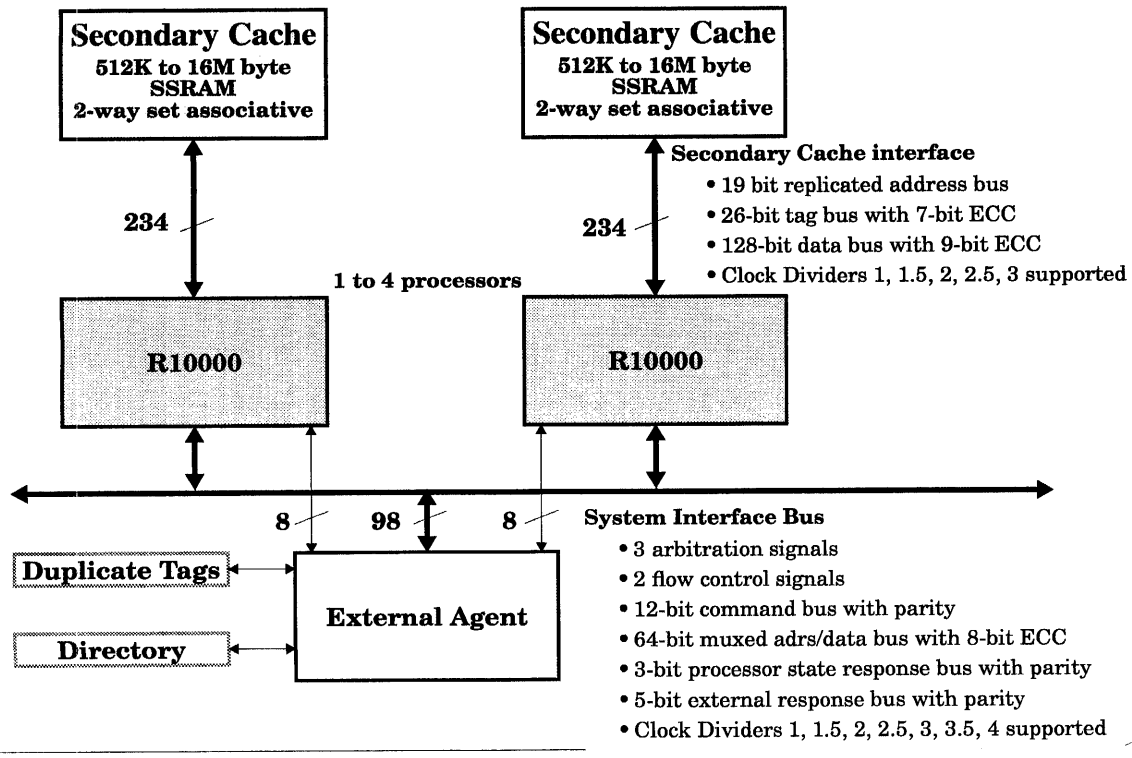
Concurrent refill times reduce effective cache latency.



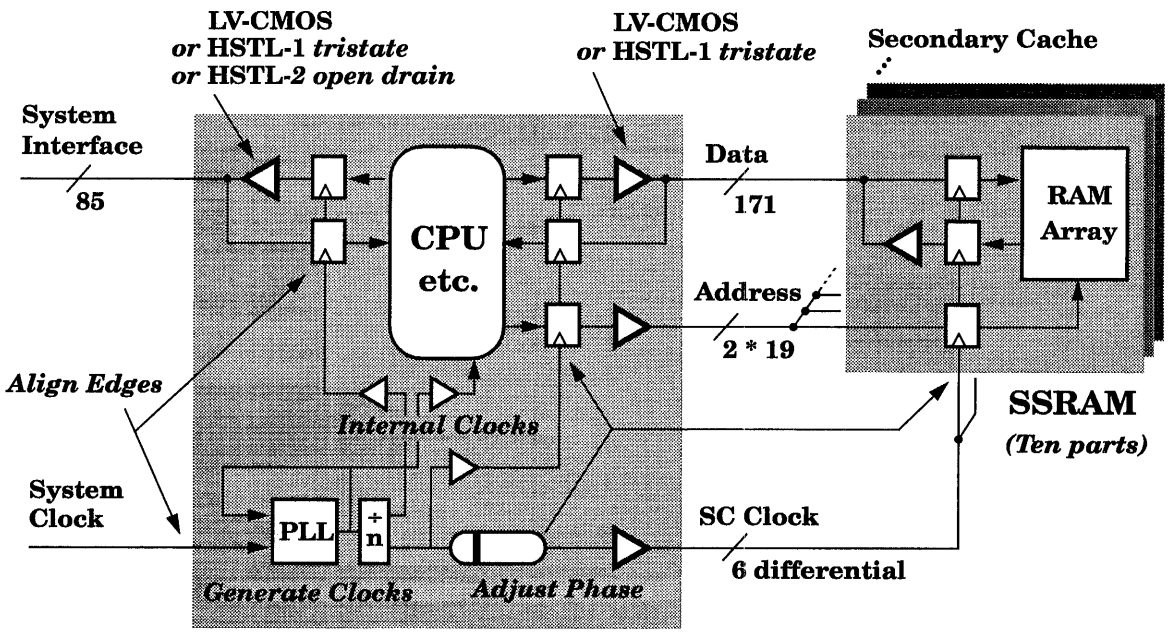
Data Cache Interleaving



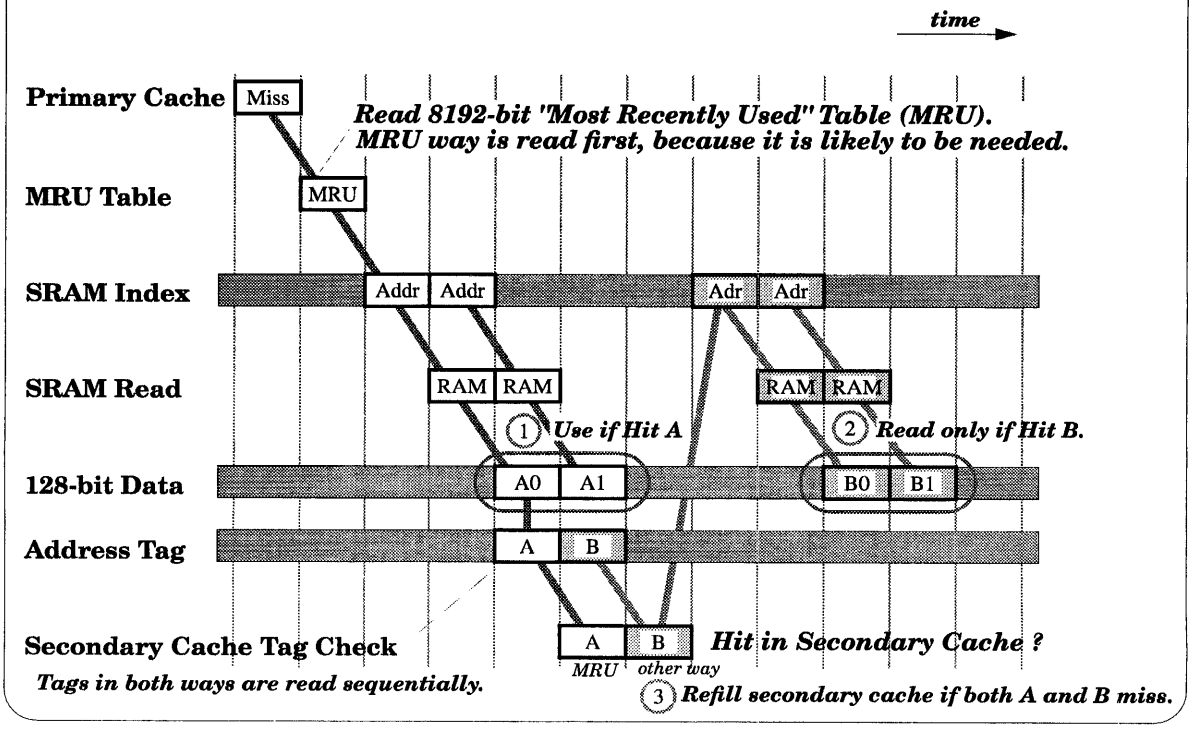
System Configurations



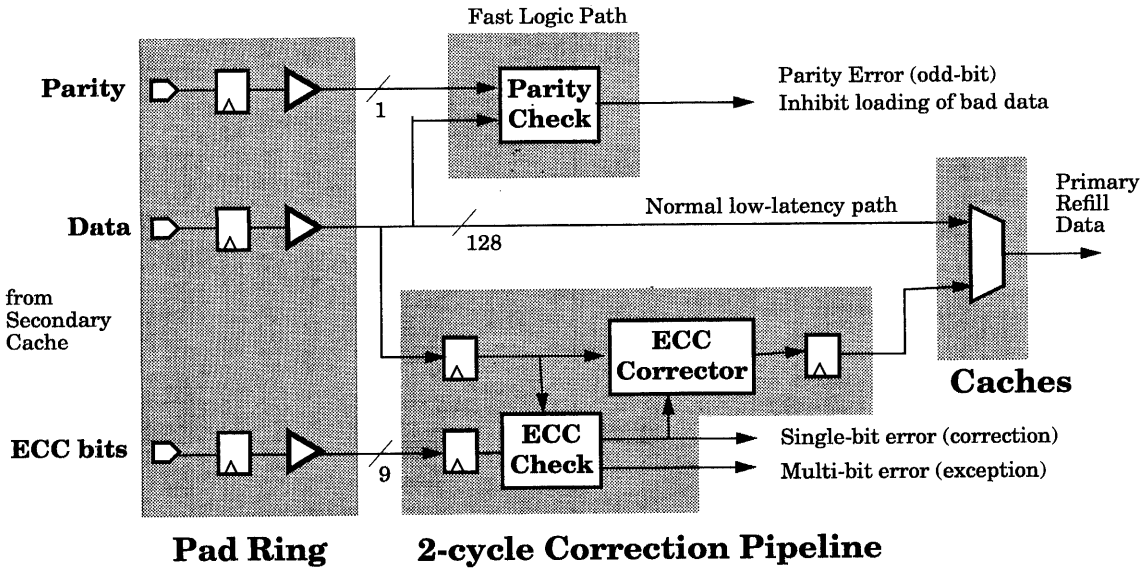
Clocks and Output Drivers



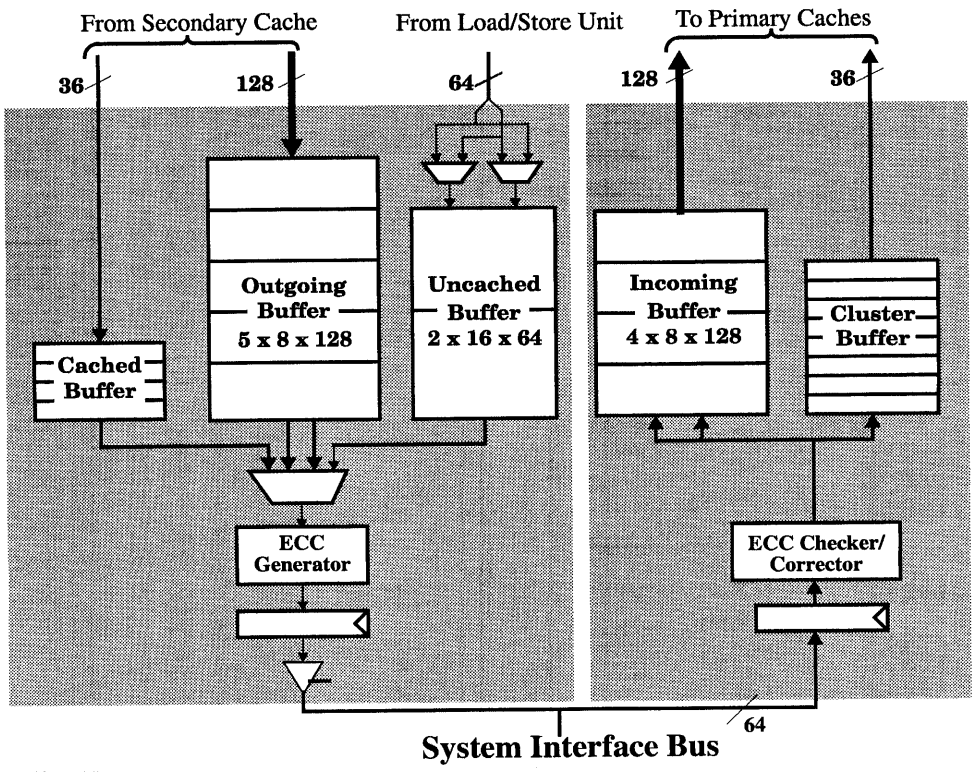
Refill from Set-Associative Secondary Cache



Secondary Cache Error Protection



System Interface Block Diagram



7.4-19

Functional Verification Methodology

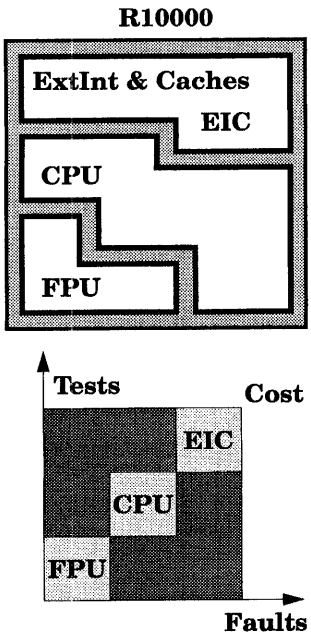
- Tools and environment:
  - Inhouse HDL and simulator with backup and replay.
  - Graphical user interface for simulation and regression.
  - An instruction level simulator as a reference machine, which checks
    - Architecture registers
    - Memory hierarchy
  - Programmable random code generators for UP and MP.
  - Arc coverage and consistency checking for state machines.
- C-based System Model supports
  - Secondary cache array, memory controller and array, bus controller.
  - Bus protocol checking.
  - External events :
    - programmable or purely random
    - imbeded in diagnostics for fine-grain control
  - 1 to 4 processor configuration.

7.4-20

Diagnostic Development

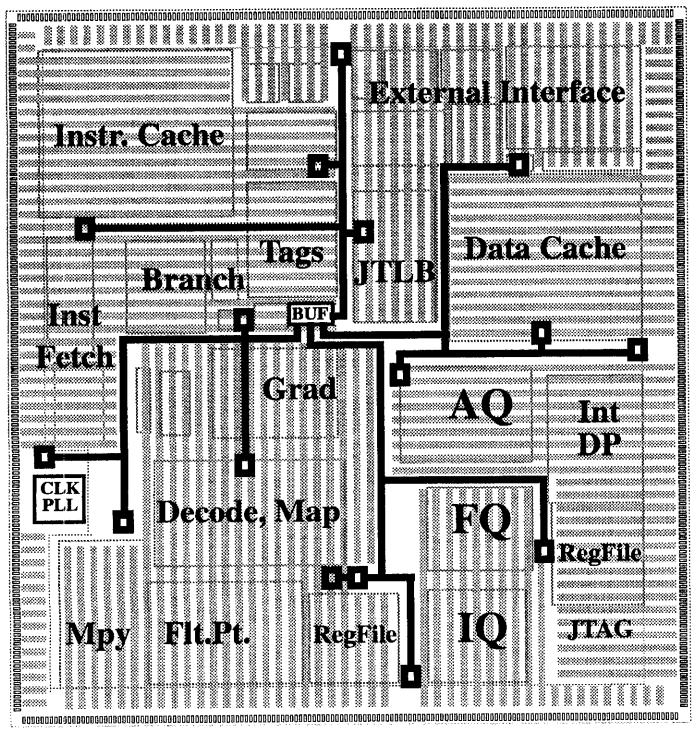
- Directed Diagnostics
  - Architecture Verification Programs (AVP)
  - Microarchitecture Verification Programs (MVP)
  - Implementation Verification Programs (IVP)
- Random Diagnostics From Programmable Random Code Generators
  - Functional unit intensive
  - Load/Store intensive
  - Branch intensive
  - Mix of the above under UP and MP environments
- Diags are self-checking and/or compared with the reference machine.
- UP and MP applications.
- Booting O/S's on R10000 RTL : 2 Unix O/S's and NT.

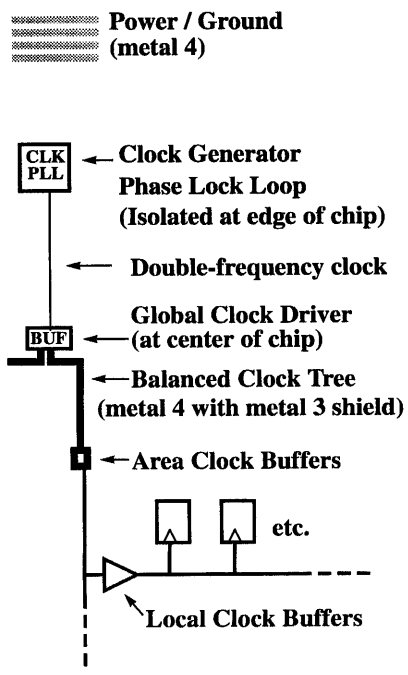
Test Features



- On-chip virtual output pins:
  - Physical design partitioning
  - Direct observability of internal signals
  - Signature compression through LFSRs (Linear-Feedback Shift Register)
- Dedicated test structures:
  - No performance impact
  - No logic design overhead
  - No special clock requirements
- Enhanced debug and diagnostics:
  - Cycle-by-cycle sampling of internal signals
  - Observed signals correlate to logic specification
  - Signature analysis
- Test cost reduction:
  - No special ATE requirements
  - Internal test-output compression by signature
  - Test and fault partitioning.
  - Reduced test time and higher fault coverage

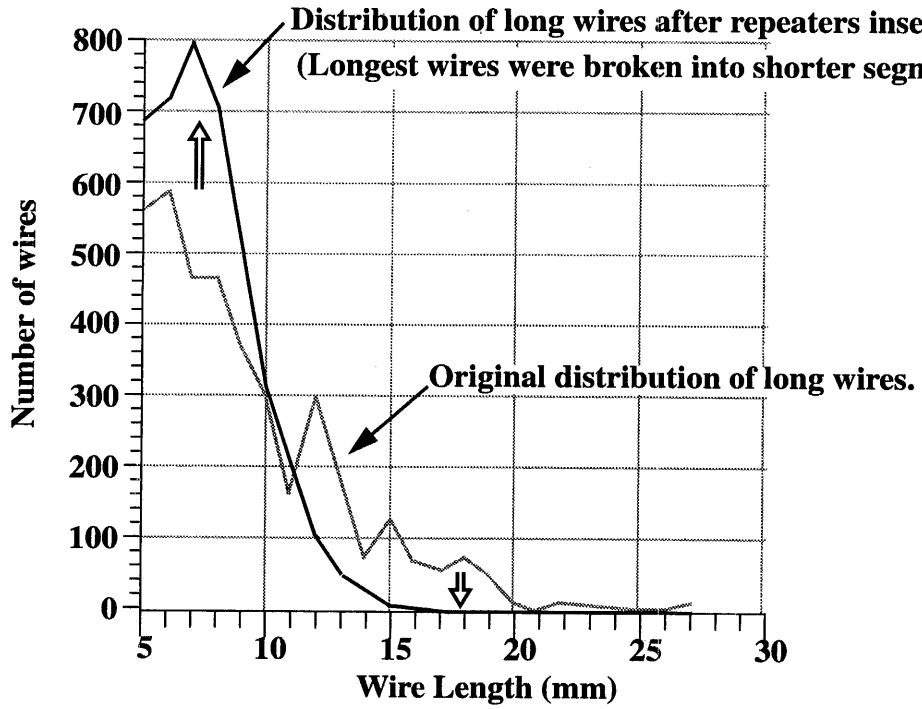
Clock and Power Distribution





7.4-23

Signal Repeaters on Long Wires



7.4-24

R10000 Die Photo

This sheet shows physical placement of major blocks.
(Full color photo slide will be shown at Hot Chips.)