Smaller, Faster, Cooler...
Evolving The PowerPC Family

Doug Balser
Somerset Design Center

IBM

Agenda

- PowerPC ISA
- 1995 Commitments
- Design Methodology
- Portable Design Characteristics
- 603ev Design Point
  - Design features
  - Block diagram
  - Instruction pipeline / latencies
  - Technology
  - Specifications
  - Competitiveness

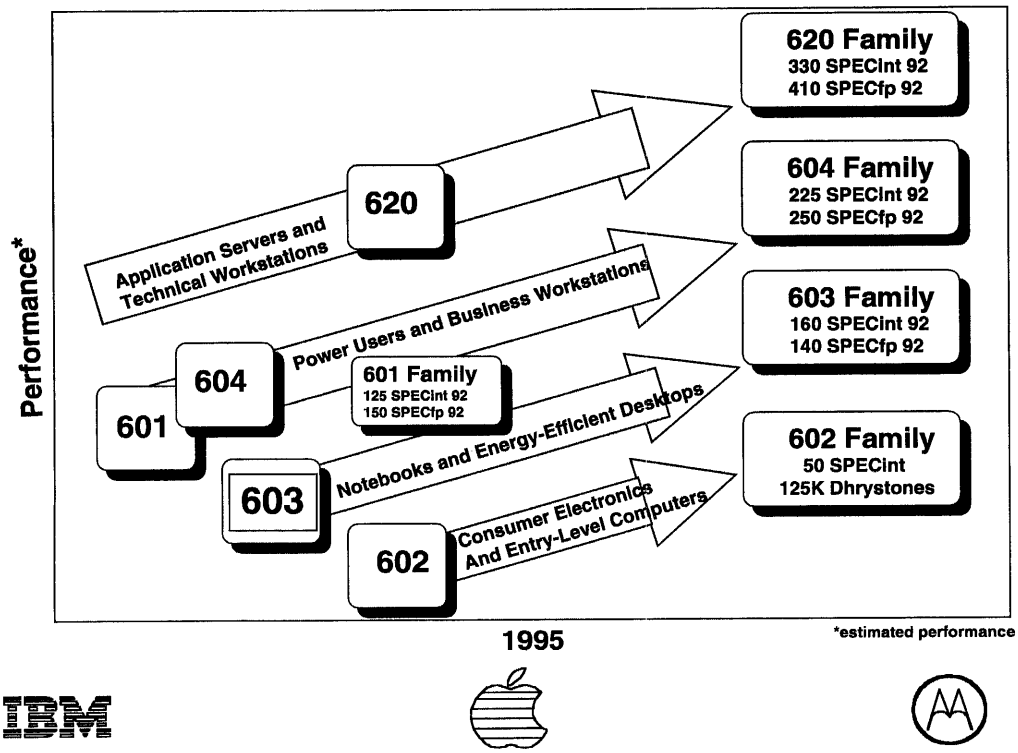
IBM

Instruction Set Architecture

- Jointly Derived by IBM / Apple / Motorola
- Maintained The ABI With POWER
- Simplify Architecture
  - More appropriate for low-cost single chip microprocessors
- Eliminate Instructions That Impede Clock Rates
- Remove Architecturally Imposed Barrier To:
  - Superscalar dispatch
  - Out-of-order execution
- New Features
  - Multi-processing support
  - Extension to 64 bits
  - Bi-endian support

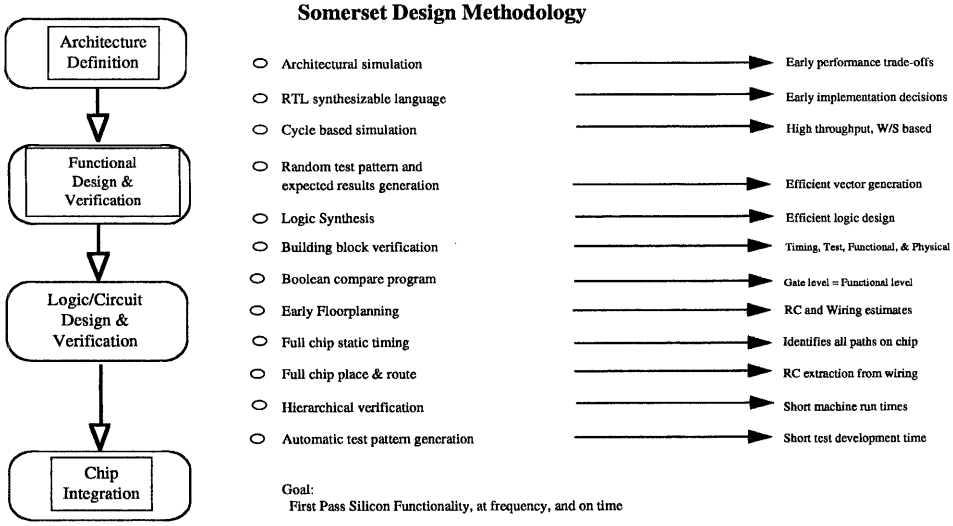
IBM

1995 Commitments

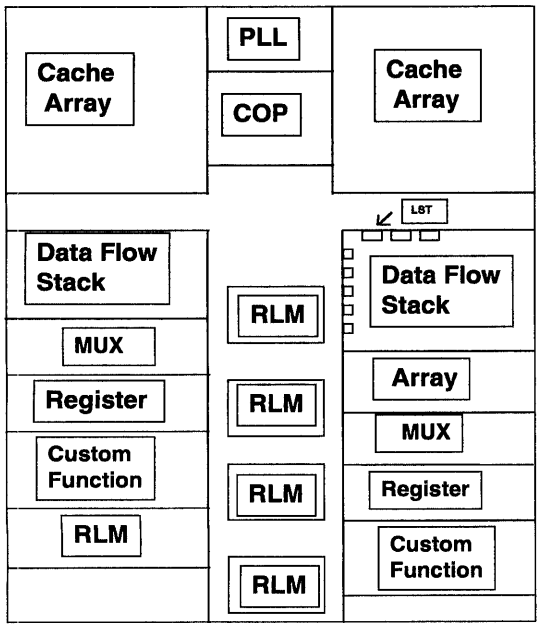


IBM

Design Methodology



Design Methodology



Arrays - Tags, TLB, BTAC, Etc..

PLL - Phase Lock Loop

COP - Common On Chip Processor
- **» JTAG**
- **» LSSD Control**

RLM - Random Logic Macro
- **» Control Logic**

Super macro - Collection of Custom, RLM, Wiring Cells

LST - Logic Service Terminal

7.3-07

Design Methodology

- Overall Design Objective
  - 1st pass silicon functionality at performance
  - Design on schedule
- Flexible Design Methodology
  - Vary degree of customization to meet schedule/performance objectives
  - Early design performance trade-off's
  - Early cycle time determination (estimated values)
  - Early floor planning
- Building Block Approach
  - Standard cells for control logic (book)
  - Custom-off-the-shelf data flow macros (ots)
  - Full custom arrays and cycle time critical circuits (custom ots)
- Rules Based
- Two Primary Views of Chip
  - Logical
  - Physical



7.3-08

Design Methodology

- Floorplanning/Chip Construction
  - Rule based
  - Hierarchical
  - RC estimates for timing
    - » early timing estimates
    - » based on real physical constraints
    - » refined as design progresses
  - Pre-wires for critical areas
  - Auto-route program incorporates pre-wires
- Static Timing Analysis
  - All possible chip paths analyzed
  - Report of path slacks from target cycle time
- Design For Test
  - Level sensitive scan design (LSSD)
  - Automatic test pattern generation (ATPG)
  - Built in self-test (BIST)



Portable Design Characteristics

- **Aggressive Performance**
  - **lags the desktop by 12 mths**
- **Low Power**
  - **under 3 watts**
- **Cost Sensitive**
  - **under 100 mm²**
- **Versatile**
  - **wide range of system configurations**

IBM

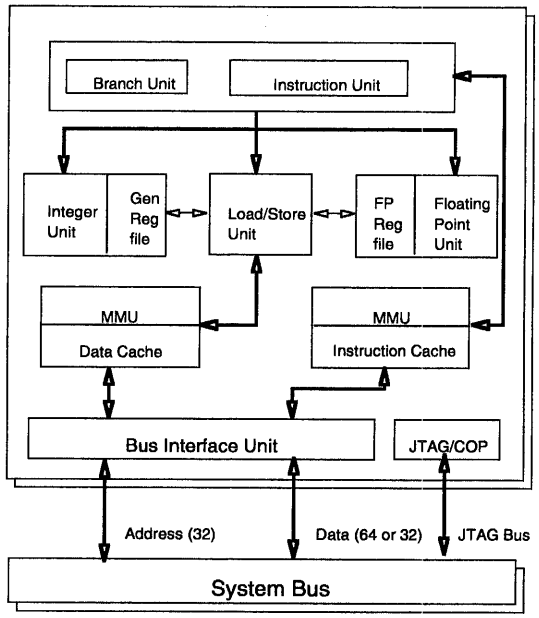
Design Features

- **Increased Cache Size Over PPC603**
- **Support For Non-integer Bus Clock Multiples**
- **5 Volt Tolerant I/O**
- **Unaligned Little Endian Support**
- **Hit Under Miss On I-cache**
- **Improved Divide Performance**
- **Simplified Memory Addressing (No PIO)**
- **Power Management**
- **Improved Clocking**

IBM

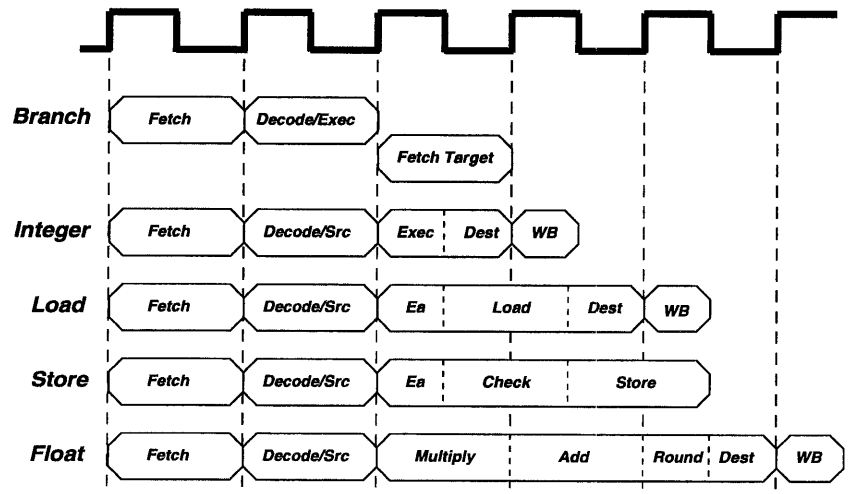
7.3-11

Block Diagram

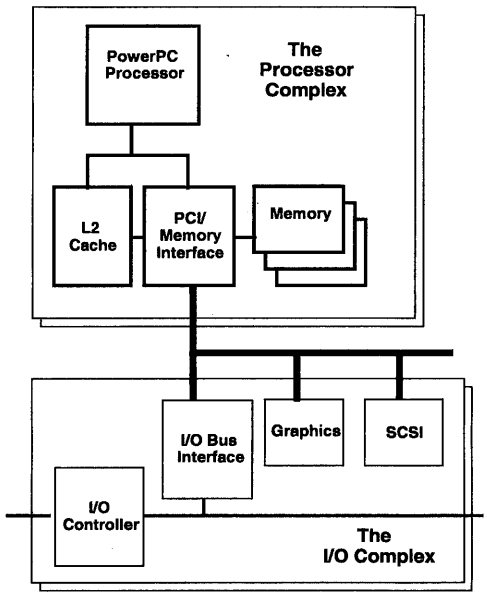


7.3-12

Instruction Pipeline



System Configuration



Power Management

- **Dynamic Power Management**
  - **Inactive units are not clocked**
- **Static Power Management:**
  - **Doze: timers, snooping only**
  - **Nap: timers only**
  - **Sleep: no clocks**

7.3-15

Process Technology

- .5u Nwell CMOS
- Five Level Metal
- Local Interconnect
- L_{eff} = 0.25um
- 2.5v Core Voltage
- 3.3v Receivers / Drivers



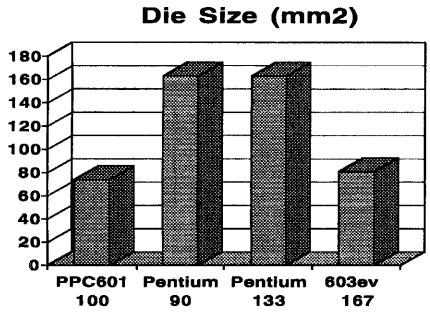
7.3-16

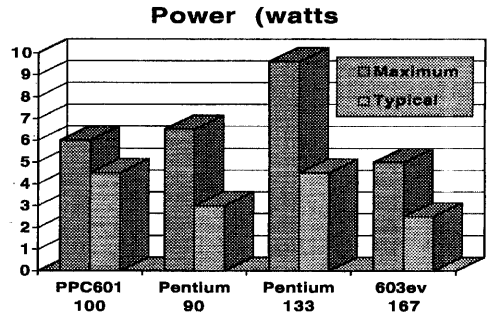
Specifications

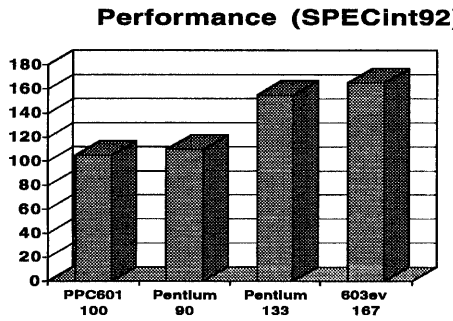
- Superscalar Low Power RISC Processor
- 16K Instruction Cache, 16K Data Cache
- 165 SPECint92 at 167 MHz (*estimated*)
- 81 sq mm. Die Size
- 2.6 Million Transistors
- 2.5w Typical Power at 167 MHz (*estimated*)
- 165 I/O Signals, CMOS/TTL Compatible
- LSSD Design, JTAG Compliant
- Quad Flat Pack & Ball Grid Array Packages



Competitiveness

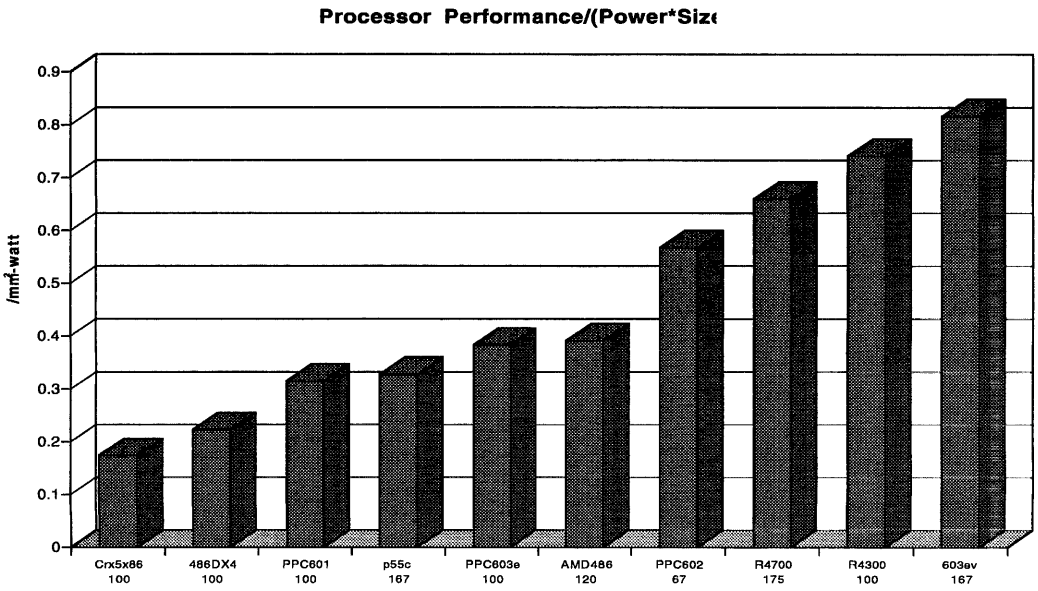






IBM

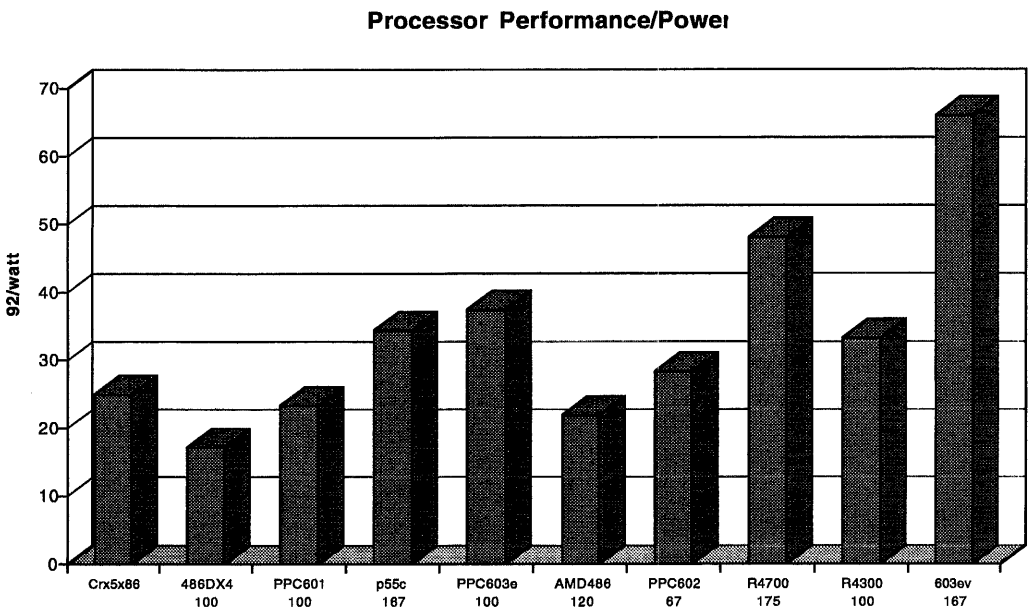
Competitiveness



IBM

7.3-19

Competitiveness



IBM

7.3-20

Summary

603ev Processor

- **Fully Functional First Pass Silicon**
- **Rapid Market Introduction**
  - **highly compatible design**
  - **samples in 4Q95, production in 1Q96**
- **High Performance**
  - **165 SPECint92, 150 SPECfp92 (estimated)**
- **Low Power**
  - **2.5w typical (estimated)**
  - **doze / nap / sleep power saving modes**
- **Low Cost**
  - **small die size**
  - **proven technology**

IBM