A 150MHz Superscalar RISC Processor with Pseudo Vector Processing Feature

Koji Saito, Masahiro Hashimoto, Hideo Sawamoto,
Ryo Yamagata, Takashi Kumagai, Eiki Kamada,
Kenji Matsubara, Toshiko Isobe*, Takashi Hotta,
Tetsuo Nakano, Teruhisa Shimizu, Kisaburo Nakazawa**

Hitachi, Ltd.
* Hitachi Computer Engineering Co.,Ltd.
** University of Tsukuba

Presentation Outline

- Design Goals
- Pseudo Vector Processing Feature
- Processor Overview
- Performance
- Physical Characteristics
- Summary

Design Goals

- Competitive Performance
- Implementation of Pseudo Vector Processing Feature
- Effective High Memory Throughput
- 0.3μm CMOS Technology
- High Operating Frequency
- Low Power

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Architectural Features

- Support for Uncacheable Memory Pages
- Pseudo Vector Processing Feature based on Slide-Windowd Registers (PVP-SW)
  - -Utilize Software-Pipelining Technique
  - -Flexible Software-Supported Register Renaming
- Architectural Extensions
  - -Slide-Windowed Floating-Point Registers
  - -Preload Instruction
  - -Poststore Instruction

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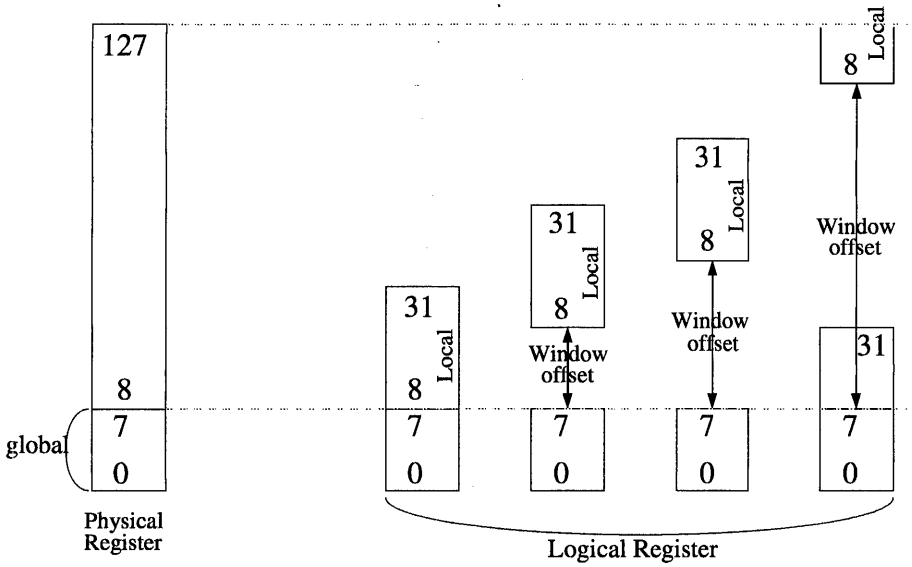
Slide-Windowed Floating-Point Registers



global registers - - - 8 or 12 or 16

Window offset = FWSTP (Floating Window STart Pointer)

FWSTPset instruction

Preload Instruction

- Directly specify 128 Physical FPRs
  - -to hide Memory Access Latency
  - -7-bit register number
- Data Transfer from Main Memory to FPR directly
  - -No Cache Pollution
- Preload 8B Data / cycle
  - -1.2GB/s Peak Transfer Rate @ 150MHz
- Compatibility with Cache

1st cache	2nd cache	Action
hit	don't care	1st cache -> FPR
miss	don't care	M.M. -> FPR

6.4-07

Poststore Instruction

- Directly specify 128 Physical FPRs
  - -to hide FP Latency
  - -7-bit register number
- Compatibility with Cache
  - -1st or 2nd cache hit -> Cache Store and M.M. Store
  - -1st and 2nd cache miss -> M.M. Store only

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Processor Core Features

- Superscalar with 2 Instruction Issues
- Up to 4 Operations / cycle
- 2 Integer ALUs, 2 SMUs(Shift Merge Unit)
- 2 Floating-point Operations(FMPADD) / cycle
- Branch History Table with 2-bit x 1024 Entries

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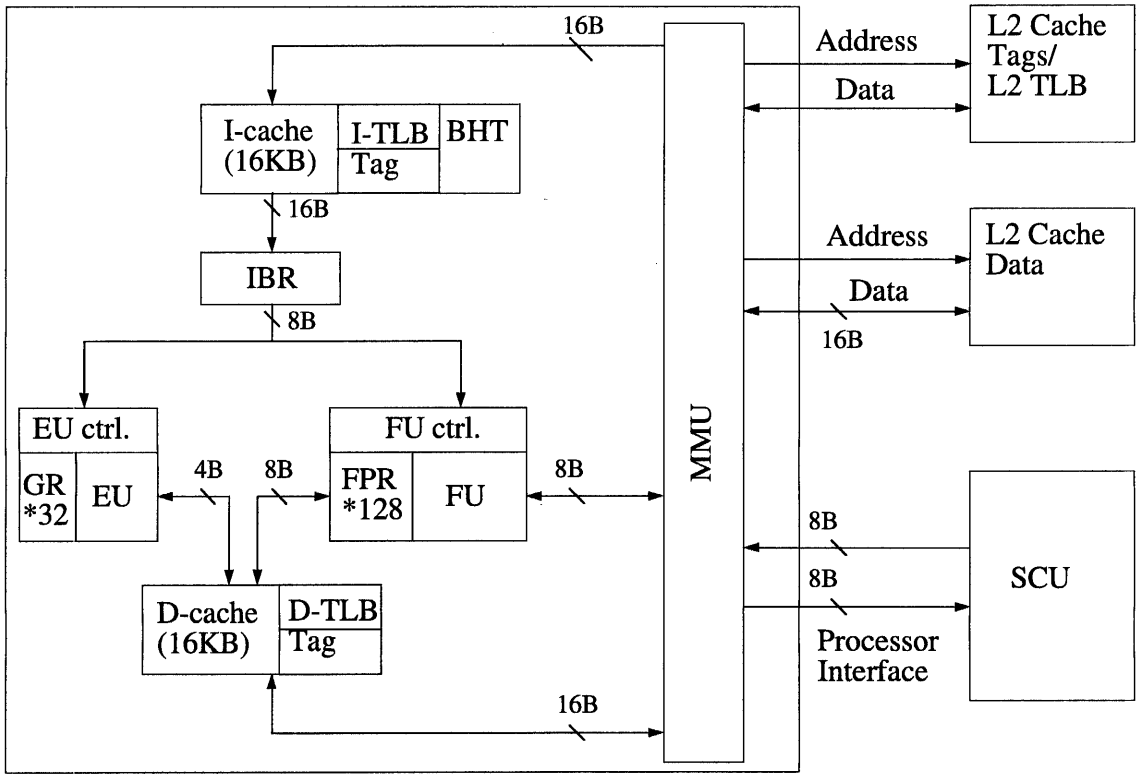
Chip Block Diagram



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TLB Organization

- 1st Level TLB

  I-TLB 256 Entries direct mapped
  6 Block Table Entries 512K-32MB/Entry
  1 Anti-Thrashing Entry

  D-TLB 256 Entries direct mapped
  6 Block Table Entries 512K-32MB/Entry
  1 Anti-Thrashing Entry

- 2nd Level TLB

  I-TLB 1K-4K Entries 2 way set associative

  D-TLB 1K-4K Entries 2 way set associative

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Cache Organization

- 1st Level Cache

  I-Cache 16KB
  D-Cache 16KB
  Direct Mapped , 32B / Block
  Single Bit Error Detection Parity

- 2nd Level Cache

  I/D Combined 512KB-8MB
  Direct Mapped , 128B / Line
  Single Bit Error Correction, Double bits Error Detection ECC / 4B

- Cache Miss Optimization
  - -Hit under Miss
  - -Pipelined Instruction Prefetching (up to 4)

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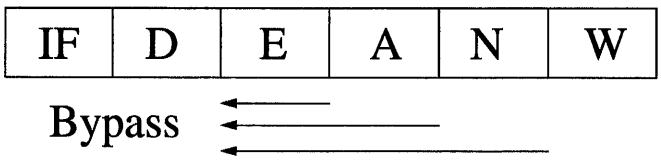
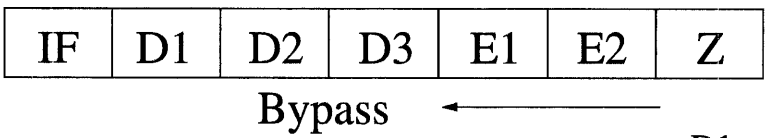
Integer Pipeline : 6 stages



IF : Instruction Fetch
D : Decode
E : Execution
A : Cache/TLB Access
N : Nullification / Interruption
W : GR Write

Floating Pipeline : 7 stages



D1 : FPR Number Conversion
D2 : Dependency Check
D3 : Source Operand Read
E1 : Execution 1
E2 : Execution 2
Z : FPR Write

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FP Latency and Issue Rate

	Single Precision		Double Precision	
	Latency	Issue Rate	Latency	Issue Rate
Add, Sub	2	1	2	1
Multiply	2	1	2	1
FMPYADD, FMPYSUB	2	1	2	1
Divide	10	9	17	16
Square Root	16	15	30	29

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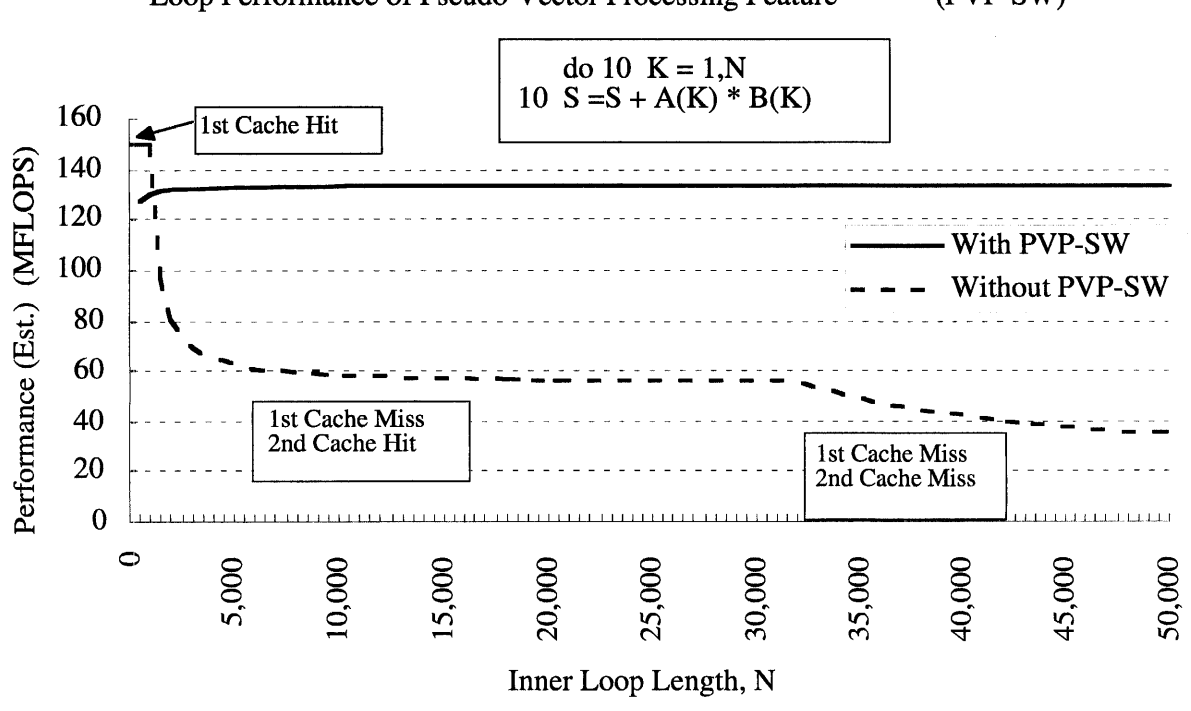
Performance



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Physical Characteristics

Process Technology	0.3 μm CMOS
Cycle Time	150 MHz (*1) > 200 MHz (*2)
Die Size	15.7 mm x 15.7 mm
Number of Transistors	4.5 M
Package	1672 pin CCB (C4) , 520 signals
Power Supply	2.5 V
Power Dissipation	13 W @ 150 MHz
Peak MFLOPS / W	23 MFLOPS / W

(*1) Worst Silicon Processing and Worst Environment

(*2) Typical Silicon Processing and Worst Environment

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Device Characteristics

- CMOS Circuit

Ldrawn	0.3 μm
Leff	0.25 μm
Tox	6.5 nm

- Interconnection

Layers 4 Metal layers

	Width (μm)	Thickness (μm)	Pitch (μm)		
			Uncontacted	Contacted	Design Rule
AL1	0.5	0.65	1.0	1.4	1.4
AL2	0.5	0.65	1.0	1.4	1.4
AL3	1.4	1.15	1.8	2.4	2.8
AL4	1.4	1.45	2.8	2.8	2.8

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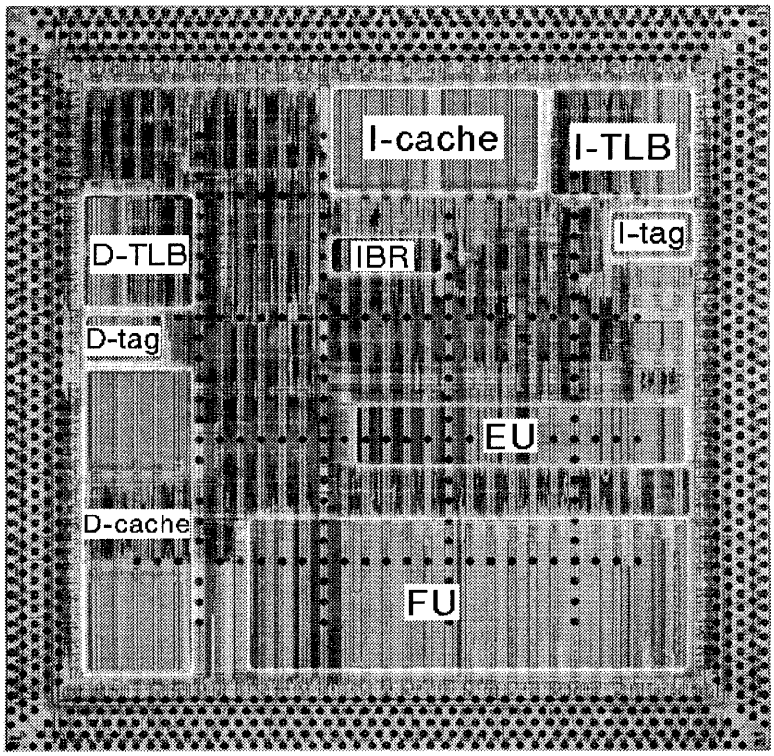
Chip Photograph



Summary

- High Performance Superscalar RISC Processor
- PVP-SW Feature Support
- Optimized to Large Scale Scientific Calculations
- High Memory Throughput
- High Clock Frequency