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Title: VLSI Architecture of the I-Frame Encoder for the MPEG-2 Video Compression

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Abstract

The recently announced IBM I-Frame Encoder chip compresses real-time digital video input into the MPEG2 standard at MP@ML. The standard specifies the syntax of the compressed bitstream and it allows considerable flexibility in choice of encoding parameters and options for application specific. The performance requirement and design complexity of these parameters becomes a challenge for the encoder architecture. This paper presents the main characteristics of the video encoder chip. The descriptions of particular co-processors are given in terms of functions and application environments. This VLSI chip has been designed, fabricated and is encoding image sequences in our laboratory. It can compress a 30 frame or 60 field/sec image sequence at 720 pixels x 480 lines. The normal power dissipation is 2.1 Watts at an operating frequency of 54 MHz in 0.5u CMOS technology. The I-Frame chip is the first of a series of encoder chips. It has a scalable architecture that provides a growth path for future expansions.

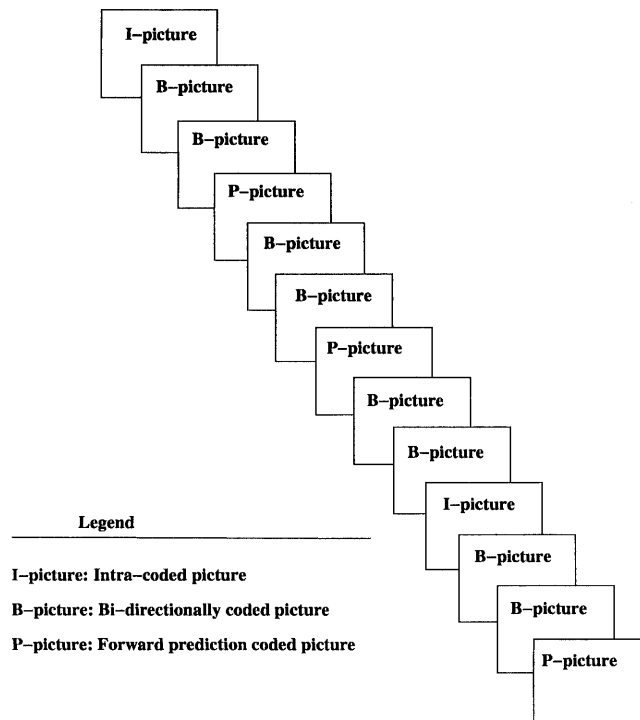
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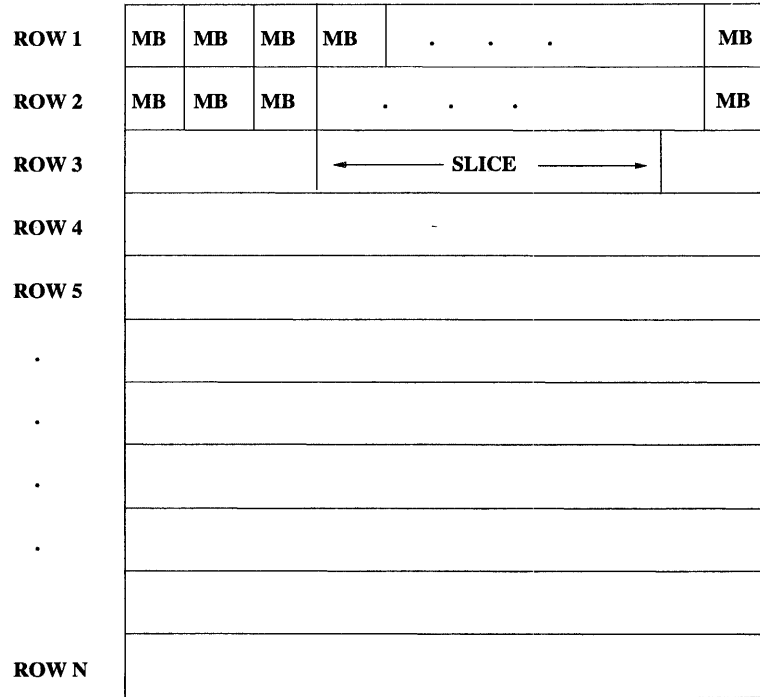
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Typical Picture Sequence

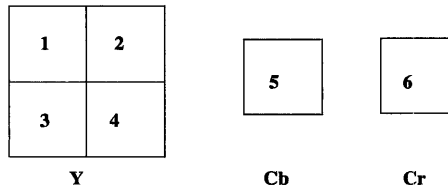


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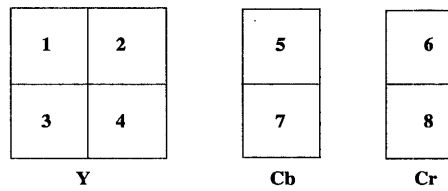
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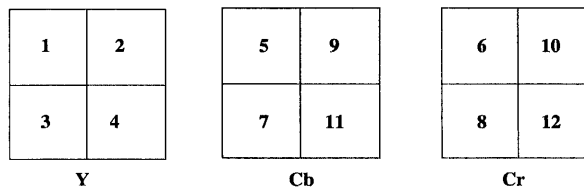
MPEG (4:2:0) format



MPEG (4:2:2) format



MPEG (4:4:4) format



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ENCODER FEATURES

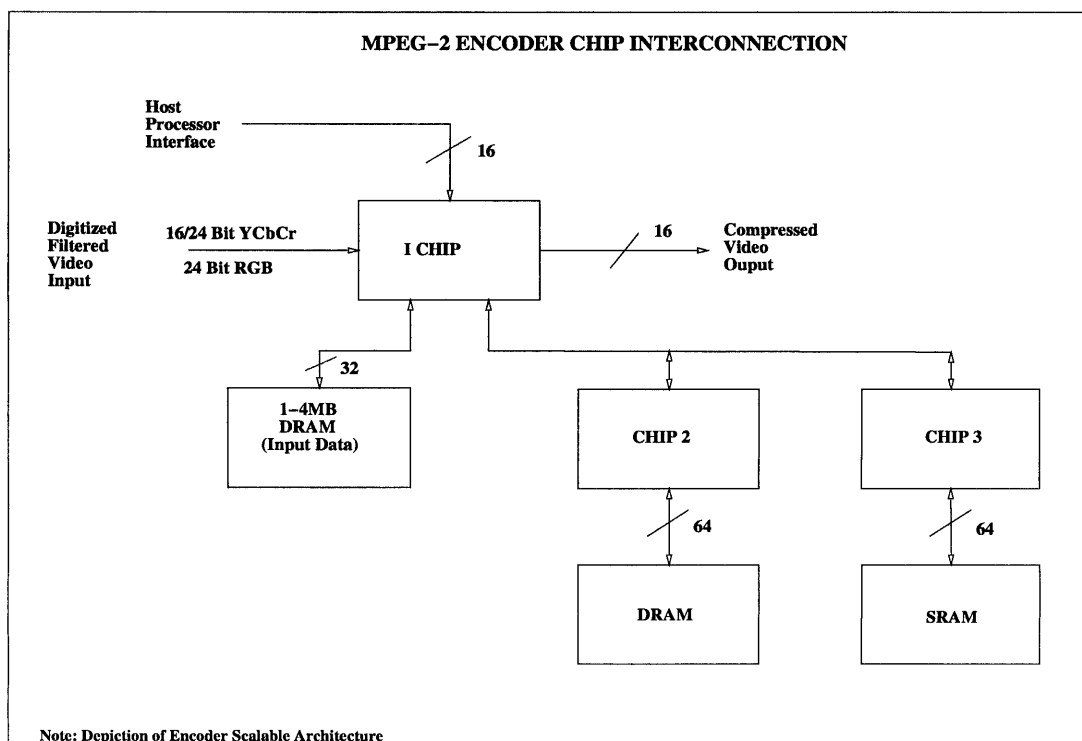
- Selectable MPEG1/MPEG2 encoding format
- Conformance with MPEG-2 MP@ML
- Real time encoding of picture resolution up to 496/512 NTSC/PAL lines/frame, 720 pels/line
- RGB input
- 16/24 bits YCbCr input
- CCIR 601 to HHR
- CCIR 601 encoding of 4:2:2 chroma format
- User specific quantizer tables
- Combined/dedicated luminance and chroma quantizer tables
- 3/2 pulldown
- 4:2:2 to 4:2:0 conversion
- Select compression parameters via 16 bit host interface
- Field and frame encoding
- 8 - 11 bits DC precision
- Automatic adaptive quantization and rate controls
- Output compressed data through host interface
- Output compressed data to FIFO
- External FIFO feedback for more accurate rate controls
- Produce up to 40+ Mb/s compressed data rate
- User data
- Includes hardwired functions for performance and programmable functions for flexibility

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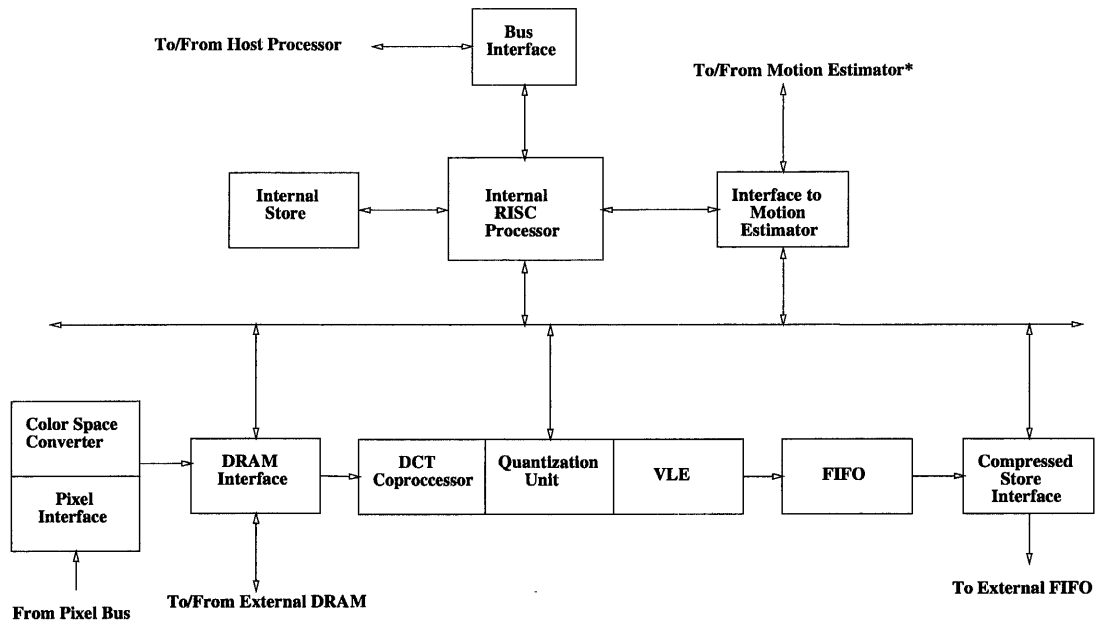
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I-Frame Video Encoder Module



* For future expansion

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PIXEL INTERFACE

- Interface maximum clock rate = 13.5 MHz
- Provides synchronization between internal circuits (54 MHz) and interface
- Accepts both 16 bit and 24 bit YCbCr data
- Converts 24 bit RGB to YCbCr (4:4:4)

$$Y = 077 * R / 256 + 150 * G / 256 + 029 * B / 256$$

$$Cb = 131 * R / 256 - 110 * G / 256 - 021 * B / 256 + 128$$

$$Cr = -044 * R / 256 - 087 * G / 256 + 131 * B / 256 + 128$$
- Converts 4:4:4 to 4:2:2 (3:2 data reduction) or 4:2:0 (4:3 data reduction)
- Component format data accumulated in external DRAM

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MEMORY INTERFACE

- **Control interface of encoder DRAMs**
 - **Store incoming pixel data in Y & UV pairs**
 - **Read out picture data by macroblock**
 - **Refresh and POR (Power On Reset) reset of DRAMs**
 - **Host read/write of DRAMs**
- **Compatible with Off The Shelf DRAMs (Industry Standard)**
 - **Glueless interface**
 - **70 ns access time**
 - **2 or 1 CAS lines**
 - **2 or 1 WE lines**
 - **1M x 16, or 256K x 16, or 1M x 8 DRAMs**

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HOST INTERFACE

- **Generic 16 bit data, 8 bit address interface**
- **Encoder chip designed as a register port to the external processor**
- **Control of the encoding process by writing registers in the chip via this interface:**
 - **Encoding parameters registers: GOP length, qscale, scan format, etc.**
 - **Encoded bitstream formats: Field/frame picture encoding, 4:2:2:/4:2:0 chroma format, frame rate, bit rate, picture aspect ratio, etc.**
 - **Chip initialization: Chip microcode, tables and personalized registers are loaded by commands**
 - **Diagnostic functions: Read/write external DRAM and chip registers**
 - **Operation commands: Start encoding, read status and host interrupts**
 - **Low performance uses: Compressed data retrieved through host data bus**

INTERNAL RISC PROCESSOR

- 54 MHz RISC processor to meet performance and flexibility requirements
- 2K 4-byte instructions can be stored on chip and executed
- Processor features:
 - "Dynamically partitionable":
 - Single 4 byte instructions (UNI mode)
 - 4-1 byte instructions (Logical Partition - LP mode)
 - Four specialized arithmetic and logical units (ALUs) are core for these operations
 - Other functions: Branch/loop processor, register/memory interface unit, and condition registers
- Processor functions:
 - Adaptive Field/Frame DCT
 - Adaptive quantization
 - Rate control
 - Picture bit allocation

DISCRETE COSINE TRANSFORM (DCT) UNIT

- Distributed arithmetic version used for high throughput
- Processing performed on block (8 x 8 pixels) basis
- 2-dimensional DCT on a block decomposed into two 1-dimensional DCT calculations
 - Data is processed in the first dimension, or row order
 - Results are stored in a transpose memory, i.e. rows become columns and columns become rows
 - After transposition, the data is processed in the second dimension, or column order
- One dimensional Discrete Cosine (DCT):

$$x(n) = \sqrt{\frac{1}{N}} X(0) + \sqrt{\frac{2}{N}} \sum_{k=1}^{N-1} \cos \frac{(2n+1)\pi k}{2N} X(k)$$
- Order of the words within a block is raster scan, i.e. non-zig-zag order
- DCT processes blocks both luminance and chrominance blocks in the same fashion
- Results from the DCT are sent to the quantization unit

QUANTIZER

- Quantize coefficients from DCT
 - Quantizing algorithms
 - Intra macroblock's DC coefficients
 - Intra macroblock's AC coefficients
 - Programmable options of Quantizer
 - Quantize stepsize for DC coefficients
 - Quantize matrix tables
 - Default/user quantizer matrix tables
 - Number of quantizer matrix tables to use for quantization
 - Quantizer stepsize for AC coefficients
 - Fixed
 - Variable

VARIABLE LENGTH ENCODER (VLE)

- Quantizer coefficients encoding
 - DC coefficient encoding
 - AC coefficient encoding
- Macroblock header data encoding
 - Macroblock type
 - Macroblock address increment
 - Motion vectors

COMPRESSED STORE INTERFACE

- **Assembly of headers with VLE data**
 - **Sequence layer headers through macroblock layer headers**
 - **User quantizer matrix tables**
 - **User data**
- **Interface for Compressed Data Store**
 - **FIFO**
 - **DRAM**