

# A Two-Chip Real-Time MPEG2 Video Encoder with Wide Range Motion Estimation

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4.1-02

## Key Features

- Low-delay SP@ML video encoder
- Wide-range motion estimation using hierarchical telescopic search
- Flexible macroblock-level pipeline architecture based on RISC CPUs
- Three small peripheral memories

### Comparison between SP@ML and MP@ML

Items		SP@ML	MP@ML (M =3)
Delay due to Motion Estimation		> 0.5 Frame **	> 3 Frames
Frame Memory Capacity		10 Mbits	26 Mbits
Frame Memory Access Rate*		133 MBytes/s	332 MBytes/s
Operating Performance Required for Motion Estimation*		3.2 GOPS	8.0 GOPS
Degradation Compared to MP@ML	SNR at 4 Mbps	0.3 - 1.2 dB	—
	Quality for Actual NTSC-Grade Video	Negligible	—

\* Hierarchical telescopic search used by our encoder chip set

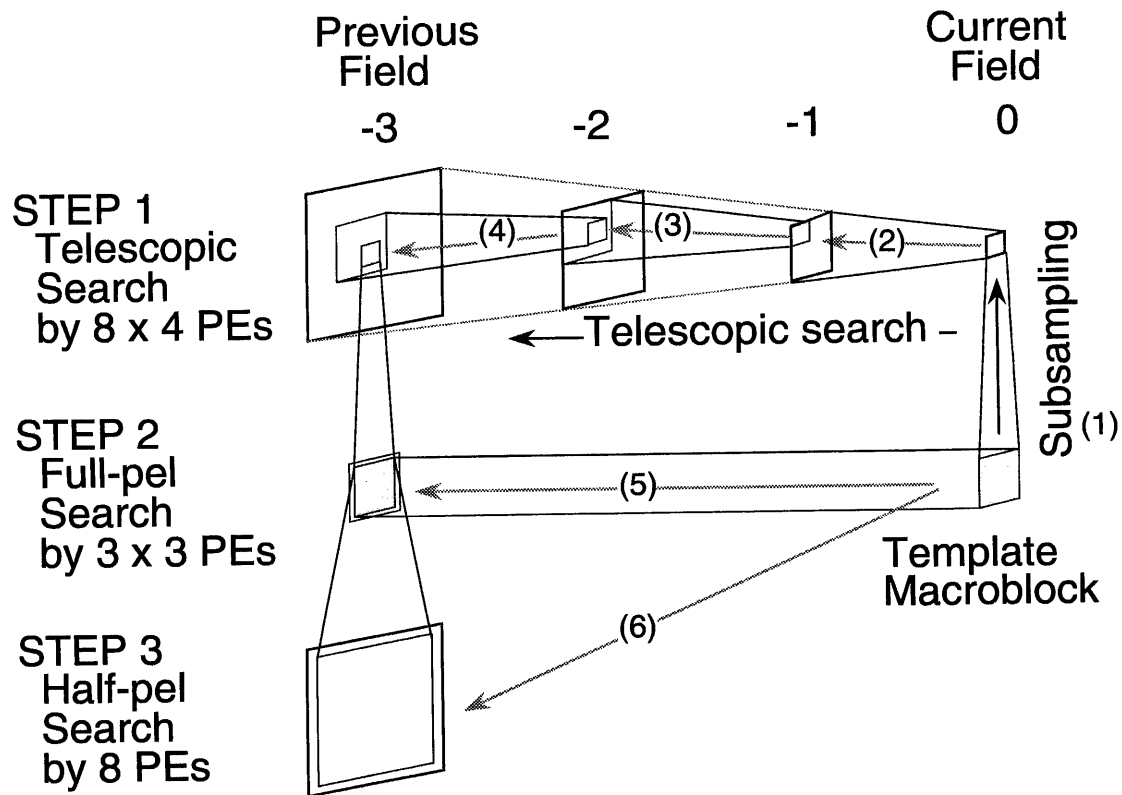
\*\* Frame structure

### Comparison of Moving Vector Search Methods

Items	Two-Step Exhaustive Search*	Hierarchical Telescopic Search
Required Operating Performance	100 GOPS	3.2 GOPS
Required Nominal Memory Access Rate	155 MBytes/S	133 MBytes/S
Signal to Noise Ratio		
Flower Garden	28.8 dB	28.6 dB
Mobile & Calender	26.9 dB	26.7 dB
Football	35.1 dB	34.8 dB

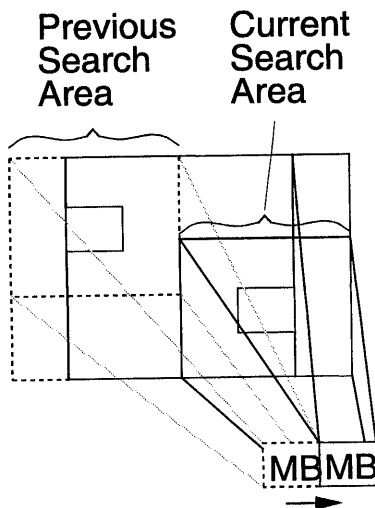
\* First step : full-pel-precision full search  
 Second step : half-pel-precision full search

**Three-Step Hierarchical Motion Estimation**



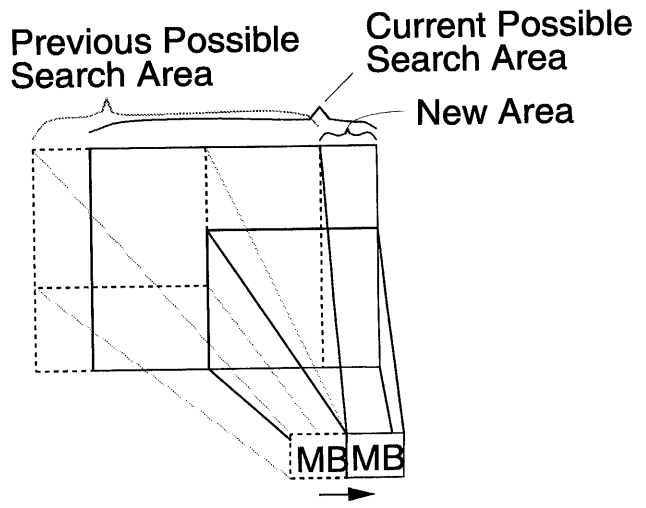
**Reduction of Frame Memory Access Rate by Full Buffering**

No Buffering



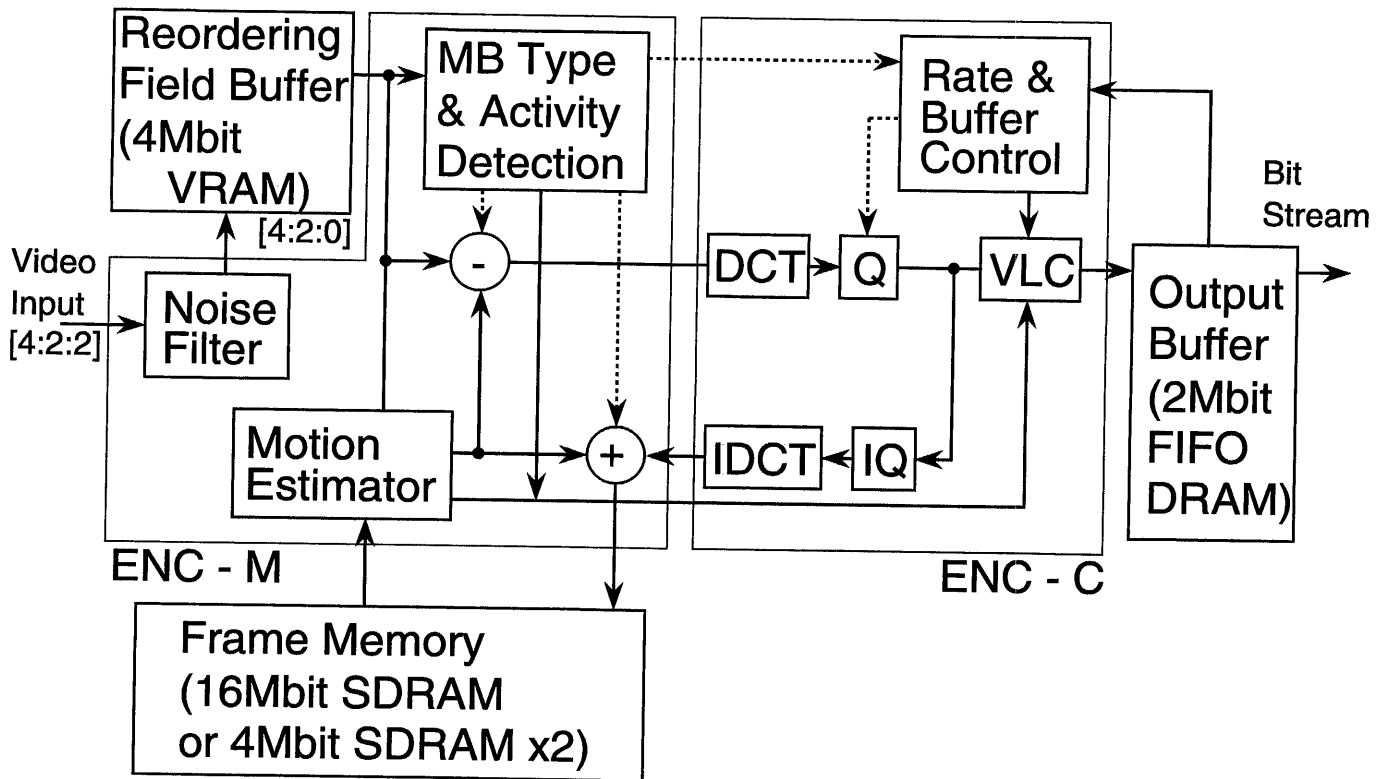
**Current Search Area = 3 x MB**

Buffering of Total Possible Search Area

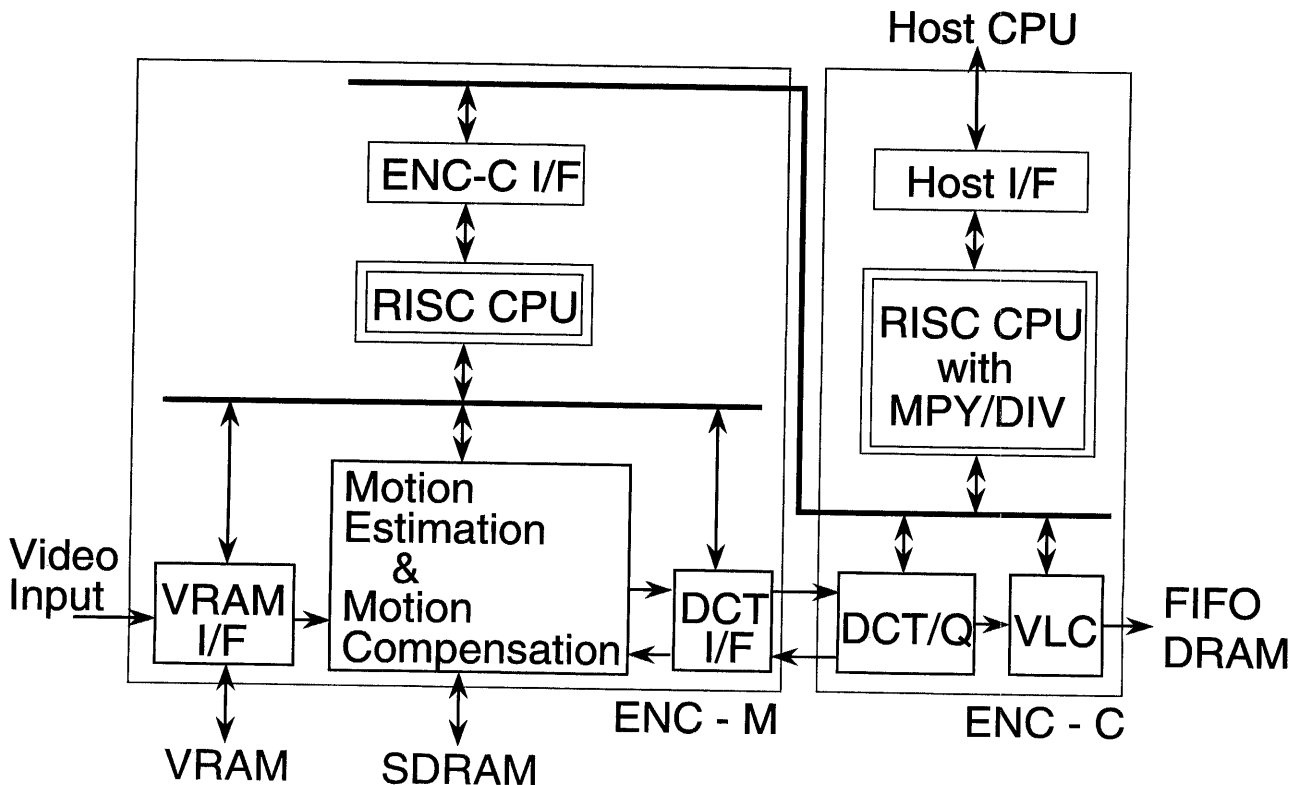


**New Area = 5 x MB**

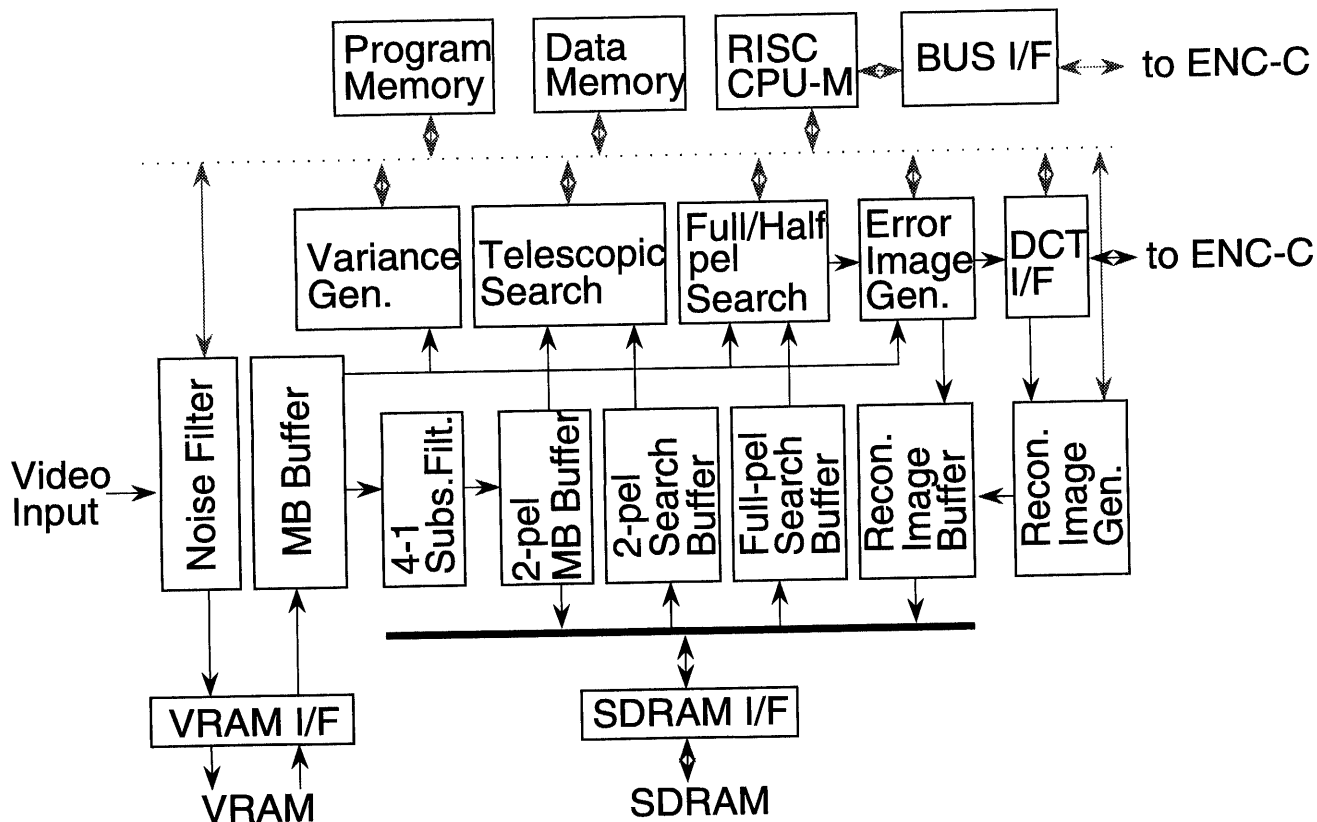
**Function Partitioning in MPEG2 Encoding Procedure**



**Flexible Pipeline Architecture Based on RISC CPUs**

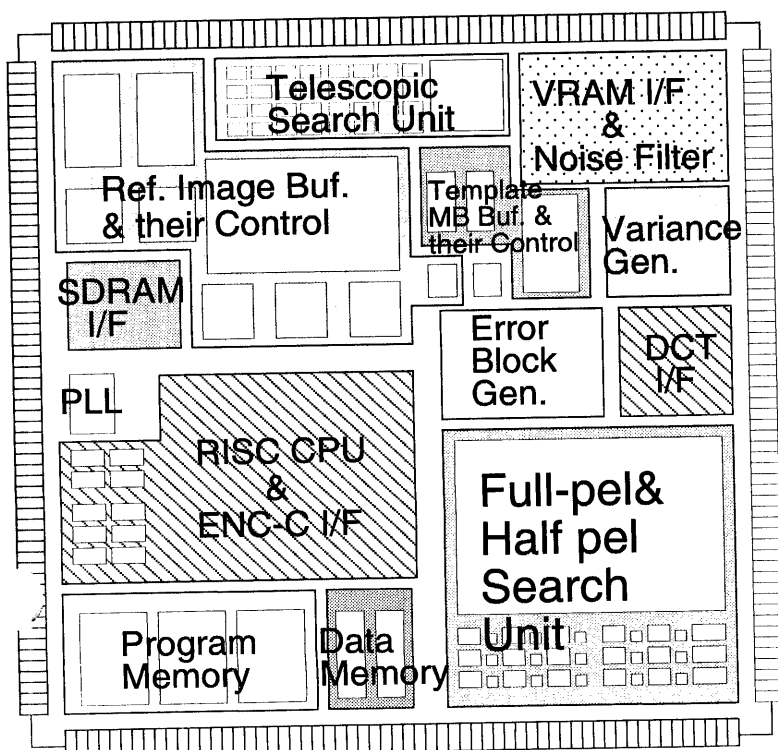


## Diagram of Motion Compensation Chip (ENC-M)



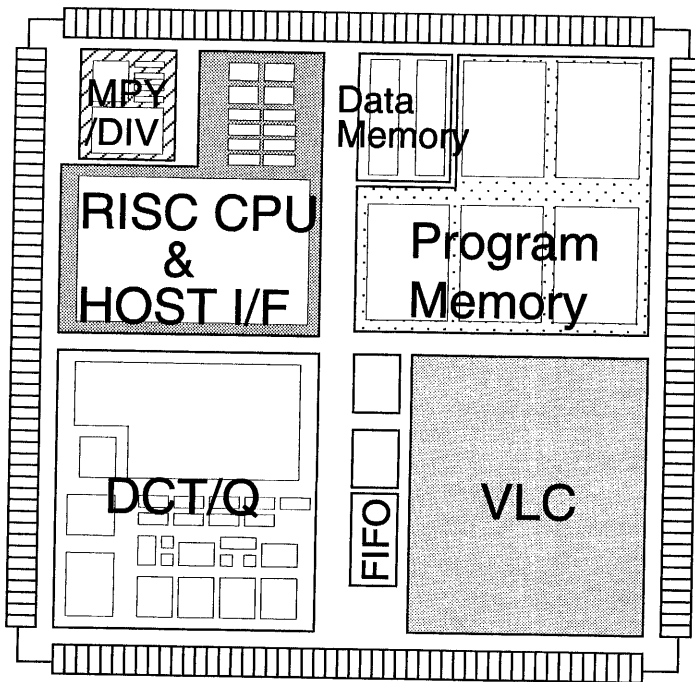
4.1-10

## Layout of ENC-M Chip



- 0.5- $\mu\text{m}$  triple-metal CMOS
- 2.0 million transistors
- Logic : 150k G
- Memory:
  - Program 24bx3.5kw
  - Data 16bx1kw
  - Others 91kb
- 16.5 x 16.5 mm<sup>2</sup> die size
- 81-MHz clock
- 3.5 Watts @ 3.3 V
- 340-lead CQFP

## Layout of ENC-C Chip



- 0.5- $\mu\text{m}$  triple-metal CMOS
- 1.3 million transistors
  - Logic : 75k G
  - Memory:
    - Program 24bx5kw
    - Data 10bx1kw
    - Others 20Kb
- 14.0 x 14.0 mm<sup>2</sup> die size
- 81-MHz clock
- 2.5 Watts @ 3.3 V
- 204-lead CQFP

## Video Encoder Specifications

Standard	MPEG2 SP@ML
Frame Size	720 x 480 / 720 x 576 / 640 x 480 (variable)
Video Input Format	4 : 2 : 2
Frame Rate	Up to 30 frames/s (Up to 40,500 macroblocks/s)
Bit Rate	Up to 15 Mbps
Picture Structure	Frame Structure
Motion Estimation Search Range	Frame: -32/31.5 h x -32/31.5 v Field : -48/47.5 h x -24/23.5 v
Encoder Delay	85 ms