Memory Performance Features of the 64-bit PA-8000

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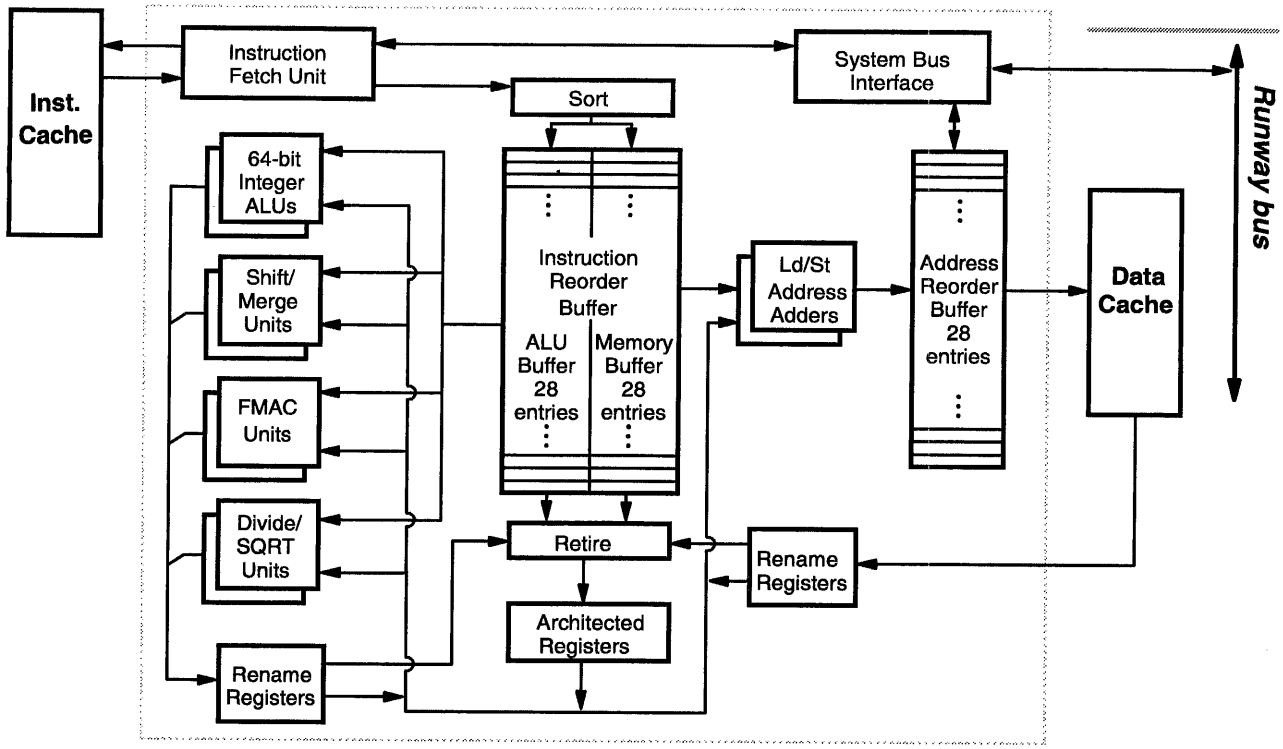
PA-8000 - Overview

- Leadership Performance
  - > 360 SPECint92
  - > 550 SPECfp92
  - > 700 TPS (est.) Uniprocessor
- 56 Entry Instruction Reorder Buffer
- 8 Computational Units
- 2 Load / Store Units
- 4 Instructions Executed / Cycle

PA-8000 - Block Diagram

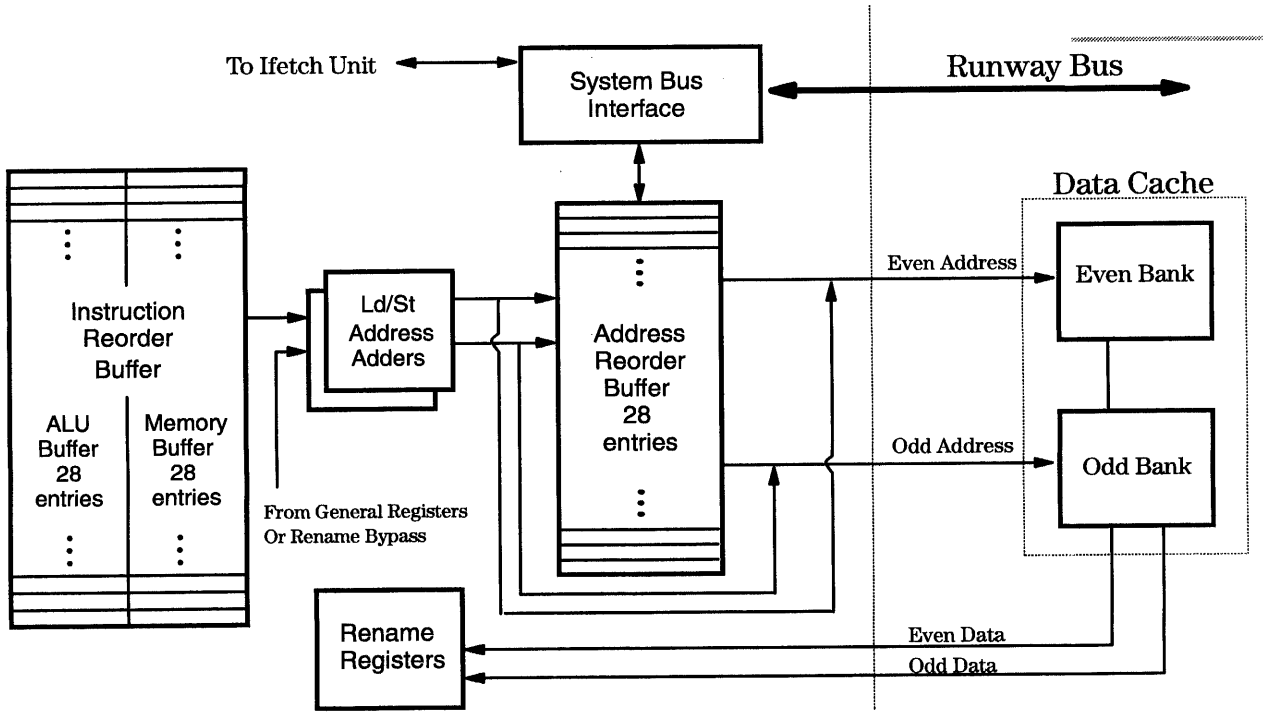


PA-8000 - Memory Performance

Three Major Design Considerations

- How to Maximize Memory Performance When Data is in Cache
- How to Maximize Memory Performance When Data is Not in Cache
- How to Maximize Performance Scaling in MP Systems

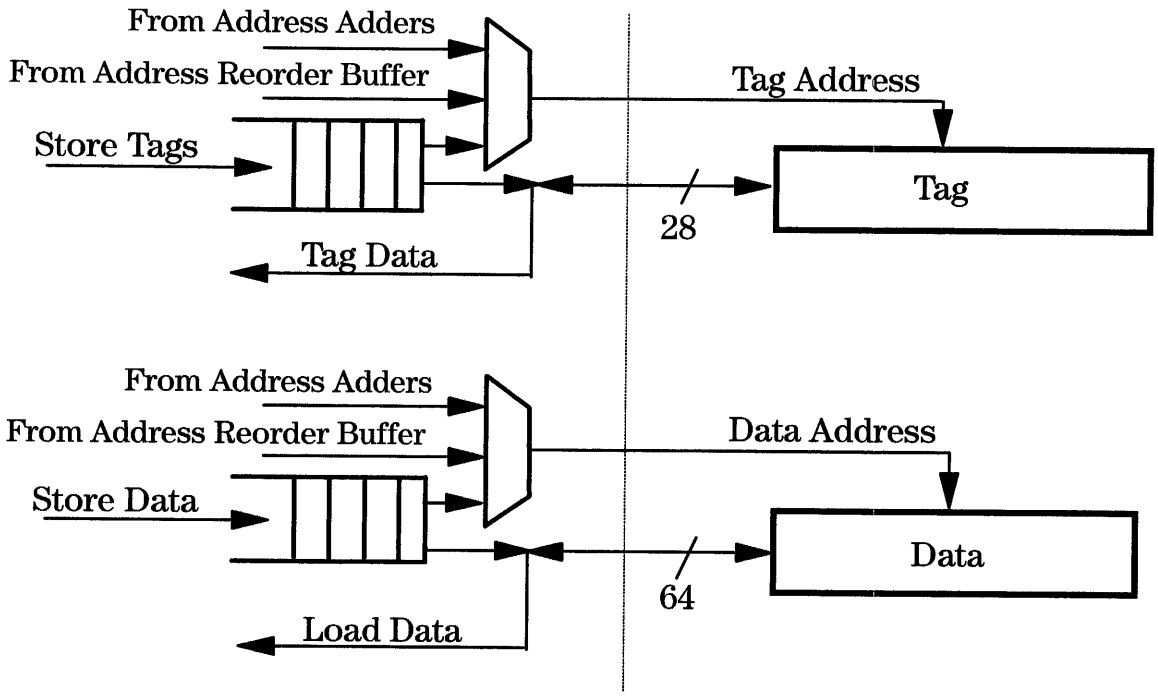
PA-8000 - Memory Subsystem



PA-8000 - Data Cache

- Large, Single-Level Off-Chip Cache
- 2 Cycle Latency
- Industry Standard Synchronous SRAMs
- Two Way Interleaving of Odd / Even Banks
- Dual Copies of Tags

PA-8000 - Data Cache Detail



PA-8000 - Data Cache: Opportunities for Parallelism

Transaction	Cache Activity Required
Load - Hit	1 Tag Read + 1 Data Read
Store - Hit - Non-Dirty	1 Tag Read + 2 Tag Writes + 1 Data Write
Store - Hit - Dirty	1 Tag Read + 1 Data Write
Coherency Check - Miss	1 Tag Read

PA-8000 - Data Cache Access Sequence Example

Read Cycles:
- 3 Data Loads to A, B, C
- 1 Coherency Tag Check to D
- 2 Store Tag Checks to E,F

Write Cycles:
- 5 Data Writes to G,H,I,J,K
- 2 Dirty Bit Tag Updates to G,K

Data Cache Bus Activity

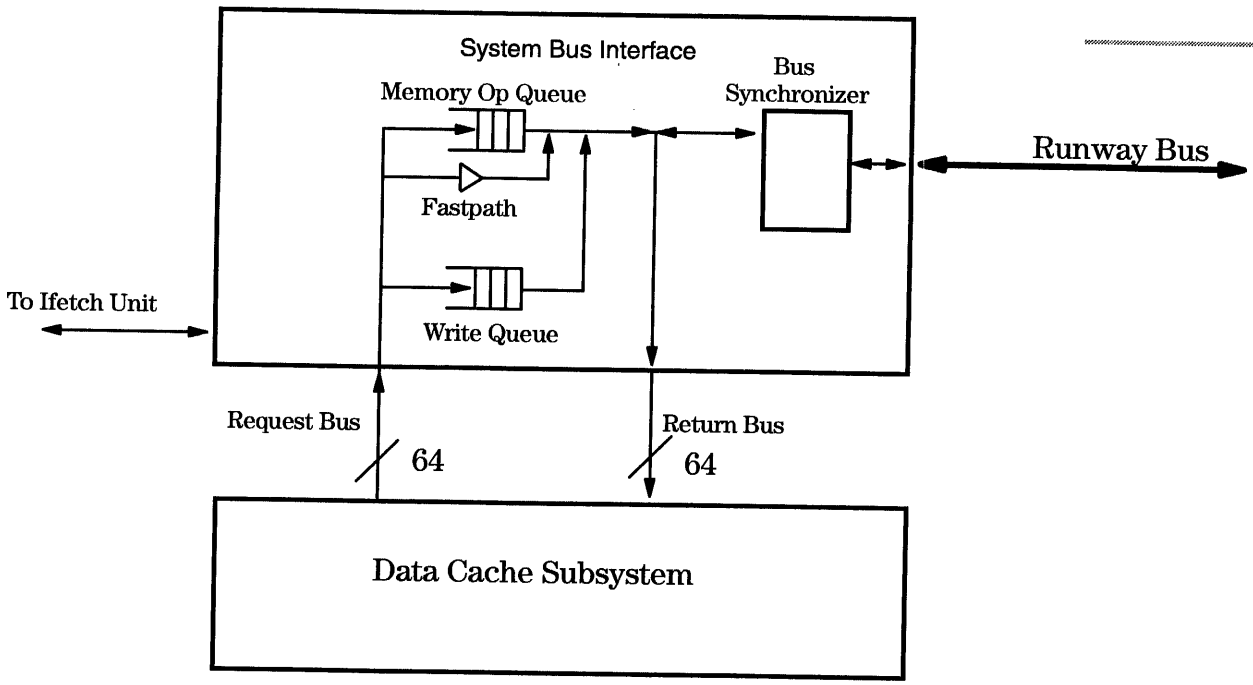
	Even Bank		Odd Bank	
CYCLE	TAG	DATA	DATA	TAG
0	STORE E (Tag Check)	STORE G	STORE H	STORE G (Tag Update)
1	STORE F (Tag Check)	STORE I	STORE J	STORE K (Tag Update)
2	LOAD A	LOAD A	STORE K	COHERENCY D (Tag Check)
3	LOAD B	LOAD B	LOAD C	LOAD C

Read Write

PA-8000 Memory Subsystem: Cache Misses to Main Memory

- Out Of Order Execution Hides Latency
- Load to GR0 Prefetch
- Efficient Path to Runway Bus

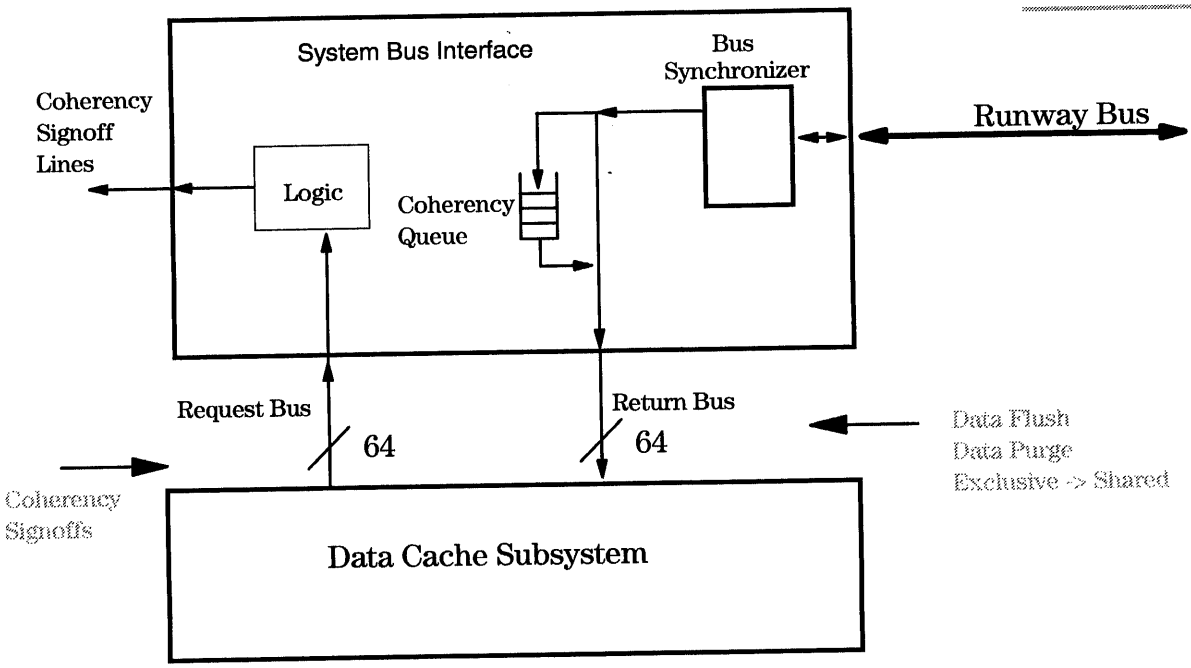
PA-8000 - Cache Miss Path



PA-8000 - Memory Subsystem: Scalable Multiprocessing

- MP "Knowledge" Kept Out Of Data Cache Subsystem
- Minimal Overhead For Processing Coherency Checks

PA-8000 - MP Coherency Path



Summary

- PA-8000 Memory Subsystem Provides Superb Memory Performance
  - Aggressive Data Cache:
    Flexibility + Parallelism → Bandwidth
  - Optimized Accesses to Main Memory:
    Parallelism + Low Latency
  - Scalable MP:
    Simple, Low Overhead Coherency