Advanced Micro Devices

AMD-K5™ Microprocessor

HOT Chips VII

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Presentation Summary

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- **Architecture Review**
- **Features & Performance Examples**
- **Design Tradeoffs**

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Highlights

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- About 2.5x 486 and 1.3x Pentium performance at the same clock
- Efficient support for 16-bit code and mixed operand sizes
- AMD-specific architectural extensions
- P54C pin compatible
- Static, 3.3 volt design
- 100% AMD design
- Baseline microarchitecture for a family of superscalar processors

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General Approach

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- x86 instructions are cached in partially decoded form
  - removes the serial process of locating key instruction bytes during decode
  - keeps pipeline short
- Instructions from the cache are processed into a stream of internal RISC operations (ROPs)
- ROPs are dispatched 4 at a time to a superscalar core modeled after a 29K superscalar RISC with extensive modifications to handle x86 idiosyncrasies
- Complex instructions (e.g. string move, far call) trap to a microcode ROM that also issues 4 ROPs per cycle

Instruction Translation Example

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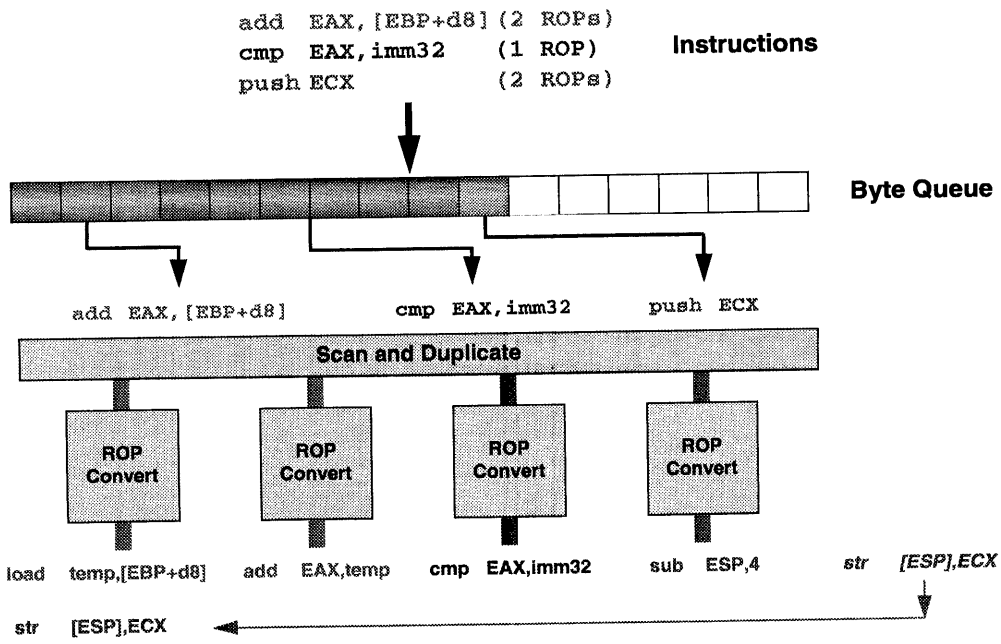

Block Diagram

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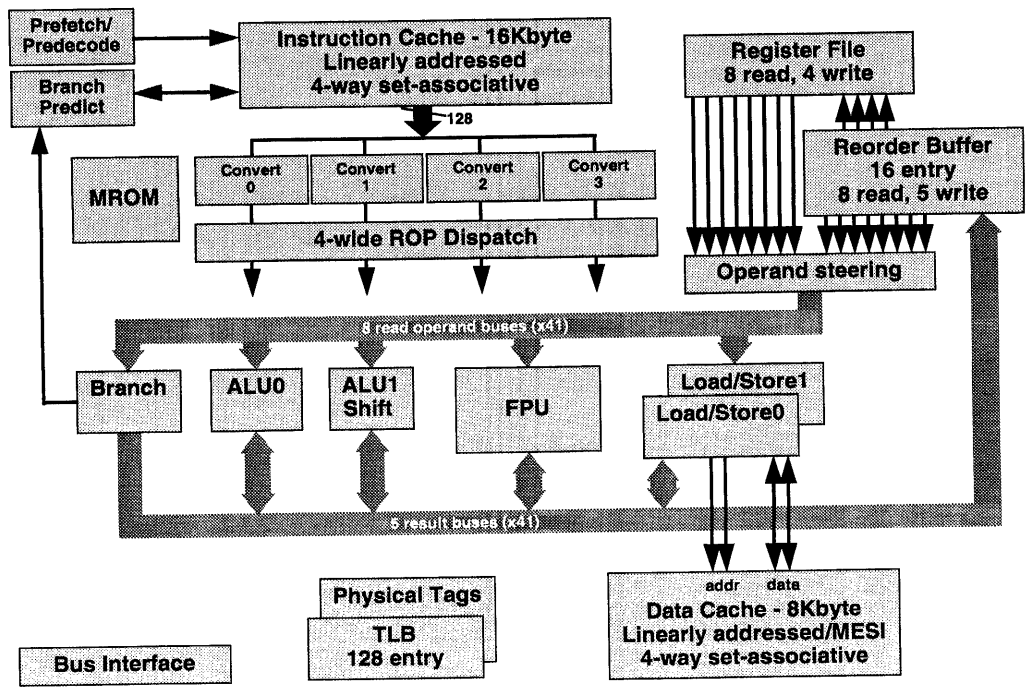

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Pipeline Timing

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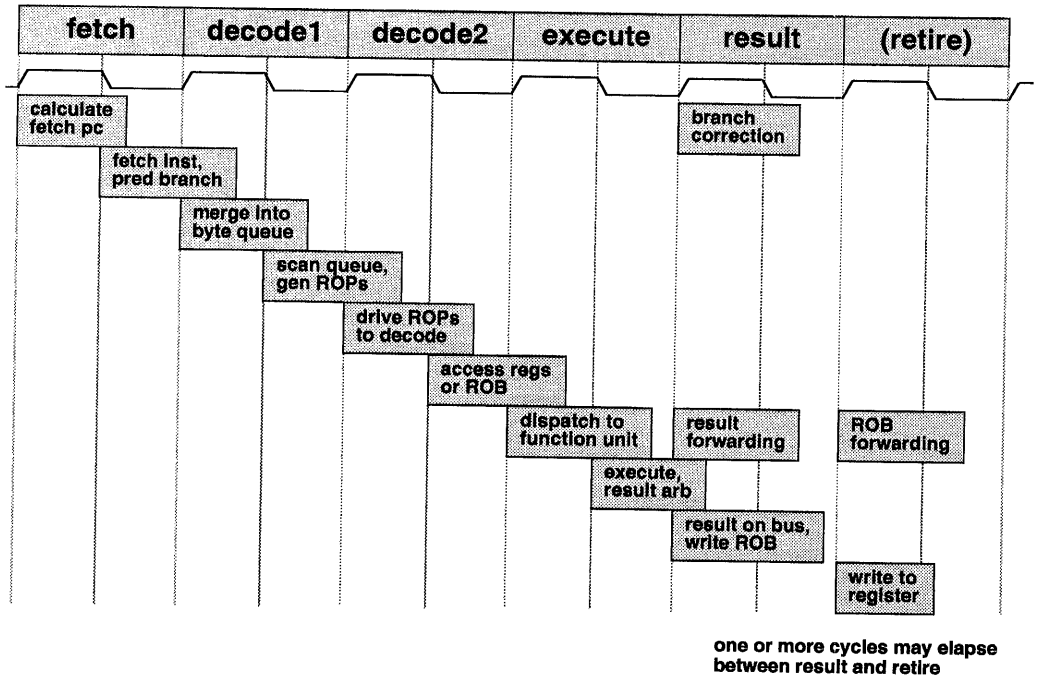

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Superscalar Core

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- Full out-of-order issue and completion
- Speculative execution
- Register renaming with a 16-entry reorder buffer (ROB)
  - plus a renaming table for floating-point stack management
- 5-stage pipeline (effective, 6 stages actual)
  - 1-cycle load even with full base+index+disp+seg addressing
  - 1-cycle penalty for an unaligned access
- 6 parallel function units (all single-cycle except f.p.):
  - 2 integer/shift, 2 load/store, branch, floating-point
- No instruction grouping requirements for parallel issue

Performance Features

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- 16K 4-way associative instruction cache, split line access
- 8K 4-way associative dual-access data cache
- 128-entry, 4-way associative TLB
- Up to 1024 taken branch predictions
- Fast branch recovery
  - 3-cycle maximum recovery time, may be partly to completely hidden by overlap with prior instruction execution

Performance Features cont'd

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- Fast integer multiply
  - four cycle latency, fully pipelined, 32x32->32/64
- Only 1 ROP for stores (reportedly 2 uops on P6)
- No penalties for mixed operand sizes
  - transparent forwarding of partial register updates

    e.g. for
    ```
    mov al, byte1
    mov ah, byte2
    add ebx, eax
    ```
    AL and AH are merged with EAX[31:8] in the reservation station
- No prefix penalties for any number of any prefixes
- No pipeline flush on segment loads
  - fully parallel execution

Execution Example #1

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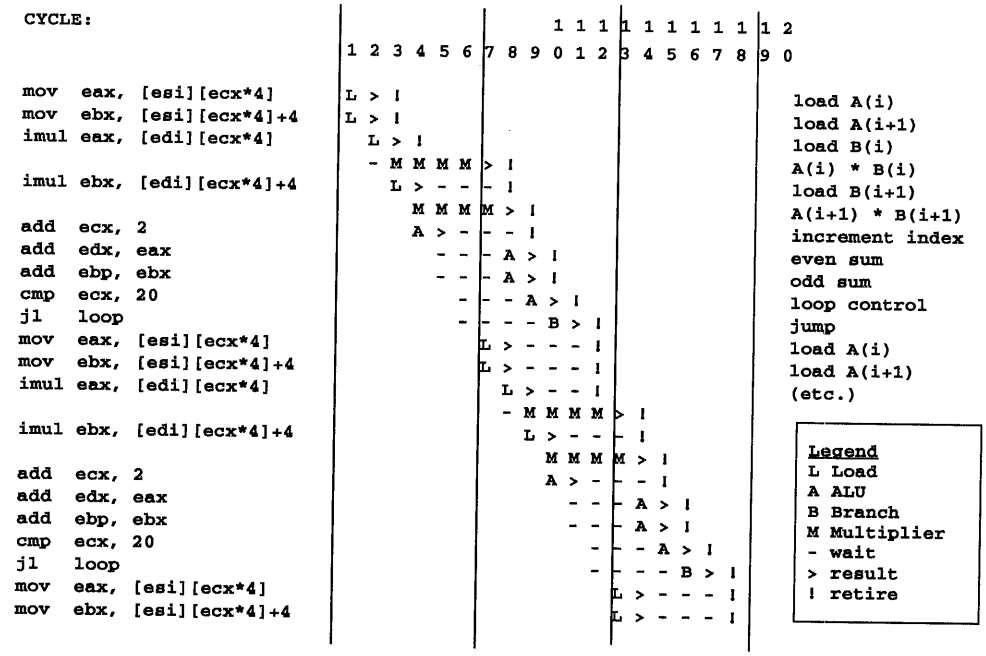
Integer Dot Product *3 cycles per MAC*



Execution Example #2

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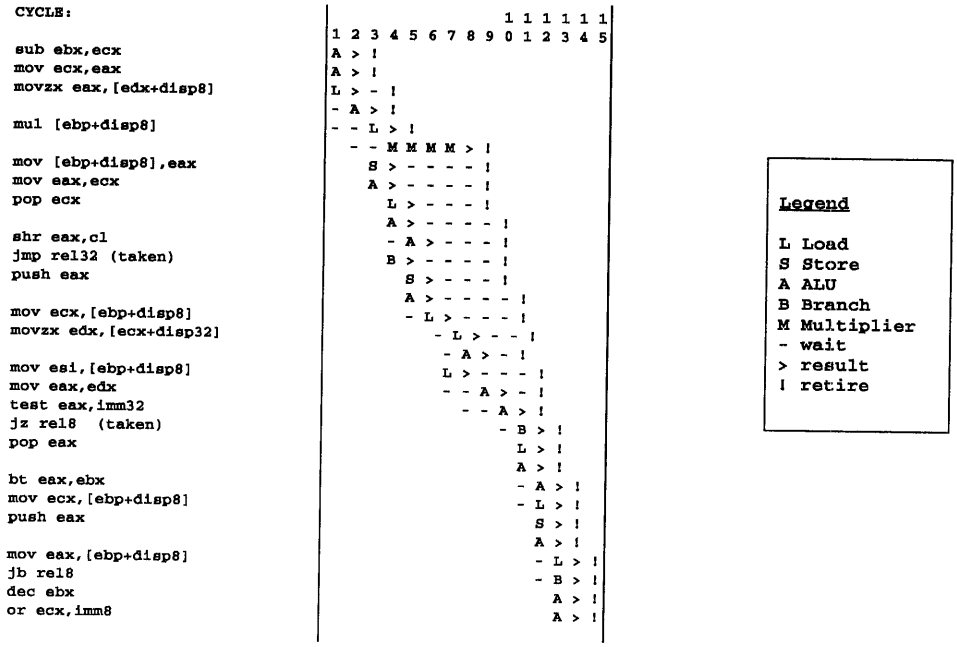
MPEG decoder -- off-the-shelf compiler



Cost/Performance Tradeoffs

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- Driven by trace-driven performance modelling of billions of instructions
- Optimized for desktop, not high-end server

➨ RISC-like microarchitecture
- RISC heritage is high-performance CISC microarchitecture
- trivial to track CISC instruction boundaries for ordering and precise exceptions
- very straightforward dependency checking
- simple functional unit design

➨ Distributed reservation structure
- much simpler issue logic than centralized scheme

Cost/Performance Tradeoffs cont'd

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➨ Dual Load/Store with single-cycle latency
- loads and stores are the primary bottleneck

➨ 1-bit branch prediction, cache-based
- greater capacity more than compensates for lower accuracy
- fast recovery 2-bit history not that beneficial

➨ No prefix penalties
- 16-bit ops in 32-bit code, segment overrides in 16-bit code

2.2-15

Architectural Extensions

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- Global pages (AMD extension)
  - allows OS to mark certain pages as global, to be preserved across TLB flushes
- Fast system call (AMD extension)
  - fast RISC-like privilege level switch
  - maintains system security
- Conditional move (AMD extension)
- System Management Mode with support for I/O trapping
- Model-specific registers
- CPUID support
  - "AuthenticAMD" vendor ID string
- Time stamp counter

2.2-16

K5 Die Photo

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